

Technical area

The invention relates to an electronic ballast for fluorescent lamps having an inverter in the form of a bridge arrangement comprising switch branches and capacitor branches, in which the inverter is supplied on the input side with the AC supply voltage via a rectifier circuit and connected on the output side to at least one load circuit which comprises the series connection of an inductor with the parallel circuit of a firing capacitor and a fluorescent tube, in which further the rectifier circuit exhibits on the input side a rectifier which is connected on the output side via at least one diode polarised in the forward direction for the rectified AC supply current to the charging capacitor forming the output of the rectifier circuit, and in which a sine correction capacitor is provided which connects the diode terminal on the side of the rectifier to the output-side terminal of the inverter on the side of the electrically effective bridge capacitor.

20 Prior art

An electronic ballast of this kind has already been disclosed, for example, in reference DE 33 19 739 A1. In this case, the sine correction capacitor serves the prescribed sine-wave form of the current which is picked up by the ballast from the grid during operation. As long as the switching rate of the inverter does not change, the ballast picks up a constant energy from the grid. The result of this is that the effective operational voltages are heavily dependent on changes in the supply voltage and/or on the load fed by the inverter. This dependence requires, inside the device, not only that the electrolytic capacitor which supports the DC supply voltage to the inverter is designed for a higher voltage value, but also necessitates special measures for monitoring this DC voltage. If the monitoring device detects an internal DC voltage which is too high, it either switches off the entire ballast or paralyses the sine correction function

effected by the sine correction capacitor. Grave operational disadvantages are inherent in both measures. In one case the fluorescent lamp is extinguished, in the second case the specified current pick up from the grid is no longer given, which leads to impermissible harmonics and a power factor deterioration.

Disclosure of the invention

The invention is based on the object of specifying a further solution for an electronic ballast of the kind mentioned above, which solution prevents the operational disadvantages described in case of changes in the AC supply voltage and/or in the load of the load circuit with the aid of simple measures in terms of circuitry.

According to the invention this object is achieved by the features as specified in Patent Claim 1.

Suitable configurations of the subject-matter according to Patent Claim 1 are specified in the further Patent Claims 2 to 7.

Short description of the drawing

In the drawing, the figures serve to further explain the invention.

Figure 1 shows a known embodiment of an electronic ballast which makes use of a sine correction capacitor,

Figure 2 shows a preferred embodiment of the electronic ballast according to the invention,

Figure 3 shows a timing diagram of the current through the charging inductor of the rectifier circuit of the ballast according to Figure 2, and

Figures 4-7 show the circuit according to Figure 2, the current at the various switching phases of the inverter being added thereto.

Best way for implementing the invention

The circuit for the electronic ballast known from DE-33 19 739 A1 according to Figure 1 comprises an

inverter WR to which the AC supply voltage UN is supplied on the input side via a rectifier circuit GS. The inverter WR comprises a switch bridge arrangement which in two branches exhibits in each case a switch SH and SL and exhibits in two branches [lacuna] a capacitor CH and CH'. The output of the inverter WR is formed by the common tie points of the two switches SH, SL, on the one hand, and of the capacitors CH, CH', on the other hand, to which the load circuit LA is connected. The load circuit LA, for its part, comprises the series connection of the inductor L with the parallel connection of the firing capacitor CZ and the fluorescent tube LL. The switches SH and SL are controlled by the radio-frequency oscillation which is not specified and are opened and closed in correspondence with it. In this way, a square-wave AC voltage whose amplitude is determined by the charging capacitor voltages UE which is present at the inverter input is applied to the load circuit in the rhythm of the radio-frequency oscillation.

The rectifier circuit GS exhibits on its input side a rectifier GL for full-wave rectification, whose output terminals are in each case connected via a diode DK or DK' which is polarised in the direction of the rectified AC current, to the charging capacitor CEL which supports the rectified AC supply voltage and at the same time represents the output of the rectifier circuit GS. In order for the inverter WR during operation to pick up a current from the grid which exhibits the required sine form, a sine correction capacitor CS or CS' is provided between the common tie point of a terminal on the output side of the rectifier GL and a diode DK or DK', on the one hand, and the common tie point, the common tie point of the capacitive switch arms of the switch bridge arrangement of the inverter WR given by the capacitors CH, CH' [sic]. Furthermore, the inverter WR exhibits the free-wheeling diodes DFL and DFH which are further requisite for the correct switch operation and which are parallel [lacuna] the switches SL and SH implemented by power transistors.

As has already been pointed out, this known circuit has the property that the inverter WR picks up a constant energy from the grid as long as the switching rate of its switches SH and SL does not change. The result of this is, that the circuit is heavily dependent on changes in the AC supply voltage and/or changes in the load of the load circuit LA. If the AC voltage decreases or the load of the load circuit decreases, the charging capacitor voltage UE consequently increases very quickly beyond an acceptable limiting value, causing safety measures which exhibit the grave operational disadvantages which have already been described.

The known circuit according to Figure 1, which shows a symmetrical construction, can be simplified, without its function being subject to change, by leaving out, on the one hand, the diode DK' and the sine correction capacitor CS'. In a similar way, since the two capacitors CH and CH' are in parallel with each other with respect to their electrical effect, the capacitor CH' can be left out, in conjunction with a doubling of the capacitance value of the capacitor CH, subsequently called the electrically effective bridge capacitor $\overline{CH}$.

Such a simplified inverter circuit is shown by the preferred embodiment of an electronic ballast in accordance with the invention in Figure 2. The circuit of the inverter WR, in contrast to the inverter WR according to Figure 1, is now complemented by the series connection of two clamping diodes DBL and DBH which, being polarised inversely to the charging capacitor voltage at the charging capacitor CEL, are connected in parallel with said capacitor. In this arrangement, their common tie point is at the same time the terminal on the output side of the inverter WR which the load circuit LA and the electrically effective bridge capacitor $\overline{CH}$ have in common. In this arrangement, the electrically effective bridge capacitor $\overline{CH}$ represents the half-bridge capacitor of the switch bridge arrangement.

The clamping diodes DBH and DBL ensure that, if fluctuations of the AC supply voltage and/or changes in

the load of the load circuit LA occur, on the one hand earth GND and on the other hand the intermediate circuit potential UZW and in consequence the charging capacitor voltage US are kept stable as far as possible. It is therefore no longer necessary to switch off the entire device or to paralyse the sine correction function in order to protect against impermissible overvoltages.

The preferred circuit of the electronic ballast according to Figure 2 furthermore differs from the known circuit according to Figure 1 in that a charging inductor LK is provided in the connecting path between the terminal of the rectifier GL on the output side and the common tie point of the diode DK and sine correction capacitor CS, and in that in addition the AC supply voltage un is supplied to the rectifier circuit GS via an harmonic filter FE.

It is expedient for the inductance of the charging inductor LK to be dimensioned for a value at which the charging inductor LK completely reverses its charge in the rhythm of the radio-frequency oscillation for the control of the switches SH and SL only in the case of small values of the instantaneous AC supply current, that is to say in the region of the zero crossings. Figure 3 shows a corresponding timing diagram of the charging inductor current ilk. For this purpose, the inductance of the charging inductor LK has to be selected relatively high. While in the case of a smaller inductance the harmonic component of the supply current can be reduced, a greater outlay, however, is then necessary in the region of the harmonic filter FE in order to meet the demands with regard to a sufficient interference suppression. In the case of the dimensioning, as specified, of the inductance of the charging inductor LK, the radio-frequency current modulation still stays within narrow limits, so that the outlay for the harmonic filter FE as indicated in Figure 2, can be limited to an inductor, which exhibits two windings, and a capacitor.

To complete the picture, it should not pass without mention that the inductance of the charging

inductor LK can be varied in principle within a wide range without the limiter function of the clamping diodes DBH and DBL suffering an impairment as a result.

For an optimal limiter function of the clamping diodes DBH and DBL it is essential that the electrically effective bridge capacitor $\overline{CH}$ has a value at which its charging voltage largely follows the radio-frequency load circuits current. Furthermore, it is expedient to select the capacitance of the sine correction capacitor CS to be substantially larger than the capacitance of the electrically effective bridge capacitor $\overline{CH}$. The capacitance ratio of the sine correction capacitor CS to the electrically effective bridge capacitor $\overline{CH}$ expediently has a value of between 1.5 and 4, preferably the value of 2.

In order to better understand the method of operation of the circuit according to Figure 2, this circuit is again shown in Figures 4 to 7, and this time in conjunction with the most important currents which occur during a supply voltage half-wave as a function of the different switch positions of the switches SL and SH within a cycle of the radio-frequency oscillator oscillation which controls the switches. Such a switching cycle exhibits four switching phases which have to be distinguished from each other. The switching phase 1, where the switch SL is closed and the switch SH is open, is shown in Figure 4. The subsequent second switching phase is shown in Figure 5, where the two switches SH and SL are open. In the third switching phase the switch SL is open and the switch SH is closed, and in the fourth switching phase, shown in Figure 7, both switches SH and SL are open again corresponding to the second switching phase according to Figure 5.

The currents as described in Figures 4-7 are, of course, only meant for a certain instantaneous value of the AC supply voltage u_n . Simply in order to complete the picture, it may be mentioned, that during zero crossing of the AC supply voltage u_n no current flows either via the charging inductor LK or via the sine correction capacitor CS. The operational current for the fluorescent

tube LL in the load circuit is exclusively drawn from the charging capacitor CEL and the bridge capacitor CH.

In all of the Figures 4 to 7, further voltages are entered beside the charging capacitor voltage UE; to be precise, the rectified AC supply voltage UN at the output of the rectifier and the corrected rectified AC supply voltage UK at the common tie point of the charging inductor LK and the diode DK with reference to earth GND have been specified. Furthermore, the bridge capacitor voltage UH at the electrically effective bridge capacitor CH, the sine correction capacitor voltage US at the sine correction capacitor CS, and the inverter voltage UW between the common tie point of the switches SH and SL and earth GND have also been specified.

In the case of the first switching phase shown in Figure 4 it is assumed that at the time the switch SL is closed the intermediate circuit potential UZW is equal the bridge capacitor voltage UH, that the sine correction capacitor CS is uncharged and the electrically effective bridge capacitor $\overline{CH}$, subsequently abbreviated to half-bridge capacitor $\overline{CH}$, is charged. The charging inductor LK is to exhibit a charge and the inductor L of the load circuit is to exhibit no charge.

By closing the switch SL, the half-bridge capacitor $\overline{CH}$ is now discharged by the current i_h via the load circuit and the switch SL. At the same time, the sine correction capacitor CS is charged by the current i_k which also flows through the charging inductor LK and discharges it. The charging inductor LK discharges itself into the sine correction capacitor CS only until the corrected rectified AC supply voltage UK is smaller than the rectified AC supply voltage UN. Subsequently, the charging inductor LK is charged until the half-bridge capacitor CH is fully discharged. The current i_{bl} now flows through the clamping diode DBL, whose circuit is likewise closed via the switch SL. This current ensures that the half-bridge capacitor CH cannot charge itself in the opposite direction. At the same time, the sine correction capacitor CS is further charged via the

charging inductor LK until the corrected rectified AC supply voltage UK is larger than the rectified AC supply voltage UN.

If now the switch SL is opened, as is shown by the second switching phase according to Figure 5, the inductor L of the load circuit which has been charged during the first switching phase is discharged, on the one hand, by means of the clamping diode current i_{bl} which flows through the clamping diode DBL and, on the other hand, by means of the current i_k which flows through the sine correction capacitor CS and in this case makes its way via the free-wheeling diode DFH and also flows through the charging inductor LK, which is now discharged. In this case, the total current which flows through the load circuit and is composed of the clamping diode current i_{bl} and the sine correction capacitor current i_k tends to the value zero.

Corresponding to the third switching phase in accordance with Figure 6, as soon as the switch SH now closes, the half-bridge capacitor $\overline{CH}$ and the inductor L is [sic] charged by means of the bridge capacitor current i_{h2} and the sine correction capacitor current i_{k2} . The sine correction capacitor CS is likewise charged by means of the sine correction capacitor current i_{k2} .

As soon as the half-bridge capacitor $\overline{CH}$ is charged to such an extent, that the sum composed of the sine correction capacitor voltage US and of the bridge capacitor voltage UH is larger than the charging capacitor voltage UE, a third current, specifically the bridge capacitor current i_{h1} , starts to flow.

At the same time the sine correction capacitor current i_{k2} stops flowing and thereby terminates charging of the sine correction capacitor CS.

The diode DK, which becomes conductive as soon as UK + UH [lacuna] UE, effects the flow of the sine correction capacitor current i_{k1} . The sine correction capacitor current i_{k1} and the bridge capacitor current i_{h2} close [sic] via the load circuit and effect further charging of the inductor L. The sine correction capacitor C3 [sic] is

discharged by means of the sine correction capacitor current i_{k1} which now flows. At the same time, the charging inductor LK is also partly discharged.

5 The bridge capacitor current i_{h2} further charges the bridge capacitor $\overline{CH}$. As soon as the bridge capacitor voltage U_H is larger than the charging capacitor voltage U_E , the clamping diode current i_{bh} starts to flow. In this way, the sine correction capacitor CS is prevented from reversing its charge in the opposite direction, that
10 is to say its charge assumes the value zero.

If, corresponding to the fourth switching phase in accordance with Figure 7, the switch SH now again opens, then the inductor L of the load circuit is discharged by means of the clamping diode current i_{bh} , which
15 is still flowing. In this case, the charging inductor LK is partly discharged by means of the charging inductor current i_{lk} , whose circuit is closed by means of the charging capacitor CEL .

Corresponding to the first switching phase in
20 accordance with Figure 4, which has already been explained, a new cycle now starts with the renewed closing of the switch SL .



Patent claims

1. Electronic ballast for fluorescent lamps, having a rectifier circuit (GS) which is fed from an AC supply voltage (un) and has a rectifying bridge (GL), a charging inductor (LK) connected to the positive terminal of said
5 rectifying bridge, and, in series with said inductor, a coupling diode (DK) polarized in the forward direction for the rectified AC supply, as well as a charging capacitor (CEL) in parallel with both their outputs,
10 having a radio-frequency inverter (WR) in a half-bridge arrangement, in which inverter two alternatively controllable switches (SH, SL) are provided arranged between one of the outputs of the rectifier circuit (GS) and a first inverter output, and having at least one load
15 circuit (LA) comprising a fluorescent lamp (LL) with a firing capacitor (CZ) connected in parallel and a lamp inductor (L) connected in series with the fluorescent lamp, the lamp inductor being connected to the first inverter output and the free lamp terminal being con-
20 nected to the second inverter output, characterized in that in the inverter (WR) two series-connected clamping diodes (DBH, DBL) whose common tie point forms a second inverter output are, in addition, connected between the outputs of the rectifier circuit (GS) in a manner
25 inversely polarized relative to the rectified AC supply voltage, and in that in the inverter (WR) a half-bridge capacitor (CH) is, moreover, arranged between the output of the rectifier circuit (GS), which output is at frame potential, and the second inverter output, and in that,
30 finally, there is provided in the inverter (WR) a sine correction capacitor (CS) which is connected, on the one hand, to the tie point of the charging inductor and coupling diode of the rectifier circuit and, on the other hand, to the second inverter output.
35 2. Electronic ballast according to Claim 1, characterized in that the charging inductor (LK) is selected so large that it completely reverses its charge in the rhythm of the radio-frequency switching rate of the inverter (WR) only in the region of the zero crossings of



the AC supply current.

3. Electronic ballast according to one of the preceding claims, characterized in that a harmonic filter (FE) is connected upstream of the rectifier circuit (GS).

5 4. Electronic ballast according to one of the preceding claims, characterized in that the magnitude of the bridge capacitor ($\overline{CH}$) of the inverter (WR) has a value at which its charging voltage largely follows the radio-frequency load circuit current.

10 5. Electronic ballast according to Claim 4, characterized in that the capacitance of the bridge capacitor ($\overline{CH}$) of the inverter (WR) is substantially smaller than the capacitance of the sine correction capacitor (CS).

15 6. Electronic ballast according to Claim 5, characterized in that the capacitance ratio of the sine correction capacitor (CS) to the bridge capacitor ($\overline{CH}$) has a value of between 1.5 and 4, preferably the value of 2.