WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:

a first stack including a first semiconductor substrate;

a plurality of through-silicon vias (TSVs) passing through the first semiconductor substrate;

a second stack on the first stack, the second stack including a second surface facing a first surface of the first stack;

a first pad on the first surface of the first stack, the first pad being in contact with one or more of the plurality of TSVs;

a second pad on the second surface of the second stack;

a bump connecting the first pad and the second pad;

a first redundancy pad on the first surface of the first stack, the first redundancy pad being spaced apart from the first pad and not being in contact with the plurality of TSVs;

a second redundancy pad on the second surface of the second stack, the second redundancy pad being spaced apart from the second pad; and

a redundancy bump connecting the first redundancy pad and the second redundancy pad,

wherein:

the first pad and the first redundancy pad are electrically connected to each other,

the second pad and the second redundancy pad are electrically connected to each other,

wherein the semiconductor package further comprises an interconnection line extending along the first surface of the first stack, and

wherein the interconnection line electrically connects the first pad and the first redundancy pad.

2. The semiconductor package as claimed in claim 1, wherein:

a height of the first pad is greater than a height of the interconnection line, as measured from the first surface of the first stack, and

a height of the first redundancy pad is greater than the height of the interconnection line, as measured from the first surface of the first stack.

3. The semiconductor package as claimed in claim 1 or claim 2, wherein:

the second stack includes a second semiconductor substrate and a semiconductor device layer on the second semiconductor substrate, and

the semiconductor device layer electrically connects the second pad and the second redundancy pad.

4. The semiconductor package as claimed in claim 3, wherein:

the semiconductor device layer includes an inter-line insulating film and lines stacked in the inter-line insulating film, and

a line stacked in the inter-line insulating film that is closest to the second surface is in contact with the second pad and in contact with the second redundancy pad.

5. The semiconductor package as claimed in claim 1, further comprising a second interconnection line extending along the second surface of the second stack,

wherein the second interconnection line electrically connects the second pad and the second redundancy pad.

6. The semiconductor package as claimed in any one of claims 1 to 5, wherein a distance at which the first pad is spaced apart from the first redundancy pad is in a range of 3 μm to 8 μm.

7. The semiconductor package as claimed in any one of claims 1 to 6, wherein a width of the first pad is in a range of 15 μm to 30 μm.

8. A semiconductor package, comprising:

a first stack including a center area and an edge area around the center area, the first stack including a first semiconductor substrate;

a plurality of through-silicon vias (TSVs) passing through the first semiconductor substrate;

one or more first pads on a top surface of the edge area of the first stack, the one or more first pads being in contact with one or more of the plurality of TSVs;

one or more first redundancy pads on the top surface of the edge area of the first stack, the one or more first redundancy pads being spaced apart from the one or more first pads and not being in contact with the plurality of TSVs; and

one or more first interconnection lines extending along the top surface of the edge area of the first stack to electrically connect the one or more first pads and the one or more first redundancy pads.

9. The semiconductor package as claimed in claim 8, wherein:

the one or more first redundancy pads includes a plurality of first redundancy pads, and

a number of the plurality of first redundancy pads electrically connected to one first pad proximate to a center of the first stack in a plan view is less than a number of the plurality of first redundancy pads electrically connected to another first pad distal to a center of the first stack in a plan view.

10. The semiconductor package as claimed in claim 8 or claim 9, wherein:

the first semiconductor substrate includes an edge surface extending in a first direction, and

the one or more first pads and the one or more first redundancy pads are arranged in the first direction.

11. The semiconductor package as claimed in claim 8 or claim 9, wherein:

the first semiconductor substrate includes an edge surface extending in a first direction, and

the one or more first pads and the one or more first redundancy pads are arranged in a second direction intersecting the first direction.

12. The semiconductor package as claimed in claim 11, further comprising:

a second redundancy pad on the top surface of the edge area of the first stack, the second redundancy pad being spaced apart from the one or more first pads and the one or more first redundancy pads and not being in contact with the plurality of TSVs; and

a second interconnection line extending along the top surface of the first stack of the edge area to electrically connect the one or more first pads and the second redundancy pad,

wherein the one or more first pads and the second redundancy pad are arranged in the first direction.

13. The semiconductor package as claimed in claim 12, further comprising:

a third redundancy pad on the top surface of the edge area of the first stack, the third redundancy pad being spaced apart from the one or more first pads, the one or more first redundancy pads, and the second redundancy pad and not being in contact with the plurality of TSVs; and

a third interconnection line extending along the top surface of the first stack of the edge area to electrically connect the one or more first pads and the third redundancy pad,

wherein the one or more first pads and the third redundancy pad are arranged in a third direction different from the first direction and the second direction.

14. The semiconductor package as claimed in claim 8 or claim 9, wherein:

the first semiconductor substrate includes an edge surface extending in a first direction, and

a distance at which the edge area is spaced apart from the edge surface is 200 μm or less.

15. The semiconductor package as claimed in any one of claims 8 to 14, wherein the first interconnection line is in contact with a side surface of the one or more first pads and a side surface of the one or more first redundancy pads.

16. The semiconductor package as claimed in any one of claims 8 to 14, wherein each first pad and each first redundancy pad are in contact with a top surface of the first interconnection line.

17. A semiconductor package, comprising:

a first semiconductor chip including a first semiconductor substrate and a first semiconductor device layer on a bottom surface of the first semiconductor substrate;

a second semiconductor chip including a second semiconductor substrate and a second semiconductor device layer on a bottom surface of the second semiconductor substrate, on the first semiconductor chip;

a plurality of first through-silicon vias (TSVs) passing through the first semiconductor substrate;

a first pad on a top surface of the first semiconductor substrate, the first pad being in contact with one or more of the plurality of first TSVs;

a second pad on a bottom surface of the second semiconductor device layer;

a bump connecting the first pad and the second pad;

a first redundancy pad on the top surface of the first semiconductor substrate, the first redundancy pad being spaced apart from the first pad and not being in contact with the plurality of first TSVs;

an interconnection line extending along the top surface of the first semiconductor substrate and connecting the first pad and the first redundancy pad;

a second redundancy pad on the bottom surface of the second semiconductor device layer, the second redundancy pad being spaced apart from the second pad; and

a redundancy bump connecting the first redundancy pad and the second redundancy pad,

wherein the second semiconductor device layer electrically connects the second pad and the second redundancy pad.

18. The semiconductor package as claimed in claim 17, wherein:

the first semiconductor chip further includes a protective layer covering the top surface of the first semiconductor substrate, and

the plurality of first TSVs pass through the protective layer.

19. The semiconductor package as claimed in claim 17 or claim 18, further comprising a filler layer that is filled in a space between the first semiconductor chip and the second semiconductor chip.