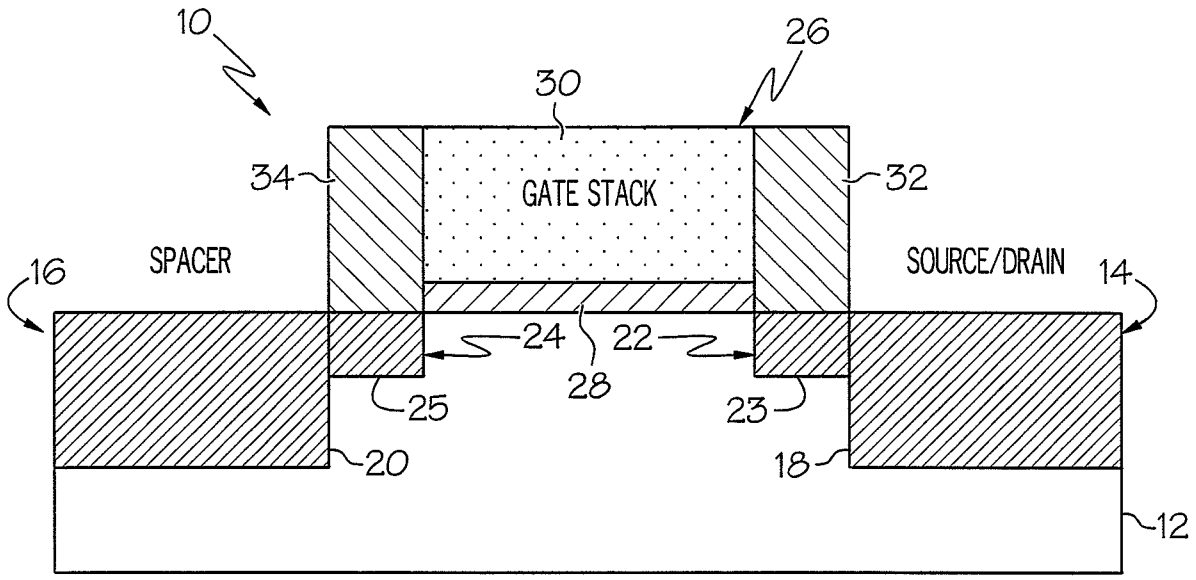

10
26
30
34
GATE STACK
32
SPACER
SOURCE/DRAIN
16
14
24
22
28
25
23
20
18
12

FIG. 1

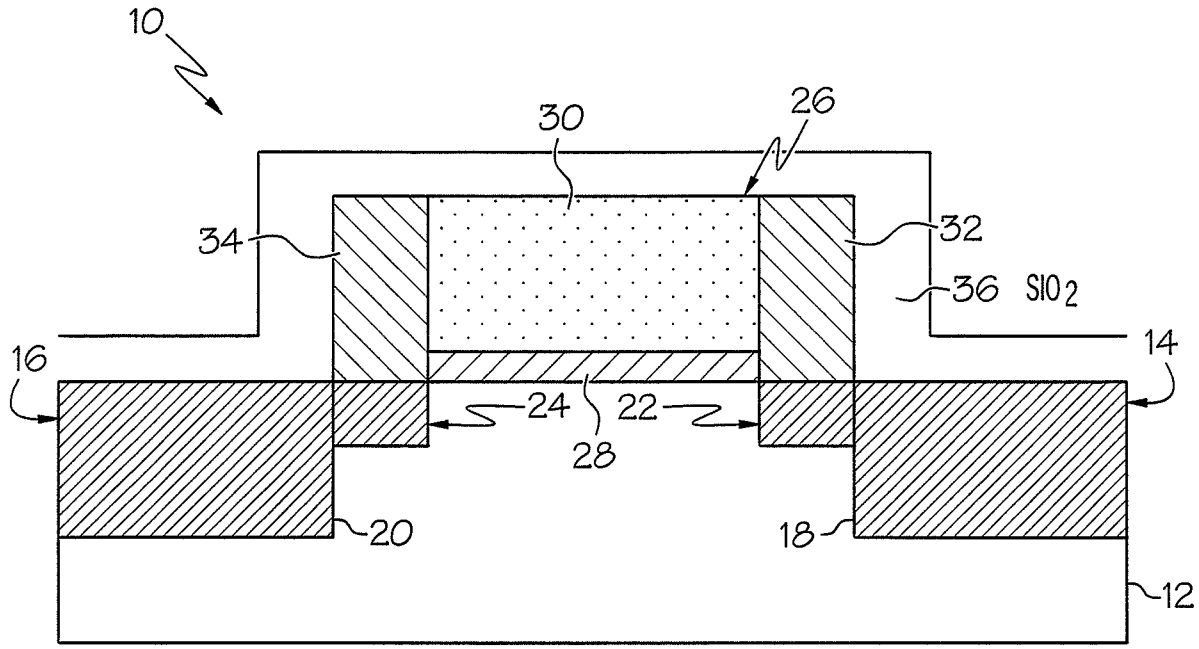

10
30
26
34
32
36
SiO_2
16
14
24
22
28
20
18
12

FIG. 2

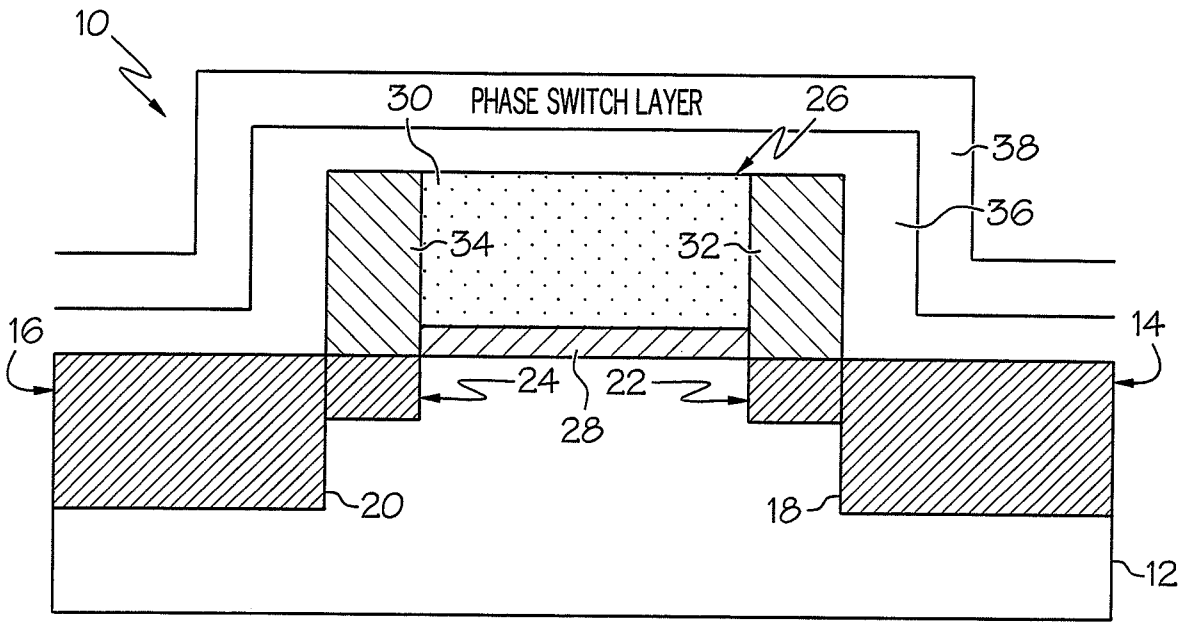

10
30
PHASE SWITCH LAYER
26
38
36
34
32
16
14
24
22
28
20
18
12

FIG. 3

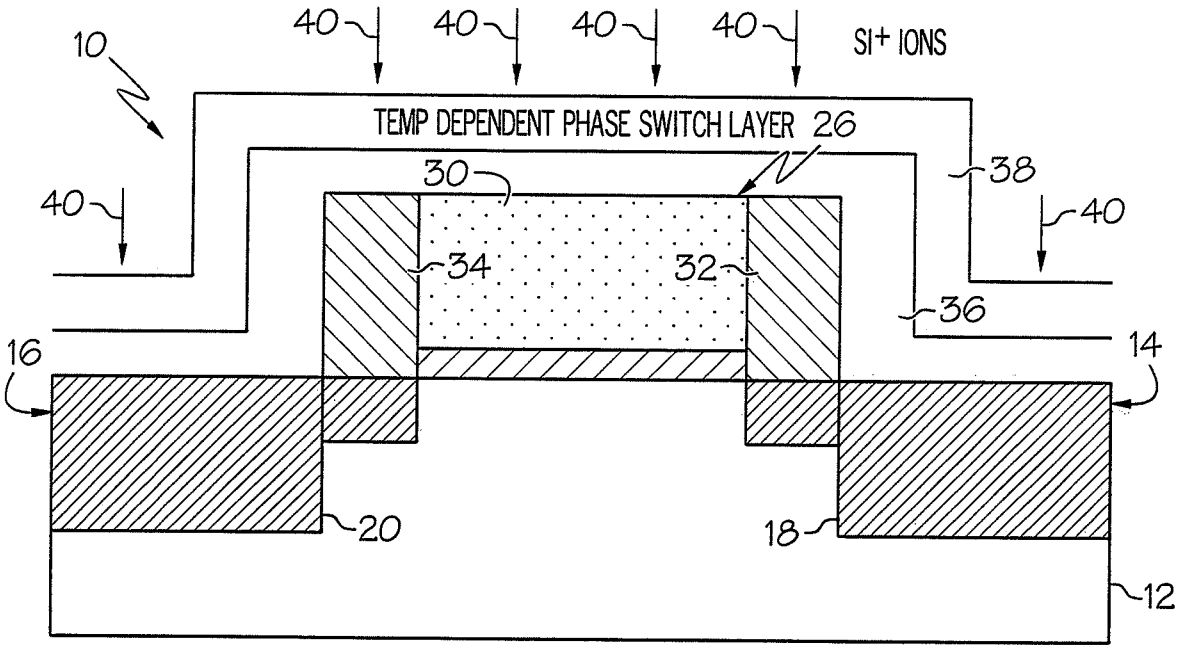

40
40
40
40
SI+ IONS
10
TEMP DEPENDENT PHASE SWITCH LAYER 26
30
38
40
40
34
32
36
16
14
20
18
12

FIG. 4

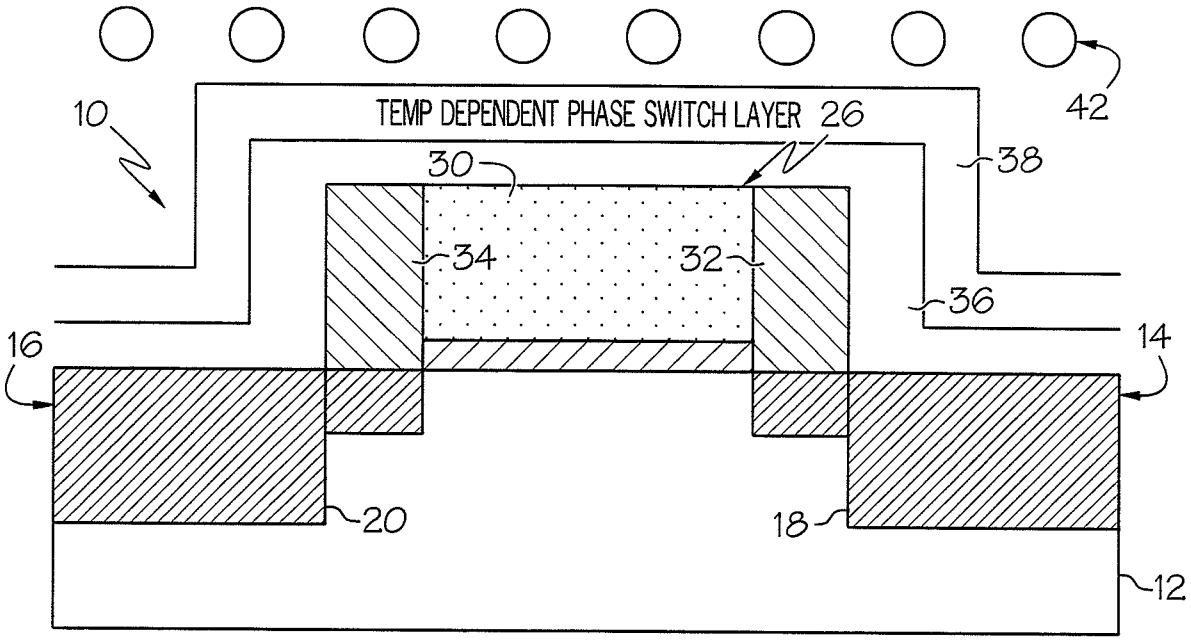

10
TEMP DEPENDENT PHASE SWITCH LAYER 26
42
38
30
34
32
36
16
14
20
18
12

FIG. 5

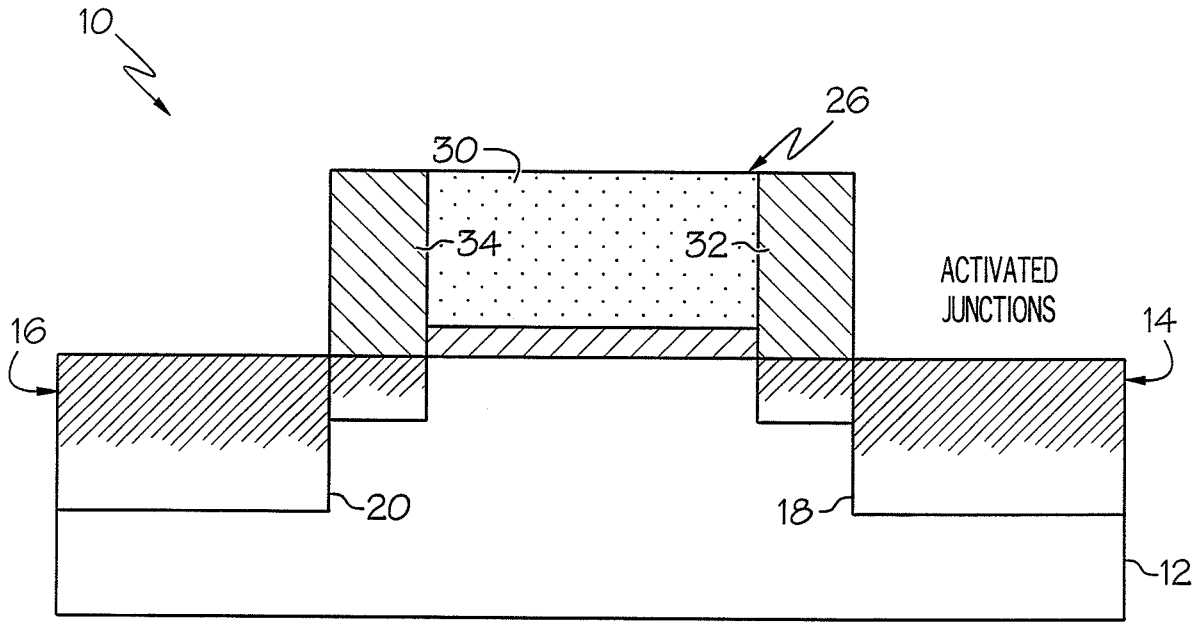

10
26
30
34
32
ACTIVATED
JUNCTIONS
16
14
20
18
12

FIG. 6

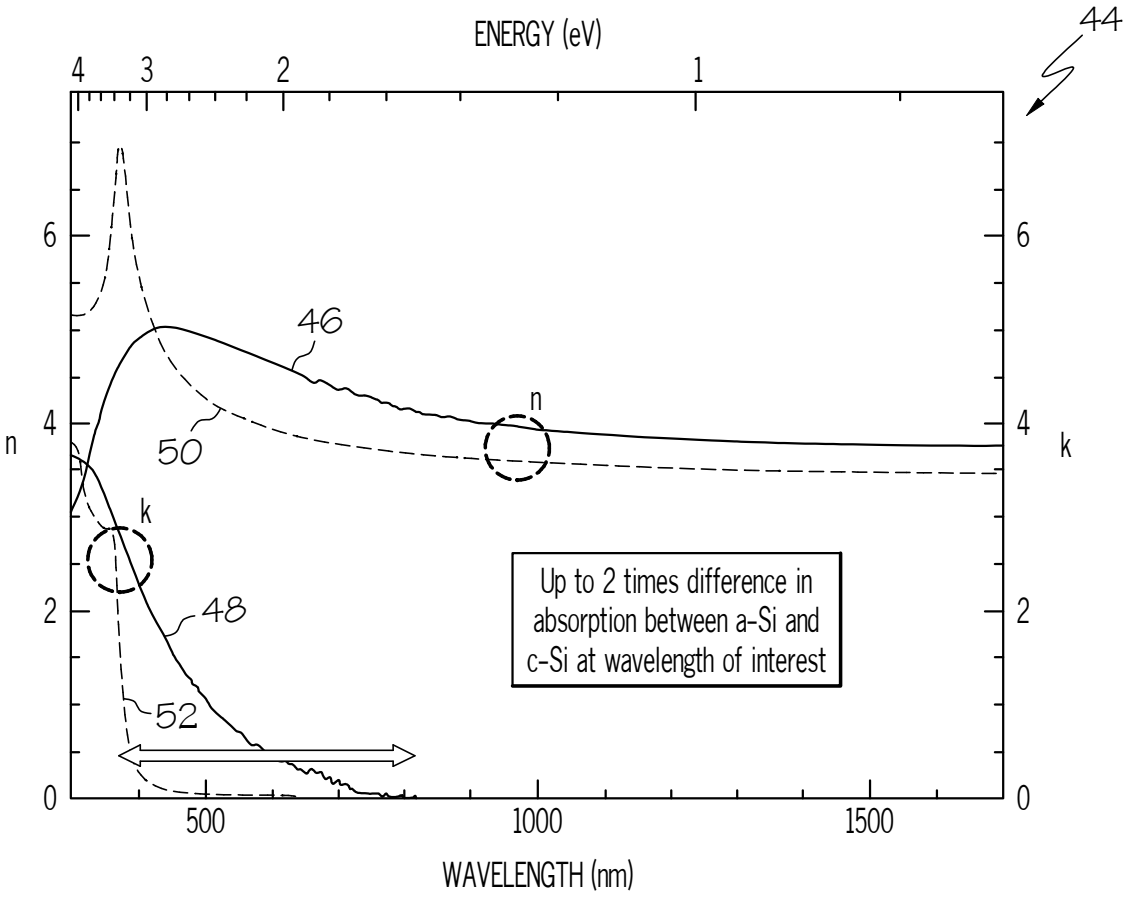

ENERGY (eV)
4
3
2
1
44
6
4
2
0
n
k
46
50
48
52
n
k
Up to 2 times difference in absorption between a-Si and c-Si at wavelength of interest
500
1000
1500
WAVELENGTH (nm)

FIG. 7

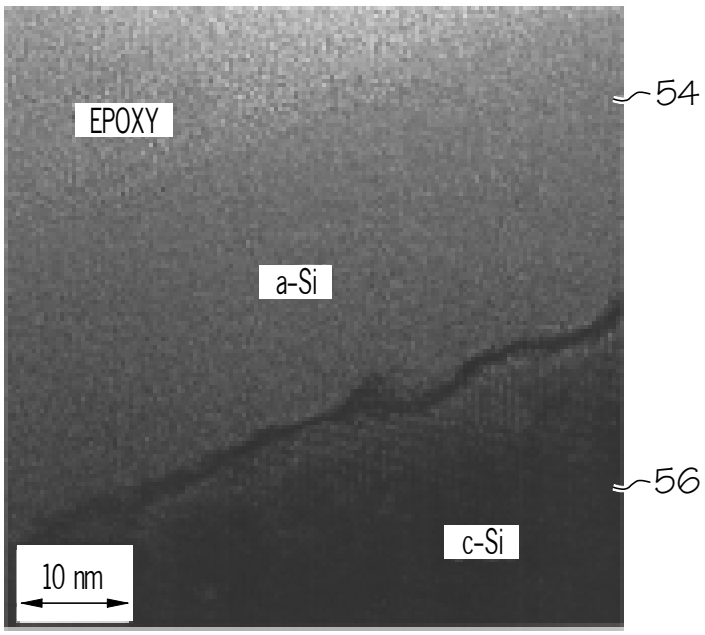

EPOXY
54
a-Si
56
c-Si
10 nm

FIG. 8

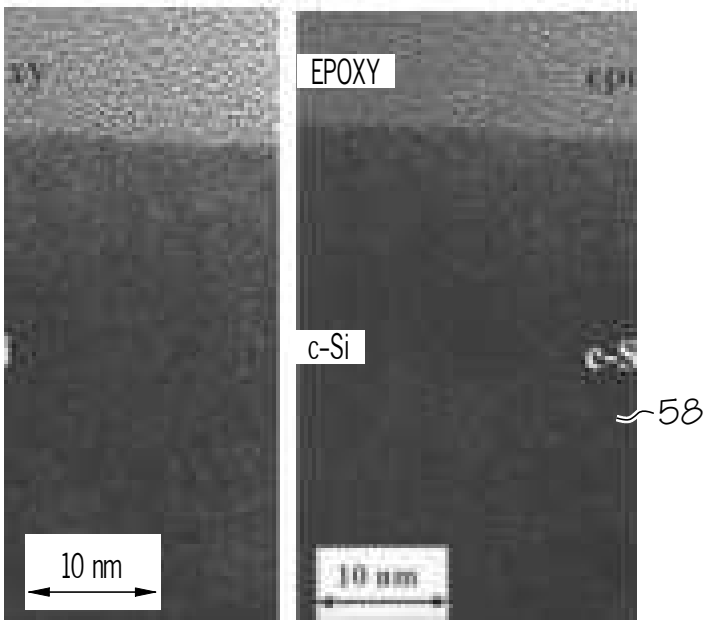

EPOXY
c-Si
58
10 nm
10 nm

FIG. 9

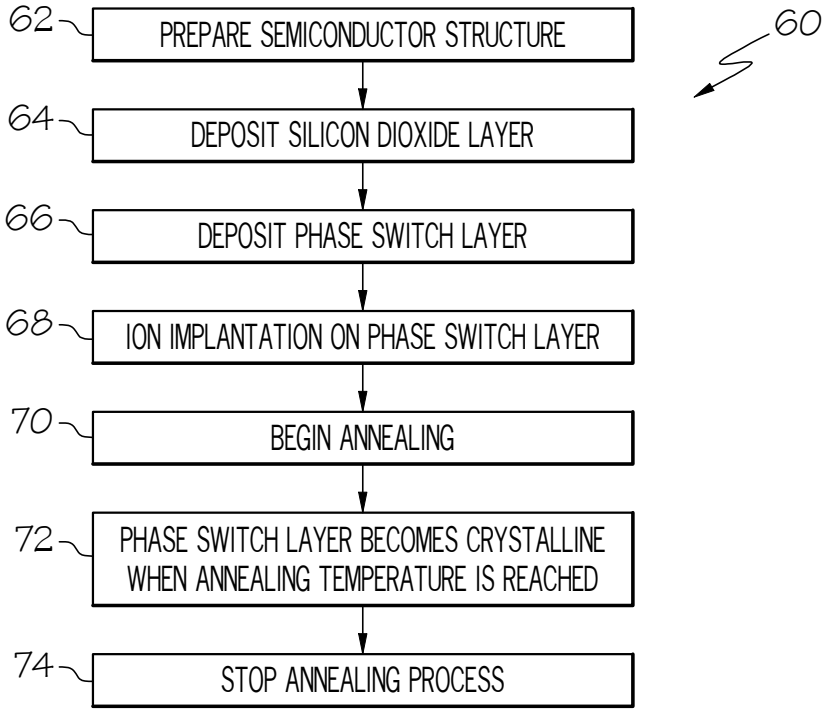

62
PREPARE SEMICONDUCTOR STRUCTURE
60
64
DEPOSIT SILICON DIOXIDE LAYER
66
DEPOSIT PHASE SWITCH LAYER
68
ION IMPLANTATION ON PHASE SWITCH LAYER
70
BEGIN ANNEALING
72
PHASE SWITCH LAYER BECOMES CRYSTALLINE WHEN ANNEALING TEMPERATURE IS REACHED
74
STOP ANNEALING PROCESS

FIG. 10