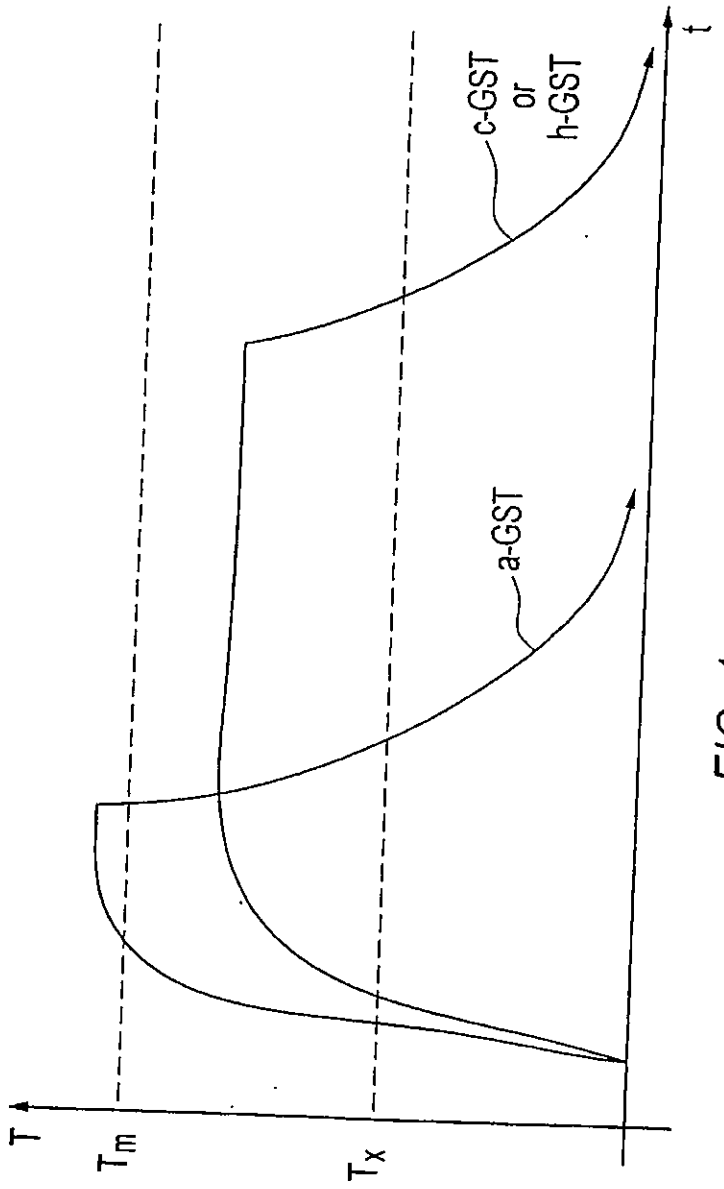


FIG. 1 (PRIOR ART)

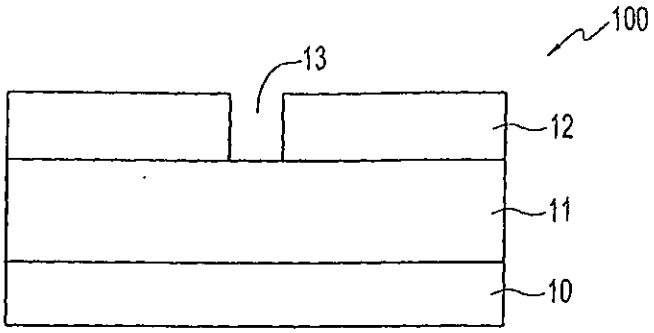


FIG. 2

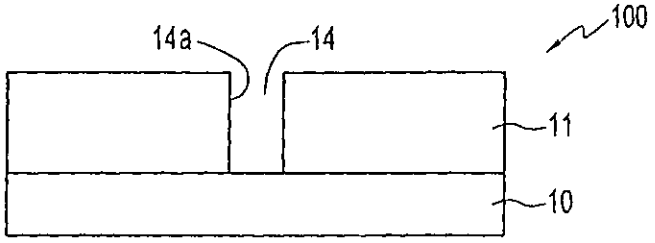


FIG. 3

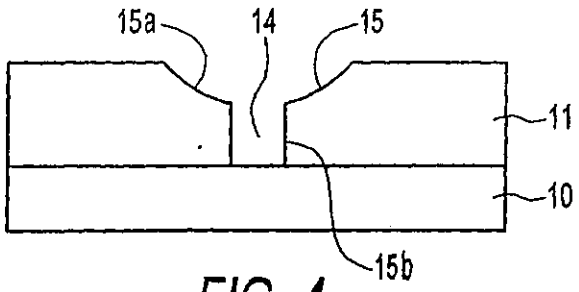


FIG. 4

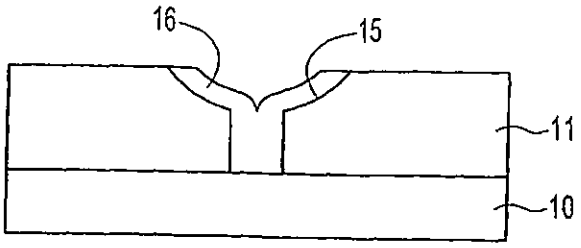


FIG. 5

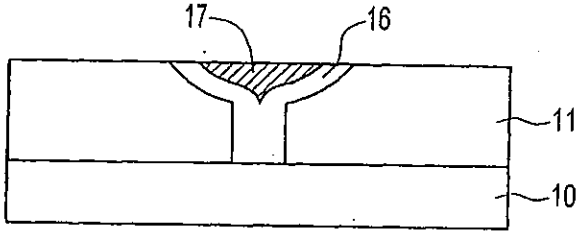


FIG. 6

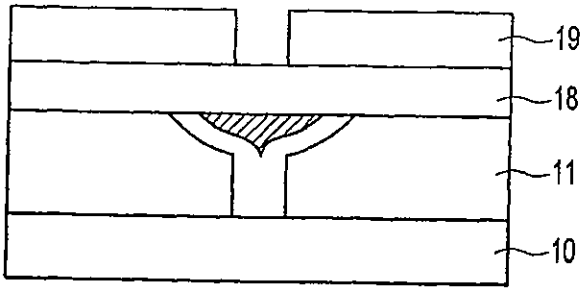


FIG. 7

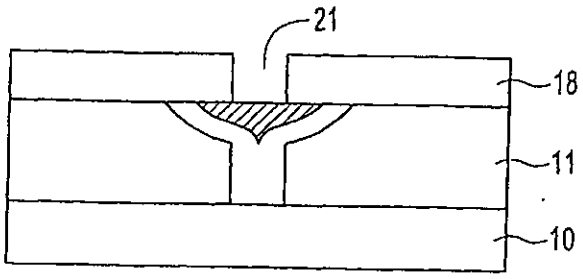


FIG. 8

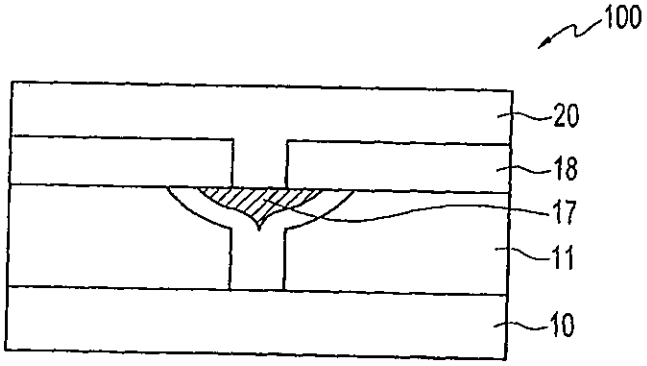


FIG. 9

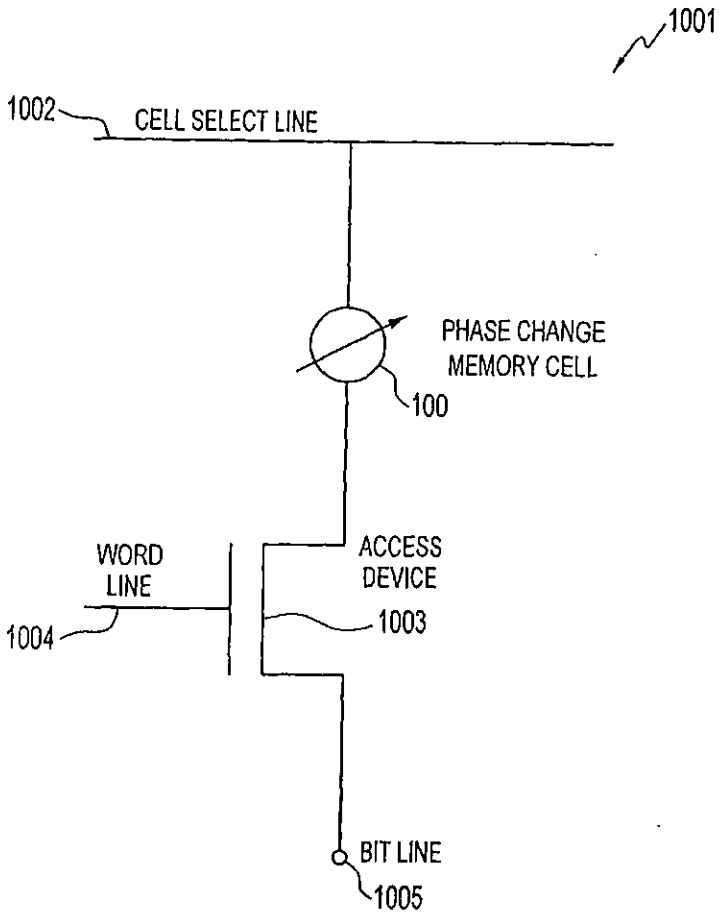

1001
1002
CELL SELECT LINE
PHASE CHANGE
MEMORY CELL
100
WORD
LINE
1004
ACCESS
DEVICE
1003
BIT LINE
1005

FIG. 10

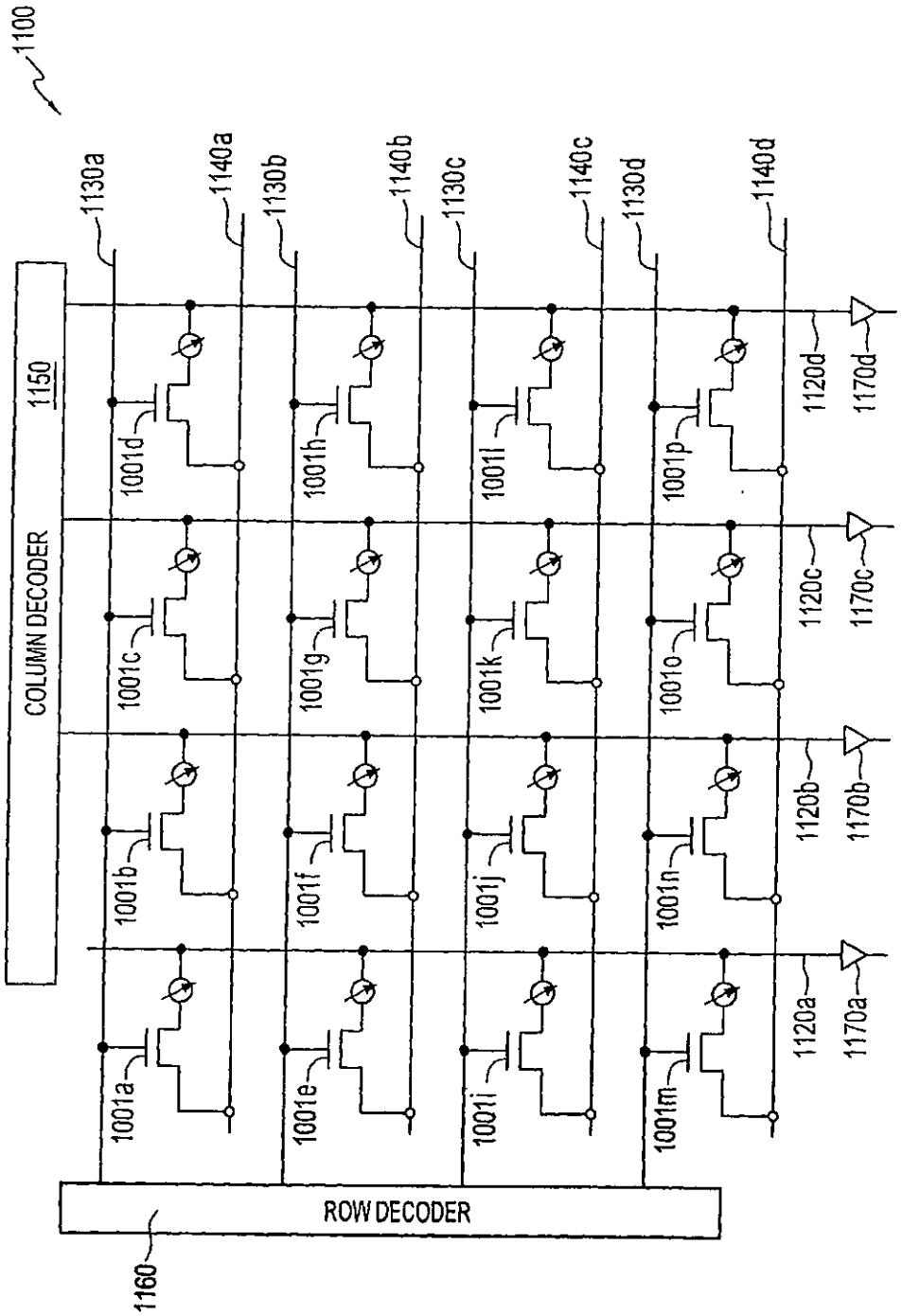

1100
1130a
1140a
1130b
1140b
1130c
1140c
1130d
1140d
COLUMN DECODER
1150
1001d
1001h
1001l
1001p
1120d
1170d
1001c
1001g
1001k
1001o
1120c
1170c
1001b
1001f
1001j
1001n
1120b
1170b
1001a
1001e
1001i
1001m
1120a
1170a
ROW DECODER
1160

FIG. 11

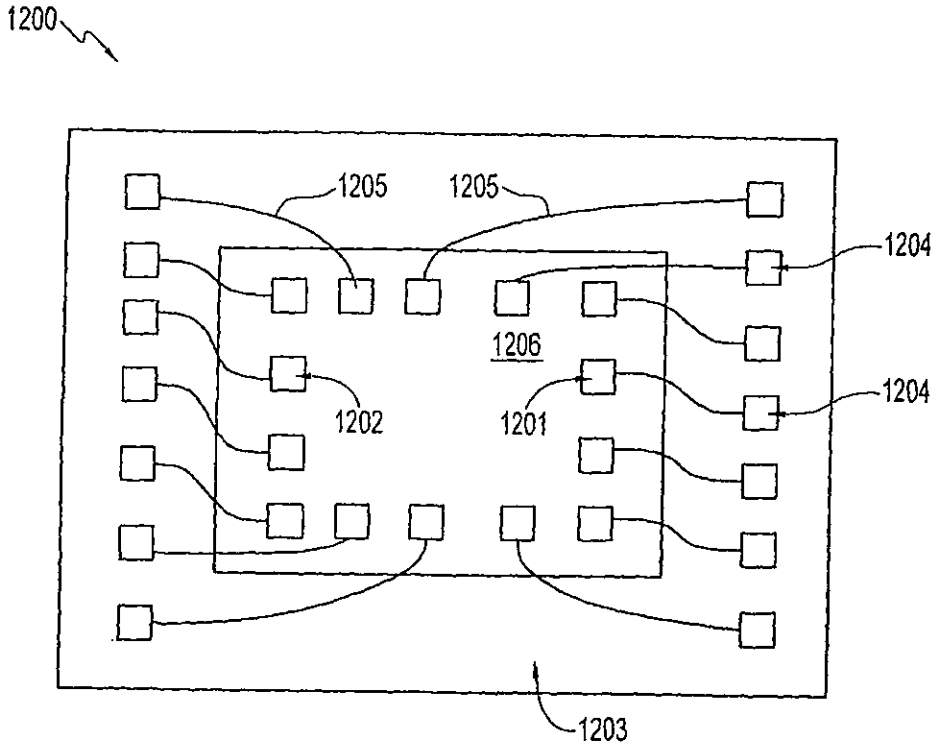


FIG. 12

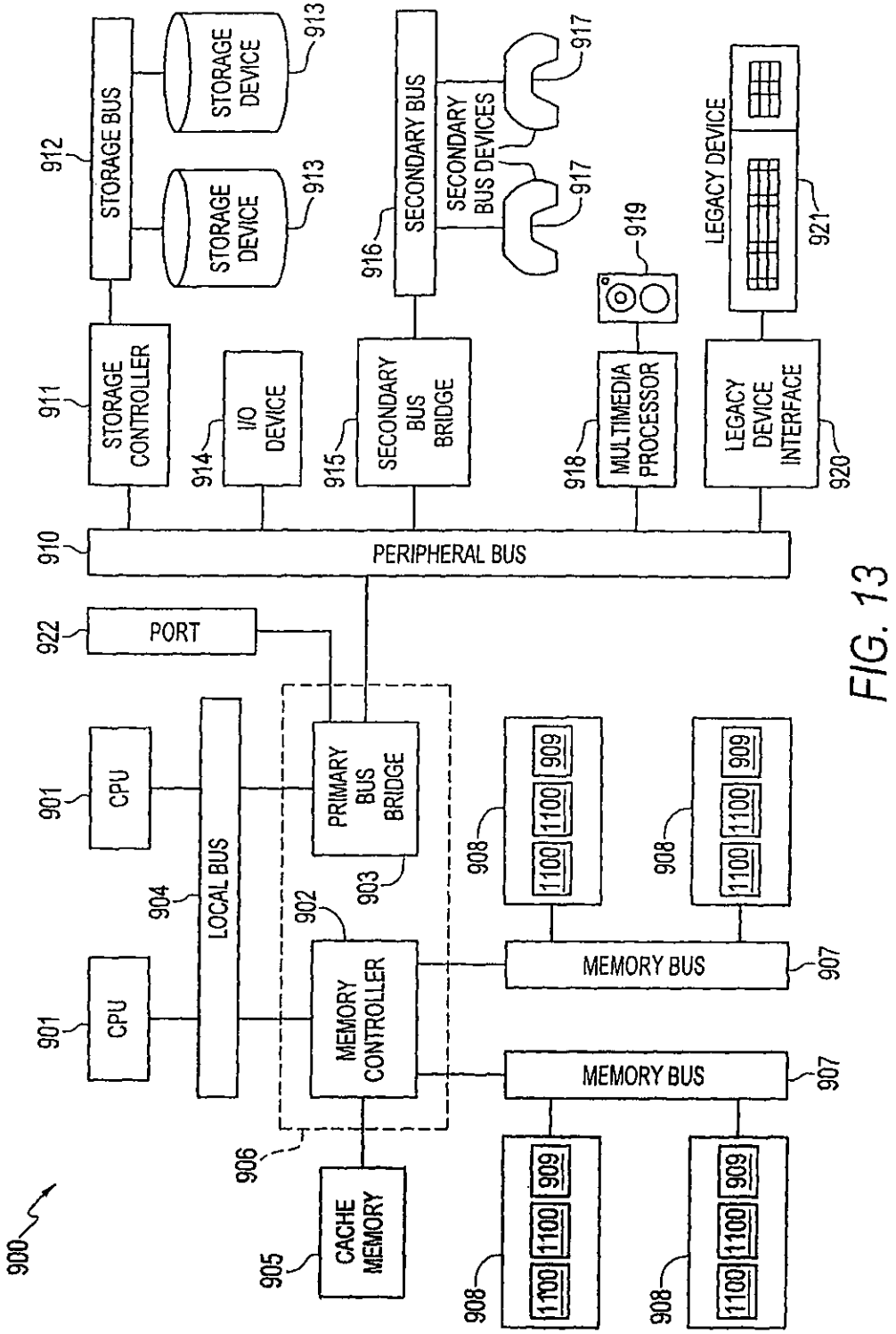

900
912
STORAGE BUS
STORAGE DEVICE
913
STORAGE DEVICE
913
916
SECONDARY BUS
SECONDARY BUS DEVICES
917
917
919
LEGACY DEVICE
921
911
STORAGE CONTROLLER
914
I/O DEVICE
915
SECONDARY BUS BRIDGE
918
MULTIMEDIA PROCESSOR
LEGACY DEVICE INTERFACE
920
910
PERIPHERAL BUS
922
PORT
901
CPU
904
LOCAL BUS
PRIMARY BUS BRIDGE
903
902
908
1100
909
908
1100
909
901
CPU
MEMORY CONTROLLER
MEMORY BUS
907
MEMORY BUS
907
906
905
CACHE MEMORY
908
1100
909
908
1100
909

FIG. 13