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Modulo addressingBACKGROUND

Digital signal processors (DSP) often include
5 specialized hardware for supporting digital signal
processing functions, such as the fast fourier transform
(FFT). For example, many DSP's include modulo addressing
registers and other hardware support for accessing data
structures, such as circular buffers, necessary for
10 manipulating and processing data.

DESCRIPTION OF DRAWINGS

Figure 1 is a block diagram illustrating an example of
a programmable processor adapted to support modulo
15 addressing according to the invention.

Figure 2 is a block diagram illustrating an example
modulo addressing unit of the programmable processor.

Figure 3 is an example mode of operation of the modulo
addressing unit.

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DETAILED DESCRIPTION

Figure 1 is a block diagram of an example system 2
having a processor 5 coupled of a memory device 7.

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Processor 5 includes modulo addressing unit 4 that, as described below, comprises specialized hardware to support efficient modulo address calculations. Software applications 8 comprise machine instructions that, when executed by processor 5, create and maintain data structures for processing data, such as circular buffer 6. Memory 7 stores circular buffer 6, typically in linear fashion over a range of memory addresses from a starting memory address to an ending memory address. Memory device 7 may comprise different memory technologies, such as FLASH memory, static random access memory (SRAM) or dynamic random access memory (DRAM).

In response to the machine instructions issued by software applications 8, modulo addressing unit 4 calculates the appropriate memory addresses necessary to interact with circular buffer 6 in order to store and retrieve data. The memory address range of circular buffer 6 can be defined in a number of ways. For example, as used for exemplary purposes below, the memory address range can be defined in terms of a base address (B) and a length (L). Alternatively, the range may be defined in terms of a base address (b) and an ending address.

While software applications 8 are accessing circular buffer 6, modulo addressing unit 4 is responsible for calculating the correct memory address of the data. In addition, modulo addressing unit 4 includes detection logic to determine whether an address falls outside the memory address range of circular buffer 6. In such circumstances, as described below, modulo addressing unit 4 "wraps" the memory address to a corresponding memory address within the address range of circular buffer 6.

One technique used in conventional systems to wrap an address into circular buffer 6, is to detect an out of range condition upon incrementing the target address past the end of the circular buffer 6 such that the target address falls within memory region 7A. At this time, the target address can be wrapped back into an acceptable address by subtracting the length of the buffer from the target address. Similarly, when the modifier (M) is a negative number, such that the circular buffer 6 is traversed from the ending address toward the starting address, an out-of-range condition is detected when the target address falls below the starting address of the circular buffer within memory region 7A. In this situation, the target address can be wrapped back into the

circular buffer by adding the length of the circular buffer to the target address. Many of the conventional techniques examine the sign of the modifier to determine the direction in which the circular buffer 6 is being traversed before
5 calculating a corrected target address. As described below, modulo addressing unit 4 supports range checking and address generation independent from the direction in which circular buffer is being traversed.

Figure 2 is a block diagram illustrating one
10 embodiment of modulo addressing unit 4 that may calculate a final target memory address 16 for each access of circular buffer 6 within memory device 7. Modulo addressing unit 4 may includes a number of modulo registers 20 such as a base address register 21 and a length register 27 for storing
15 the base address and length of circular buffer 6, respectively. In addition, modulo addressing unit 4 may include index register 23 for storing an index address (I), which points to a current location within circular buffer 6. Modifier register 25 may store a modifier value (M)
20 used as to increment or decrement the index address I for each access of circular buffer 6. For example, after accessing a first data value at memory address I within circular buffer 6, the next data value accessed may

typically be address $I + M$, where M can either be a positive or negative integer.

In order to ensure that the target address falls within the memory address range of circular buffer 6 without testing the sign of the modifier (M), modulo addressing unit 4 includes three adders, 12A, 12B and 12C that calculate three possible target addresses in parallel. Adder 12A receives the index value (I) and the modifier value (M) and outputs a first target address 14A equal to $I + M$. Adder 12B receives the index value (I), the modifier value (M) and the length of the buffer (L) and outputs a second target address 14B equal to $I + M + L$. Adder 12C receives I , M and L and outputs a third possible target address 14C equal to $I + M - L$. In this manner, target addresses 14A, 14B and 14C represent: (1) an uncorrected target address, (2) a corrected target address for use when the uncorrected target address falls below the acceptable address range, and (3) a corrected target address for use when the uncorrected target address falls above the acceptable address range, respectively.

In parallel to the computation of the possible target addresses 14, comparator 17 receives the index address (I), the modifier value (M), the buffer length (L) and the base

address (B). Based on the inputs, asserts selection signals 19 to cause multiplexer 20 to select one of the three possible target address 14A, 14B and 14C as the final target address 16. More specifically, comparator 17 is
5 adapted to assert selection signals 19 to select an appropriate target address 14 in based on whether the target address falls outside of the acceptable range of addresses and, therefore, must be corrected. Notably, comparator 17 need not determine the sign of the modifier
10 in selecting an appropriate target address 14. Because modulo addressing unit 4 includes a plurality of adders 12 that calculate an uncorrected target address and two corrected target addresses, comparator 17 need not determine the direction in which circular buffer 6 is being
15 traversed. In this manner, comparator may select the appropriate target address 14 independently from the sign of the modifier. In one embodiment, selection signals 19 comprise two signals defining four states for selecting one of the three possible target addresses 14 provided by
20 adders 12, as illustrated in the following table:

Selection Signals	Condition	Destination Address
00	$B \leq I + M < B + L$	$I + M$ (14A)
01	$I + M < B$	$I + M + L$ (14B)
10	$I + M \geq B + L$	$I + M - L$ (14C)
11	--	--

Table 1

Figure 3 is a flowchart illustrating an example mode of operation 30 of modulo addressing unit 4 for calculating and selecting a target address within circular buffer 6 independently from the direction in which the circular buffer 6 is being traversed. Although illustrated sequentially, many of the operations may occur in parallel, as described above.

First, modulo addressing unit 4 of processor 5 calculates three possible target addresses: (1) $I + M$, (2) $I + M + L$ and (3) $I + M - L$ (31). As described above, the second and third possible target addresses are calculated to wrap the target address back into an circular buffer 6 in the event the target address is below the starting address or above the ending address, respectively.

In parallel with the address calculation, modulo addressing unit 4 determines whether the target address falls outside the acceptable address range and, therefore, needs correction. More specifically, modulo addressing unit 4 determines whether $I + M$ is $< B$, i.e. whether the target address falls below the address range of circular buffer 6 (32). If so, multiplexer 10 selects target address #2 as provided by adder 12B (35). If not, modulo addressing unit 4 determines whether the target address falls beyond the upper end of circular buffer 6 (33) and, if so, selects target address #3 as provided by adder 12C (36). If not, modulo addressing unit 4 selects the target address #1 as supplied by adder 12A, which falls within the acceptable address range of circular buffer 6 and may not be corrected (34).

Various embodiments of the invention have been described. The processor described above may be implemented in a variety of systems including general purpose computing systems, digital processing systems, laptop computers, personal digital assistants (PDA's) and cellular phones. In such a system, the processor may be coupled to a memory device, such as a Flash memory device or a static random access memory (SRAM), that stores an

operating system and other software applications. These and other embodiments are within the scope of the following claims.

What is claimed is:

- 1 1. An apparatus comprising:
 - 2 a plurality of adders to concurrently output an
 - 3 uncorrected target modulo address as a function of an index
 - 4 address and a modifier value and at least one corrected
 - 5 target modulo address as a function of the index address,
 - 6 the modifier value and a length value; and
 - 7 a comparator to select one of the target modulo
 - 8 addresses independent from a sign of the modifier value.

- 1 2. The apparatus of claim 1, wherein the plurality of
 - 2 adders comprise:
 - 3 a first adder adapted to output a first target modulo
 - 4 address equal to the index address plus the modifier value;
 - 5 a second adder adapted to output a second target
 - 6 modulo address equal to the index address plus the modifier
 - 7 value plus a length value; and
 - 8 a third adder adapted to output a third target modulo
 - 9 address equal to the index address plus the modifier value
 - 10 minus a length value.

- 1 3 The apparatus of claim 2, further comprising:
 - 2 an index register to store the index address;

3 a modifier register to store the modifier value; and
4 a length register to store the length value.

1 4. The apparatus of claim 1, further comprising a
2 multiplexer to select one of the target modulo addresses.

1 5. The apparatus of claim 4 further comprising a
2 comparator adapted to output a plurality of selection
3 signals to control the multiplexer.

1 6. The apparatus of claim 5, wherein the comparator
2 asserts the selection signals as a function of a base
3 address (b) for a circular buffer, a length (L) of the
4 circular buffer, an index address (I) and a modifier value
5 (M).

1 7. The apparatus of claim 6, wherein the comparator
2 asserts the selection signals to a first state when $I+M < B$,
3 a second state when $I+M \geq B+L$ and a third state when $B \leq$
4 $I+M < B+L$.

1 8. A method comprising:

2 concurrently generating an uncorrected target modulo
3 address as a function of an index address and a modifier
4 value and at least one corrected target modulo address in
5 parallel address as a function of the index address, the
6 modifier value and a length value; and
7 selecting one of the target modulo addresses
8 independently from a sign of the modifier value.

1 9. The method of claim 8, wherein generating the target
2 module addresses comprises:

3 generating first a target modulo address equal to the
4 index address plus the modifier value;

5 generating a second target modulo address equal to the
6 index address plus the modifier value plus the length
7 value; and

8 generating a third target modulo address equal to the
9 index address plus the modifier value minus the length
10 value.

1 10. The method of claim 9 further comprising:
2 storing the index address, the modifier value and the
3 length value in modulo registers.

1 11. The method of claim 8, wherein selecting one of the
2 target modulo addresses comprises selecting the target
3 modulo address as a function of a base address (b) for a
4 circular buffer, a length (L) of the circular buffer, an
5 index address (I) and a modifier value (M).

1 12. The method of claim 11, wherein selecting one of the
2 target modulo addresses comprises:
3 selecting a first target modulo address when $I+M < B$;
4 selecting a second target modulo address when
5 $I+M \geq B+L$; and
6 selecting a third target modulo address when $B \leq I+M$
7 $< B+L$.

1 13. A system comprising:
2 a Flash memory device; and
3 a processor including an modulo addressing unit
4 comprising:
5 a plurality of adders to concurrently output an
6 uncorrected target modulo address as a function of an index
7 address and a modifier value and at least one corrected
8 target modulo address as a function of the index address,
9 the modifier value and a length value; and

10 a comparator to select one of the target modulo
11 addresses independent from a sign of the modifier value.

1 14. The system of claim 13, wherein the modulo addressing
2 unit comprises a comparator to select one of the target
3 modulo addresses.

1 15. The system of claim 13, wherein the plurality of adders
2 comprise:

3 a first adder adapted to output a first target modulo
4 address equal to the index address plus the modifier value;

5 a second adder adapted to output a second target
6 modulo address equal to the index address plus the modifier
7 value plus the length value; and

8 a second adder adapted to output a third target modulo
9 address equal to the index address plus the modifier value
10 minus the length value.

1 16. The system of claim 15, the modulo addressing unit
2 further comprises:

3 an index register to store the index address;

4 a modifier register to store the modifier value; and

5 a length register to store the length value.

1 17. The system of claim 13, wherein the modulo addressing
2 unit further comprises a multiplexer to select one of the
3 target modulo addresses.

1 18. The system of claim 17, wherein the modulo addressing
2 unit further comprises a comparator adapted to output a
3 plurality of selection signals to control the multiplexer.

1 19. The system of claim 18, wherein the comparator asserts
2 the selection signals as a function of a base address (b)
3 for a circular buffer, a length (L) of the circular buffer,
4 an index address (I) and a modifier value (M).

1 20. The system of claim 19, wherein the comparator asserts
2 the selection signals in a first state when $I+M < B$, a
3 second state when $I+M \geq B+L$ and a third state when $B \leq I+M$
4 $< B+L$.