CLAIMS

What is claimed is:

1. A test circuit for applying current pulses to a device under test (DUT), the test circuit comprising:

a first multiplexer configured to output analog voltage pulses, the first multiplexer configured to generate both bipolar and unipolar voltage pulses; and

at least one operational amplifier and resistor configured to receive the voltage pulses from the first multiplexer and convert the voltage pulses to current pulses, wherein an operational amplifier is configured to output current pulses, wherein the current pulses are bipolar or unipolar current pulses depending on whether the at least one operational amplifier and resistor receive bipolar or unipolar voltage pulses.

2. The test circuit of Claim 1, further comprising a charge booster circuit configured to minimize overshoots and undershoots during transitions between current levels, wherein the charge booster circuit comprises at least one operational amplifier and a plurality of resistors.

3. The test circuit of Claim 2, further comprising a second multiplexer, wherein the charge booster circuit is configured to receive voltage pulses from the second multiplexer, wherein the voltage pulses from the second multiplexer are synchronized with but independent from the voltage pulses received from the first multiplexer and the charge booster circuit delivers its output to the DUT, wherein the DUT is positioned between ground and the output of the current pulses.

4. The test circuit of Claim 3, wherein the first and second multiplexers have the same input select lines.

5. The test circuit of Claim 1, wherein the first multiplexer has one less input select line than voltage levels provided to its input terminals.

6. The test circuit of Claim 5, wherein the first multiplexer has three voltage levels provided to four input terminals.

7. The test circuit of Claim 6, wherein an intermediate voltage level is selected with a transitional address for an input select combination of the first multiplexer, wherein the input select combination comprises address values assigned to the input select lines.

8. The test circuit of Claim 5, wherein only one input select address line changes during a transition from highest voltage to intermediate voltage or from lowest voltage to intermediate voltage.

9. The test circuit of Claim 1, wherein the multiplexer generates an analog signal from discrete voltages.

10. The test circuit of Claim 1, wherein at least two operational amplifiers and five resistors receive the voltage pulses from the first multiplexer and convert the voltage pulses to current pulses.

11. A method of providing a pulsed current to a device under test (DUT), the method comprising:

providing a first multiplexer having a plurality of input terminals;

providing a plurality of different voltage levels to the plurality of input terminals of the first multiplexer;

generating voltage pulses from a selected voltage level by using input select combination of input select lines of the first multiplexer to determine which of the input terminals of the first multiplexer is connected to an output of the first multiplexer, wherein input select combination of the first multiplexer is performed by assigning address values to input select lines of the first multiplexer in a way such that any transitional address value leads to a monotonic change of the output of the first multiplexer, wherein the output of the first multiplexer comprises voltage pulses; and

converting the voltage pulses to current pulses using a plurality of resistors, operational amplifiers, and capacitors.

12. The method of Claim 11, wherein converting further comprises:

using a charge booster circuit to minimize overshoots and undershoots, the charge booster circuit comprising an operational amplifier, a plurality of resistors, and a capacitor.

13. The method of Claim 12, wherein using the charge booster circuit comprises providing a second multiplexer that receives a plurality of voltage levels independent from the voltage levels provided to the first multiplexer.

14. The method of Claim 13, wherein using the charge booster circuit further comprises allowing a charge stored in the capacitor to stabilize such that current flows only through resistors.

15. A single circuit capable of providing both unipolar and bipolar current pulses, the circuit comprising:

a muiltiplexer configured to receive at least one positive voltage signal and at least one negative voltage signal, wherein the multiplexer is configured to generate both bipolar and unipolar voltage pulses from the voltage signals it receives; and

at least one operational amplifier and resistor configured to receive the voltage pulses from the multiplexer and convert the voltage pulses to current pulses, wherein an operational amplifier is configured to output bipolar or unipolar current pulses depending on whether the at least one operational amplifier and resistor receive bipolar or unipolar voltage pulses.

16. The circuit of Claim 15, wherein at least two operational amplifiers and five resistors that receive the voltage pulses from the multiplexer and convert the voltage pulses to current pulses.

17. A test circuit for applying current pulses to a device under test (DUT), the test circuit comprising:

a first multiplexer configured to output analog voltage pulses, the first multiplexer configured to generate both bipolar and unipolar voltage pulses;

at least one operational amplifier and resistor configured to receive the voltage pulses from the first multiplexer and convert the voltage pulses to current pulses, wherein an operational amplifier is configured to output current pulses, wherein the current pulses are bipolar or unipolar current pulses depending on whether the at least one operational amplifier and resistor receive bipolar or unipolar voltage pulses; and

a charge booster circuit configured to minimize overshoots and undershoots during transitions between current levels, wherein the charge booster circuit comprises at least one operational amplifier, a plurality of resistors, and a capacitor.

18. The test circuit of Claim 17, wherein the charge booster circuit further comprises a second multiplexer receives a voltage signal and outputs voltage pulses, wherein the first and second multiplexers have the same input select lines.

19. The test circuit of Claim 17, wherein the output of the charge booster circuit is delivered to the DUT.