[0015] FIG. 7 is a diagram showing the defect bands shown in FIG. 5 and showing radial defect bands for no nitrogen doping and with nitrogen doping for variation of the radial defect bands under low Oi conditions; and

[0016] FIG. 8 is a graph showing the v/G ratio between crystal center and the R/2 position and the GOI failure free region as a function of nitrogen concentration.

[0017] Corresponding reference characters indicate corresponding parts throughout the drawings.

DETAILED DESCRIPTION

[0018] Provisions of the present disclosure relate to methods for producing single crystal silicon wafers for use in insulated gate bipolar transistors (IGBT). An example IGBT device is shown in FIG. 1. Such devices may include at least four layers (with at least one of the layers being a chip singulated from a wafer produced by an embodiment of the methods described herein). The transistor may include a gate electrode, collector electrode, and emitter.

[0019] The single crystal silicon wafers of the present disclosure are sliced from a single crystal silicon ingot. In accordance with embodiments of the present disclosure and with reference to FIG. 2, an example ingot puller apparatus (or more simply “ingot puller”) for producing a single crystal silicon ingot is indicated generally as “100”. The ingot puller apparatus 100 includes a crucible assembly 102 (or more simply “crucible”) for holding a melt 104 of semiconductor or solar-grade material silicon. The crucible assembly 102 is supported by a susceptor 106.

[0020] The ingot puller apparatus 100 includes a crystal puller housing 108 that defines a growth chamber 152 for pulling a silicon ingot from the silicon melt 104 along a pull axis A. The growth chamber 152 includes two portions - a lower growth chamber 155 (or simply "lower chamber") and an upper growth chamber 165 (or simply "upper chamber") disposed above the lower growth chamber 155. The hotzone of the ingot puller apparatus 100 (e.g., crucible, reflector assembly, susceptor, heaters, and the like) is disposed within the lower chamber 155. During ingot growth, the ingot 113 is pulled through the lower chamber 155 and continues to be pulled through the upper chamber 165 as the ingot lengthens.

[0021] The crystal puller housing 108 includes a domed lower segment 119 that defines the lower chamber 155 and an upper segment 140 that defines the upper chamber 165. The lower domed segment 119 includes a dome-shaped portion 169 which tapers in size to the diameter of the upper segment 140. The upper segment 140 is generally cylindrical in shape and includes a lower end and an upper end. The upper segment 140 of the crystal puller housing 108 is removably connected to the lower segment 119 (e.g., by fasteners, gaskets or the like).

[0022] The crucible assembly 102 is disposed in the lower chamber 155. The crucible assembly 102 has a sidewall 131 and floor 129 and rests on a susceptor 106. The susceptor 106 is supported by a shaft 105. The susceptor 106, crucible assembly 102, shaft 105, and ingot 113 have a common longitudinal axis or "pull axis" A.

ingot tapers in diameter after the main body 145. When the diameter becomes small enough, the ingot 113 is then separated from the melt 104.

[0029] The crystal growth process may be a batch process in which solid silicon is initially added to the crucible assembly 102 to form a silicon melt without additional solid-silicon being added to the crucible assembly 102 during crystal growth. In other embodiments, the crystal growth process is a continuous Czochralski process in which an amount of silicon is added to the crucible assembly 102 during ingot growth.

[0030] The ingot puller apparatus 100 includes a side heater 135 and a susceptor 106 that encircles the crucible assembly 102 to maintain the temperature of the melt 104 during crystal growth. The side heater 135 is disposed radially outward to the crucible sidewall 131 as the crucible assembly 102 travels up and down the pull axis A. The side heater 135 and bottom heater 126 may be any type of heater that allows the side heater 135 and bottom heater 126 to operate as described herein. In some embodiments, the heaters 135, 126 are resistance heaters. The side heater 135 and bottom heater 126 may be controlled by a control system (not shown) so that the temperature of the melt 104 is controlled throughout the pulling process.

[0031] The ingot puller apparatus 100 may include a reflector assembly 151. The reflector assembly 151 includes an opening 157 through which the single crystal silicon ingot 113 is pulled during ingot growth. The ingot puller apparatus 100 may include an inert gas system to introduce and withdraw an inert gas such as argon from the growth chamber 152.

reduced or eliminated at the precipitate region due to low oxygen. The pull speed range between the R/2 position and the ingot center can produce a COP free window, as shown in the right panel of Fig 7 (i.e., free of gate-oxide integrity failures of a size greater than 8 MVcm).

[0042] The nitrogen concentration may be selected to achieve GOI failure free material across the radius of the ingot based on the radial v/G profile. In some embodiments, a difference between the ratio of v/G at the center of the ingot and the ratio of v/G at the R/2 position is determined. The nitrogen concentration may be selected based on the determined difference between the ratio of v/G at the center of the ingot and the ratio of v/G at the R/2 position such that the ingot is free of gate oxide integrity failures across the ingot radius (e.g., nitrogen may be selected according to the function shown in FIG. 8).

[0043] The ratio v/G at the R/2 position and at the center of the crystal may be determined empirically, such as by an axial ramping velocity test method. A full-diameter test ingot is grown in the ingot puller apparatus (i.e., the same ingot puller apparatus at which the product ingots are grown) with the growth velocity being ramped up during growth of the test ingot. The growth velocity, v, at a given radial position of the test ingot (e.g., the R/2 position or the center of the ingot) at which a transition from interstitial-defects begins (i.e., the velocity at which critical v/G occurs) is then determined. The ramped velocity axial test shows where the I-defect region forms at the radial positions (center, edge, R/2) and, from this information, the ratio of v/G between the R/2 position and the center of the ingot can be calculated. As the critical v/G is a pre-determined or known parameter (for a given

doping level), the axial temperature gradient, g, may be calculated for the radial position based on the growth velocity, v, at which the interstitial-defect band terminates at the given radial position in the test ingot.

[0044] The position of the transition from the interstitial-dominant region at the given radial position may be determined by vertical cut slabbing and observation of the slab to determine the position at which the I-defect band stop and determination of the growth velocity, v, at this position. Alternatively, the position at which interstitial defects stop may be determined by slicing wafers from the ingot and observation of the wafers to determine the position at which the interstitial-defects stop.

[0045] Once a product ingot has been grown by a method of the present disclosure, a plurality of wafers are sliced from the single crystal silicon ingot, optionally after one or more additional processing steps (e.g., ingot grinding). Singulation may be performed to divide the wafers into a plurality of semiconductor chips. An insulated gate bipolar transistor may be produced in which at least one of layers of the transistor is a semiconductor chip singulated from the wafer.

[0046] Compared to conventional methods for producing single crystal silicon wafers for insulated gate bipolar transistors, the methods of the present disclosure have several advantages. By controlling the growth parameters such that ingot oxygen concentration is less than 2.75×10^{17} atoms/cm^3, the resulting wafers are suitable for low-oxygen IGBT applications. By determining

CLAIMS:

1. A method for producing single crystal silicon wafers for insulated gate bipolar transistors (IGBT), the method comprising:

producing a single crystal silicon ingot, the single crystal silicon ingot having a radial profile of a ratio between (i) a growth velocity, v, and (ii) an axial temperature gradient, G, the single crystal silicon ingot being produced by:

determining a radial v/G profile of the single crystal silicon ingot;

selecting an ingot nitrogen concentration at which the ingot is free of gate oxide integrity failures across the ingot radius based on the radial v/G profile of the ingot;

adding polycrystalline silicon to a crucible disposed within a growth chamber of an ingot puller apparatus;

heating the polycrystalline silicon to cause a silicon melt to form in the crucible;

adding nitrogen to the silicon melt to achieve the selected ingot nitrogen concentration; and

pulling a single crystal silicon ingot doped with nitrogen from the melt; and

slicing a plurality of wafers from the single crystal silicon ingot, each wafer of the plurality of wafers having an oxygen concentration of less than 2.75 x

10^{17} atoms/cm^3, being free of crystal originated particles and being free of gate-oxide integrity failures.

2. The method as set forth in claim 1 wherein selecting an ingot nitrogen concentration at which the ingot is free of gate oxide integrity failures across the ingot radius based on the radial v/G profile of the ingot comprises:

determining a difference between the ratio of v/G at the center of the ingot and the ratio of v/G at a point halfway between the center and a circumferential edge of the ingot; and

selecting a nitrogen concentration at which the ingot is free of gate oxide integrity failures across the ingot radius based on the determined difference between the ratio of v/G at the center of the ingot and the ratio of v/G at a point halfway between the center and a circumferential edge of the ingot.

3. The method as set forth in claim 2 wherein the nitrogen concentration at which the ingot is free of gate oxide integrity failures across the ingot radius is determined based on a ratio between the ratio of v/G at the center of the ingot and the ratio of v/G at a point halfway between the center and a circumferential edge of the ingot.

4. The method as set forth in any one of claims 1 to 3 wherein the radial v/G profile is determined empirically by a ramping test method comprising:

pulling a test ingot in the ingot puller apparatus, the test ingot being grown while ramping the growth velocity;

determining the growth velocity, v, at a given radial position of the test ingot at a transition from interstitial-defects; and

calculating the axial temperature gradient, g, at the radial position based on a predetermined critical v/G at the transition from interstitial-defects and the growth velocity, v, at which the transition from interstitial-defects was observed at the radial position in the test ingot.

5. The method as set forth in claim 4 wherein the radial position is the R/2 position.

6. The method as set forth in claim 5 wherein v/G is also determined at the center of the ingot.

7. The method as set forth in any one of claims 4 to 6 wherein the growth velocity, v, at a given radial position of the test ingot at the transition from interstitial-defects is determined by vertical cut slabbing and observation of the slab to determine the position at which the transition from interstitial-defects occurs and determination of the growth velocity, v, at the position at which the transition from interstitial-defects occurs.

8. The method as set forth in any one of claims 4 to 6 wherein the growth velocity, v, at a given radial position of the test ingot at the transition from interstitial-defects is determined by slicing wafers from the ingot and observation of the wafers to determine the position at which the transition from interstitial-defects occurs and determination of the growth velocity, v, at the position at which the transition from interstitial-defects occurs.

9. The method as set forth in any one of claims 1 to 8 wherein a concentration of nitrogen in each wafer is at least 2×10^{13} atoms/cm^3.

10. The method as set forth in any one of claims 1 to 9 wherein the concentration of oxygen in each wafer is less than 2.2×10^{17} atoms/cm^3.

11. The method as set forth in any one of claims 1 to 10 wherein each wafer of the plurality of wafers has an oxygen content of less than 5.5 ppma.

12. The method as set forth in any one of claims 1 to 10 wherein each wafer of the plurality of wafers has an oxygen content of less than 5.0 ppma.

13. The method as set forth in any one of claims 1 to 12 wherein one or more growth parameters selected from a crystal rotation rate, a crucible rotation rate and a magnetic field strength are selected to achieve the oxygen concentration in each of the plurality of wafers of less than 2.75×10^{17} atoms/cm^3.

14. The method as set forth in claim 13 wherein:

a cusp magnetic field is applied to the silicon melt;

the crystal rotation rate is between 6 rpm and 15 rpm;

the crucible rotation rate is between 0.5 rpm and 2.5 rpm; and

the magnetic field strength is between 0.02 and 0.075 Tesla at an edge of the silicon ingot at a melt-solid interface and between 0.05 and 0.20 Tesla at a wall of the crucible.

15. The method as set forth in claim 13 wherein:

a horizontal magnetic field is applied to the silicon melt with a maximum gauss plane of the horizontal magnetic field being maintained from 20 mm to 250 mm above a melt free surface;

the crucible rotation rate is between 0.1 rpm to 5.0 rpm; and

the magnetic flux density is from 0.1 Tesla to about 0.4 Tesla.

16. The method as set forth in any one of claims 1 to 15 wherein the plurality of wafers are free of gate-oxide integrity failures of a size greater than 8 MVcm.

17. The method as set forth in any one of claims 1 to 16 wherein the single crystal silicon ingot is grown in a batch process in which silicon is not added to the crucible during growth of the single crystal silicon ingot.

18. The method as set forth in any one of claims 1 to 16 wherein the single crystal silicon ingot is grown in a continuous process in which silicon is added to the crucible during growth of the single crystal silicon ingot.

19. The method for producing an insulated gate bipolar transistor comprising:

singulating a wafer produced by the method of any one of claims 1 to 18 into a plurality of semiconductor chips; and

forming an insulated gate bipolar transistor having at least four layers, wherein at least one of the layers comprises a semiconductor chip singlated from the wafer, the insulated gate bipolar transistor comprising a gate electrode, collector electrode, and emitter.