CLAIMS

1. A process of fabricating a printed circuit board, the process comprising:

providing a first sheet of dielectric material including a first top surface having at least one first conductive trace and a second sheet of dielectric material including a second top surface having at least one second conductive trace;

depositing a first solder bump on the at least one first conductive trace;

applying the second sheet of dielectric material to the first sheet of dielectric material with bonding film sandwiched in between;

bonding the first and second sheets of dielectric material to one another; ~~and~~

providing a conductive material to connect the first solder bump on the at least one first conductive trace to the at least one second conductive trace;

depositing a second solder bump on the at least one second conductive trace; and

removing a portion of the second sheet of dielectric material between the first solder bump and the second solder bump to create a ramp between the first solder bum and the second solder bump,

wherein the ramp is formed by milling along a continuous path through the first solder bump, the second sheet of dielectric material, the at least one second conductive trace, and the second solder bump.

~~2. The process of claim 1, further comprising depositing a second solder bump on the at least one second conductive trace.~~

~~3. The process of claim 2, further comprising removing a portion of the second sheet of dielectric material between the first solder bump and the second solder bump to create a ramp therebetween.~~

~~4. The process of claim 3, wherein removing a portion of the second sheet of dielectric material includes using a milling process to remove the portion.~~

~~5~~2. The process of claim ~~2~~1, further comprising removing a portion of ~~at least one of~~ the first solder bump and the second solder bump to provide a clean surface for soldering.

~~6~~3. The process of claim ~~5~~2, wherein removing a portion of ~~the at least one of~~ the first solder bump and the second solder bump includes using a milling process to remove the portion.

~~7~~4. The process of claim 1, wherein the conductive interconnection is performed by an aerosol jet process configured to use aerodynamic focusing to precisely and accurately deposit electronic inks between the first solder bump and the second solder bump.

~~8~~5. The process of claim 1, wherein the first solder bump is located between the first sheet of the dielectric material and the second sheet of dielectric material.

~~9~~6. The process of claim ~~8~~5, wherein the second conductive trace includes a ground plane.

~~10~~7. The process of claim ~~9~~6, further comprising creating a through hole from the second sheet of dielectric material, the first solder bump and the first sheet of dielectric material.

~~11~~8. The process of claim ~~10~~7, wherein the conductive material is applied to walls of the through hole.

~~12~~9. The process of claim ~~11~~8, wherein the conductive material includes a solder ball, formed of solder paste material, disposed above the through hole, the solder ball being reflowed so that the solder paste material is drawn through the through hole.

~~13~~10. The process of claim ~~12~~9, wherein the solder paste material is drawn through the through hole by a vacuum process to coat the walls of the through hole.

~~14~~11. The process of claim 1, wherein the first solder bump includes lead-based or lead-free solder.

~~15~~12. The process of claim 1, wherein bonding the first and second sheets of dielectric material to one another includes curing the sheets under pressure and temperature to form an integral final product.

~~16. A circuit comprising:~~

~~a first sheet of dielectric material including a first top surface having at least one first conductive trace;~~

~~a second sheet of dielectric material including a second top surface having at least one second conductive trace, the second sheet of dielectric material being bonded to the first sheet of dielectric material with bonding film;~~

~~a first solder bump provided on the at least one first conductive trace; and~~

~~a conductive material configured to connect the first solder bump on the at least one first conductive trace to the at least one second conductive trace.~~

~~17. The circuit of claim 16, further comprising a second solder bump on the at least one second conductive trace.~~

~~18. The circuit of claim 17, further comprising a ramp created by removing a portion of the second sheet of dielectric material between the first solder bump and the second solder bump.~~

~~19. The circuit of claim 16, wherein the first solder bump is located between the first sheet of the dielectric material and the second sheet of dielectric material, the circuit further comprising a through hole from the second sheet of dielectric material, the first solder bump and the first sheet of dielectric material.~~

~~20. The circuit of claim 19, wherein the conductive material is applied to walls of the through hole.~~