two from the edge of the semiconductor wafer, may, in effect, interact with the edge ring so as to provide a small, localized region in which the flow conductance between the edge ring and the semiconductor wafer is higher than the flow conductance therebetween in most or all other locations around the edge ring. This, in turn, was found by the inventors to result in a locally elevated radially inward flow rate of the purge gas from the region between the edge ring and the pedestal. Thus, the flow rate of purge gas across the edge of the semiconductor wafer and towards the wafer center may be elevated at the location(s) along the semiconductor wafer's edge that overlay the notch(es) that may be present on the wafer. Some wafers have flats instead of notches, but a similar effect may be observed with such wafers as well (although potentially spread out along a larger portion of the outer circumference of the wafer).

[0046] The present inventors, having identified such issues as contributing to potential wafer non-uniformity, determined that such non-uniformities could be mitigated or even eliminated by modifying the structure of the edge ring such that the underside of the edge ring that overlaps with the wafer when in use has areas or regions that are raised and/or recessed with respect to the surface that forms the nominal underside of the edge ring that radially overlaps with a wafer when the wafer is present. Such areas or regions allow for local adjustment of the flow conductance in the gap between the underside of the edge ring and the top of the wafer to as to increase or decrease the amount of purge gas that flows radially inward at that location. The present inventors also determined that such non-uniformities could alternatively or additionally be mitigated or even eliminated by modifying the circular inner edge of the edge ring so as to have regions (which are positioned so as to align with features, e.g., wafer notches and/or recesses or receptacles in the pedestal) in which the inner edge moved radially inward or outward with respect to the circle that the inner edge of the edge ring lies along. Further details of such implementations are discussed in more detail below with respect to the Figures.

[0047] FIG. 1 depicts a plan view of an example edge ring 100 according to the present disclosure. The edge ring 100 has an outer portion 106 and an inner portion 104. The inner portion 104 has an inner edge 108. The inner edge 108 may define a substantially circular opening 110 centered on a ring center axis 112. The circular opening 110 has a diameter 114. The diameter 114 is slightly less than the diameter of a semiconductor wafer 102. In the example shown, the outline of an example semiconductor wafer 102 is shown. For example, a semiconductor wafer 102 may have a diameter of about 300 mm. In this example, the diameter 114 of the circular opening 110 is less than the 300 mm. The diameter 114 may be between 297-299.5 mm when used for processing 300 mm semiconductor wafer (FIG. 1, it will be understood, is not drawn to

scale).

[0048] The edge ring 100 may have flow conductance features. The flow conductance features may be used to tune the flow conductance of the gap between the semiconductor wafer 102 and the overlapping portion of the inner portion 104 of the edge ring 100. The flow conductance features may be placed in specific locations to modify the flow conductance in corresponding areas around the semiconductor wafer 102. In the example shown in FIG. 1, the edge ring 100 has four locations where the flow conductance features are placed. The first three locations are each at a corresponding section 122 and the fourth location is at a notch section 118. Each section 122 may have a first type of flow conductance feature while the notch section 118 may have a second type of flow conductance feature, thereby allowing the radial flow conductance of the edge ring to be tuned to accommodate different purge gas flow rate needs at different locations. The notch section 118 may be located so as to align with a notch 120 of the semiconductor wafer 102 that the edge ring 100 is to be used with. The sections 122 may similarly generally be above recesses or receptacles in a pedestal (not shown) that are designed to receive fingers or similar structures attached to the edge ring 100. The fingers (not shown, but see FIGS. 2-1 and 2-3) and similar structures may be attached to the edge ring 100 by attachment screws 116.

[0049] FIG. 2-1 shows a perspective view of the edge ring 100 holding the semiconductor wafer 102 in a raised position above a pedestal 124. The semiconductor wafer 102 is held by edge ring features 156 attached to the edge ring 100 by attachment screws. In this embodiment, the edge ring features 156 are fingers 158 having a roller 164. In the embodiment, there are three edge ring features 156. In some embodiments, there may be a single edge ring feature 156. In some embodiments, there may be two or more edge ring features 156 attached to the edge ring 100. The pedestal 124 may have one or more receptacles 162. The pedestal 124 has receptacles162 to match the number of edge ring features 156. In the example shown, the edge ring 100 has three edge ring features 156 and the pedestal 124 has three receptacles 162. As discussed above, a receptacle 162 can sometimes trap small amounts of process gases during a semiconductor processing operation. This trapped gas may be undesirably released during a subsequent phase of the semiconductor processing operation and be a source of wafer non-uniformity. The pedestal 124 may also have a plurality of ports 163. The ports 163 may be used to deliver gases such as a purge gas to the underside of the edge ring during wafer processing.

[0050] FIG. 2-2 shows a perspective of the edge ring 100 in a lowered position over the pedestal 124. When the edge ring 100 is lowered from a raised position, as shown in FIG. 2-1, to the lowered position, the edge ring features 156 are lowered into their corresponding receptacle 162

144 is coincident with the highest portion of the top surface 142 and parallel to the first reference plane 132.

[0054] FIGS. 5-1, 5-2, and 6-1 through 6-5 show examples of flow conductance features on an edge ring 500 over a notch 520 in a wafer 502. When an edge ring is used during semiconductor wafer processing, a notch area of the semiconductor wafer is minimally covered by the edge ring, i.e., an outer edge of the wafer at the notch is radially closer to an inner edge of the edge ring than the outer edge of the wafer in other portions wafer. Thus, during purge operations, the area around the notch is generally less obstructed and has a higher flow conductance than other locations around the inner perimeter of the edge ring. The high flow conductance may allow more purge gas to flow radially inward in the region around the notch compared to in other areas around the circumference of a semiconductor wafer.

[0055] FIG. 4 shows flow conductance in the area around the notch of a semiconductor wafer compared to the flow conductance in other areas around the circumference of a semiconductor wafer. Shown in each figure is a cross-sectional view an edge ring 500 over a semiconductor wafer 502 on a pedestal 524. The top figure shows a cross-sectional view of the semiconductor wafer 502 under the edge ring 500 at a non-notch location along the wafer circumference while the bottom shows a cross-sectional view of the semiconductor wafer 502 under the edge ring 500 at a notch 520. Each view shows a higher-conductance region 570 and a lower-conductance region 572. Around the circumference, there is a larger radial distance between an inner edge 508 of the edge ring 500 and an outer edge 536 of the semiconductor wafer 502 and thus the smaller higher-conductance region 570 is smaller compared to the higher-conductance region 570 at the notch 520, where there is a smaller radial distance between the inner edge 508 of the edge ring 500 and the outer edge 536 of the semiconductor wafer 502. Since the higher-conductance region 570 is larger at the notch 520, there is generally a higher flow conductance in this area which allows more purge gas to flow radially inward compared to the other areas around the circumference of the semiconductor wafer. Flow conductance features in the edge ring may be used to reduce the flow conductance in the area around the notch of the semiconductor wafer. By using flow conductance features to reduce the flow conductance, the flow conductance around the wafer notch may be tuned so that the amount of gas remaining in the notch area after a purge is consistent with the amount of gas remaining in other areas around the circumference of the semiconductor wafer.

[0056] One example flow conductance feature that may be used to reduce the flow conductance in the vicinity of where a wafer notch will be is an overhang section. An overhang section, as the term is used herein, refers to a portion of the edge ring that extends radially inward from a circle

532 coplanar with a majority of an outer bottom surface 528, a second reference plane 534, and a top reference plane 544 are shown. As discussed above, the second reference plane 534 is coincident with a majority of an inner bottom surface and parallel to the first reference plane 532. The top reference plane 544 is coincident with the highest portion of a top surface 542 and parallel to the first reference plane 532.

[0062] FIG. 6-1 shows the edge ring 500 having an overhang section 538. In the embodiment shown, the overhang section 538 locally extends the inner portion 504 of the edge ring 500 radially inward, moving the inner edge 508 inwards so that the inner edge in the overhang section is closer to the center of the edge ring than the inner edge is around most or all of the remainder of the edge ring 500. Depending on the flow conductance desired, the overhang section 538 may be extended or shortened.

[0063] FIG. 6-2 shows the edge ring 500 having an overhang section 538 and a raised section 546. The raised section 546 in FIG. 6-2 is indicated by the darker shaded region relative to the rest of the edge ring 500. The raised section 546 has a raised section bottom surface 548. The bottom surface 548 is between the first reference plane 532 and the second reference plane 534, thus positioning a portion of the bottom surface of the edge ring 500 closer to a top surface 526 of the semiconductor wafer 502. The raised section bottom surface 548 may be located anywhere between a top surface 526 of the semiconductor wafer 502 and the second reference plane 534. By having a raised section 546 the gap between the edge ring 500 and the semiconductor wafer 502 reduces, thus reducing the flow conductance in the area. The closer the raised section bottom surface 548 is to the wafer 502, the smaller the gap between the raised section bottom surface 548 and the semiconductor wafer 502. The smaller the gap between the raised section bottom surface 548 and the semiconductor wafer 502, the lower the flow conductance is in that region. In the embodiment shown, the raised section 546 extends from the overhang section 538 through the inner portion 504 to a boundary 507 between the inner portion 504 and the outer portion 506. The boundary 507 may also be referred to as the outer edge of the inner portion 504 or the inner edge of the outer portion 506.

[0064] FIG. 6-3 shows another embodiment of an edge ring 500 having both an overhang section 538 and a raised section 546. In this embodiment, the raised section 546 extends from the overhang section 538 into the inner portion 504. Unlike in the previous embodiment, the raised section 538 ends part of the way into the inner portion 504. In some embodiments, the raised section 538 may only be a segment of the inner portion 504 between the inner edge 508 and the boundary 507. In some embodiments, the raised section may not extend to the inner edge 508 of

the inner portion 504. In these embodiments, the raised section starts radially outward of the inner edge 508.

[0065] FIG. 6-4 shows yet another example of an edge ring 500 with a flow conductance feature of a raised section 546 for use over the notch 520 of the semiconductor wafer 502. The raised section 546 extends outward from the nominal bottom surface of the edge ring 500 so that a bottom surface 548 of the raised section 546 is between a top surface 536 of the semiconductor wafer 502 and the second reference plane 534. The raised section 546 extends from the inner edge 508 through the inner portion 504 until a boundary 507 between the inner portion 504 and the outer portion 506. In the example shown, the edge ring 500 does not have an overhang section as shown in the previous examples. Thus, the flow conductance is modified only by the decreased gap between the bottom surface 548 of the raised section 546 and a top surface 526 of the semiconductor wafer 502.

[0066] FIG. 6-5 shows another example of an edge ring 500 with a flow conductance feature of a raised section 546 for over the notch 520 of the semiconductor wafer 502. Similar to the example in FIG. 6-4, in this example the raised section extends outward so that a bottom surface 548 of the raised section 546 is between a top surface 526 of the semiconductor wafer 502 and the second reference plane 534. In this example, the raised section 546 extends from the inner edge 508 through the inner portion 504 towards the outer portion 506. The raised section 546 ends part way into the inner portion 504 before extending to a boundary 507 between the inner portion and the outer portion 506. In some embodiments, the raised section 546 may be a segment of the inner portion 504 between the inner edge 508 and the boundary 507.The segment of the raised section 546 may be designed to create a desired flow conductance in the area above the notch 520 of the wafer 502.

[0067] While the above-discussed flow conductance features may be used to decrease flow conductance in a localized area of an edge ring, e.g., to offset increased flow conductance that may be present due to features such as wafer notches, a second type of flow conductance features may be used to locally increase flow conductance so as to increase purge gas flow rate in particular areas around the circumference of the edge ring. Generally speaking, such flow conductance features may be used where features on an edge ring, e.g., a finger, that may require the presence of recesses or receptacles in the pedestal are located. Such recesses or receptacles may trap gases that may resist being purged through the standard purging gas flows that may be provided by an edge ring. The second type of flow conductance features may increase the flow conductance in these areas, allowing for locally increased purge gas flow that may act to more efficiently remove

the trapped gas, thus preventing such trapped gas from leaking out slowly over a longer period of time and potentially interfering with subsequent processing operations. Examples of the second type of flow conductance features include a recessed section in the bottom surface of the inner portion of the edge ring, a cut-out section along the inner edge of the edge ring, or a combination thereof.

[0068] FIG. 7 depicts a plan view of an example edge ring 700 with three feature sections 722. In some embodiments there may be a single feature section. In some embodiments, there may be two or more feature sections. Such implementations may, for example, be used in situations in which there are other than three recesses or receptacles in the pedestal.

[0069] The edge ring 700 has an outer portion 706 and an inner portion 704. The inner portion 704 has an inner edge 708. The inner edge 708 may define a substantially circular opening 710 centered on a ring center axis 712. A semiconductor wafer 702 with an outer edge 736 is shown. The inner edge 708 of the inner portion 704 is interior to the outer edge 736 of the semiconductor wafer 702. As discussed with respect to FIG. 1, sections 722 have features below the edge ring 700 that may require the presence of recesses or receptacles in the pedestal to house such features when the edge ring is placed on top of the pedestal. Such recesses or receptacles may trap or contain processing gases that may then leak out slowly and potentially interfere with subsequent processing operations using other gases. It may thus be desirable to provide for localized areas of the edge ring with higher flow conductance to enhance the purge rate of such areas. If the purge rate is left at the "default" purge rate in such areas, the processing gas that leaks out of the recesses or receptacles may cause localized processing non-uniformities on the semiconductor wafer 702 around the sections 722 to increase. The flow conductance features discussed above may be located in these sections to improve purge gas flow rate in these areas, thereby allowing the trapped process gases to be more expediently removed.

[0070] As mentioned earlier, one type of flow conductance feature that may be used is a recessed section (not shown). Such flow conductance features are usually cut from a bottom surface of the inner portion 704. The sections 722 highlight the area of the edge ring 700 that may be modified to incorporate a flow conductance feature. In the embodiment shown, the sections 722, and thus the flow conductance features, i.e., recessed sections, have an arcuate outer edge. In this embodiment, the arcuate edge follows an arc of a circle concentric with the edge ring 700. In some embodiments, the recessed section may have a straight outer edge. In some embodiments, the recessed sections may extend from the inner edge 708 through the inner portion 704 to a boundary 707 between the inner portion 704 and the outer portion 706. The boundary 707 is where

an inner portion outer edge meets an outer portion inner edge and may be referred to as either the inner portion outer edge or outer portion inner edge. In some embodiments, the recessed section may only cover a segment of the inner portion 704 that extends radially outward. In these embodiments, the recessed section may extend to one of or neither of the boundary 707 and inner edge 708 of the inner portion 704.

[0071] FIG. 8-1 through FIG. 8-3 show three cross sectional areas of edge rings 700 each with an example recessed section 750. Each figure shows an edge ring 700 with an outer portion 706, inner portion 704, and a top surface 742. The inner portion 704 meets the outer portion 706 at a boundary 707. The inner portion 704 has an inner bottom surface 730 and an inner edge 708. The outer portion 706 has an outer bottom surface 728. A first reference plane 732 is coplanar at with a majority of the outer bottom surface 728. A second reference plane 734 is coincident with a majority of the inner bottom surface 730 and is parallel to the first reference plane 732. A top reference plane 744 is coincident with a highest portion of the top surface 742 and is parallel to the first reference plane 732. The second reference plane 734 is between the first reference plane 732 and the top reference plane 744. Shown in each figure is a semiconductor wafer 702 on a pedestal 724. The semiconductor wafer 702 has an outer edge 736 and a top surface 726. In each figure, the wafer outer edge 736 is radially outwards of the inner edge 708 of the inner portion 704, i.e., the inner edge 708 of the inner portion 704 lies within a circle defined by the wafer outer edge 736.

[0072] FIG. 8-1 shows a first example of a recessed section 750. The recessed section 750 is an area where material has been removed from the inner portion 704 of the edge ring 700, thereby creating a recessed section bottom surface 752. The recessed section bottom surface 752 may be anywhere between the second reference plane 734 and the top reference plane 744. In some implementations, the recessed section bottom surface 752 may be at least 10 um away from the second reference plane 734. In some implementations, the recessed section bottom surface 752 may be up to a distance of 200 um away from the second reference plane 734. The recessed section 750 raises the bottom surface in the local area of the edge ring 700, creating a larger gap between a portion of a bottom surface of the edge ring 700 and a wafer top surface 726. The enlarged gap may cause the flow conductance in that area to be increased and thus may encourage a higher purge gas flow rate that more effectively purges any process gas in the area around the recessed section 750. Generally, the closer the recessed section bottom surface 752 is to the top reference plane 744, the higher the flow conductance. As shown in FIG. 8-1, the recessed section may extend from the inner edge 708 to the boundary 707.

may be two or more cut-out sections. Such implementations may, for example, be used in situations in which there are other than three recesses or receptacles in the pedestal.

[0077] Shown in the figure is a semiconductor wafer 902. The edge ring 900 has an outer portion 906 and an inner portion 904. The inner portion 904 has an inner edge 908. The semiconductor wafer 902 has a reference circle 960 that is generally co-radial and concentric with the inner edge 908 of the edge ring 900 that is centered on a ring center axis 912, i.e., the reference circle 960 is concentric with the inner edge 908 not part of each of the three cut-out sections 954. At each of the three cut-out sections 954, the inner edge 908 of the inner portion 904 is moved radially outward so that the inner edge is between the reference circle 960 and a boundary 907 between the inner portion 904 and the outer portion 906. As describe in figures above, the boundary 907 is where the inner portion outer edge outer portion inner edge meet. In the embodiment shown, the cut-out section 954 is an angular sector from the ring center axis 912. The inner edge 908 at the cut-out section 954 is an arcuate shape. In some embodiments the inner edge 908 at the cut-out section 954 may be a straight line. The arcuate shape may be less than 5 degrees. In some embodiments, the arcuate shape may be between 5 and 10 degrees. In still some other embodiments, the arcuate shape may be greater than 10 degrees. In some embodiments, the cut-out section may be a rectangular shape (not shown).

[0078] As shown in FIG. 9, the inner edge 908 at the cut-out section 954 is moved radially outwards toward the outer portion 906 relative to the non-cut-out section areas. In the embodiment shown, the inner edge 908 at each cut-out section 954 is approximately midway between the reference circle 960 and the boundary 907. In this embodiment, the inner edge 908 at the cut-out sections 954 remain radially interior to a wafer outer edge 936, i.e., the inner edge 908 at each cut-out section lies within a circle concentric and co-radial with the wafer outer edge. It should be noted that the examples shown are exaggerated in size to allow for clearer viewing; such cutouts and wafer overlap may be much smaller than shown, e.g., radial depths of the cutouts may be a millimeter or so. In some implementations, the radial depths of such cutouts may be less than a millimeter, e.g., less than 0.9 mm, less than 0.8 mm, less than 0.7 mm, less than 0.6 mm, less than 0.5 mm, less than 0.4 mm, less than 0.3 mm, etc. In some embodiments, the cut-out section 954 may have the inner edge 908 closer to the reference circle 960such that the inner edge at the cut-out section is closer to the reference circle 960 than the wafer outer edge 936. In some other embodiments, the cut-out section 954 may have the inner edge 908 closer to the boundary 907 such that the inner edge is above or slightly radially interior to the wafer outer edge 936.

[0079] FIGS. 10-1 and 10-2 show cross-sectional views of example cut-out sections 954 on an

edge ring 900. In FIG. 10-1, the edge ring 900 has a single flow conductance feature, a cut-out section. The example in FIG. 10-2 has two flow conductance features on an edge ring 900, a cut-out section 954 and a recessed section 950. In both figures, the edge ring 900 has an outer portion 906, an inner portion 904, and a top surface 942. The inner portion 904 meets the outer portion 906 at a boundary 907. The boundary 907 may be referred to as the outer edge of the inner portion 904 or inner edge of the outer portion 906. The inner portion 904 has an inner bottom surface 930 and an inner edge 908. The outer portion 906 has an outer bottom surface 928. A first reference plane 932 is coplanar with a majority of the outer bottom surface 928. A second reference plane 934 is coincident with a majority of the inner bottom surface 930 and is parallel to the first reference plane 932. A top reference plane 944 is coincident with a highest portion of the top surface 942 and is parallel to the first reference plane 932. Shown in each figure is a semiconductor wafer 902 on a pedestal 924. The semiconductor wafer 902 has an outer edge 936. In each figure, the outer edge 936 is radially outward of the inner edge 908 of the inner portion 904.

[0080] The cross-sectional view in FIG. 10-1 shows the cut-out section 954 of the edge ring 900. Behind the cut-out section 954 is the edge ring 900 without a flow conductance feature, i.e., the normal edge ring without any cut-out section, which is indicated by a darker shaded region. The cut-out section 954 has the inner edge 908 closer to the outer portion 906 of the edge ring 900 reducing the overhang of the edge ring 900 over the semiconductor wafer 902 in the local area. As described with reference to FIG. 9, the cut-out section 954 may extend radially inward such that the material removed is reduced, or may extend radially outward, such that the material removed is greater. For example, the cut-out section 954 may remove the inner portion 904 in the area, leaving the inner edge 908 above or slightly interior to the wafer outer edge.

[0081] In the embodiment shown, the inner bottom surface 930 is unchanged and remains at the same height as the rest of the edge ring 900. Thus, in this embodiment, the flow conductance in the area is changed by reducing the overhang of the edge ring 900 by the cut-out section 954 and not by changing the gap between the inner bottom surface 930 and a top surface 926 of the semiconductor wafer 902.

[0082] In the embodiment in FIG. 10-2, an edge ring 900 has both a cut-out section 954 and a recessed section 950. Unlike in the previous embodiment, both the amount of overhang of the edge ring 900 over the semiconductor wafer 902 and the gap between a bottom surface of the edge ring 900 and a top surface 926 of the semiconductor wafer 902 are modified to change the flow conductance in the area. The cut-out section 954 may be made so that the inner edge 908 of the inner portion 904 at the cut-out section 954 is approximately midway between the inner edge of

an unmodified inner portion and the boundary 907. In the embodiment shown, the inner edge 908 of the cut-out section 954 is radially interior to the wafer outer edge 936. The cut-out section 954 can be made deeper, e.g., the inner edge at the cut-out section may be moved closer toward the outer portion 906, or shallower, e.g., the inner edge at the cut-out section may be moved away from the outer portion 906, depending on the desired flow conductance. In some embodiments, the cut-out section 954 may be made deeper towards the outer portion 906. In some embodiments, the cut-out section 954 may be made shallower so that the inner edge 908 is closer to a center (not shown) of the semiconductor wafer 902. The recessed section 950 raises a recessed section bottom surface 952 away from the wafer top surface 926. The recessed section bottom surface 952 is between the top reference plane 944 and the second reference plane 934. The recessed section 950 may be modified as described with reference to FIGS. 8-1 through 8-3.

[0083] To assist with further understanding and to provide additional insight, various example recessed sections and raised sections are shown in FIG. 11. FIG. 11 provides four example recessed sections and four raised sections on an inner portion 1104 of an edge ring 1100; these flow conductance features are all placed side-by-side for comparison. A first recessed section 1180 is an example of the embodiment discussed with respect to FIG. 8-3. A second recessed section 1182 is a perspective view of an example of the recessed section 650 shown in FIG. 8-1. A third recessed section 1184 is a perspective view of an example recessed section 650 shown FIG. 8-3. A fourth recessed section 1186 is a perspective view of an example recessed section 750 shown in FIG. 8-2. A first raised section 1190 is an example of the embodiment discussed with respect to FIG. 6-5. A second raised section 1192 is a perspective view of an example of the raised section 546 shown in FIG. 6-4. A third raised section 1194 is another example of the embodiment discussed with respect to FIG. 6-5. A fourth raised section 1196 is a perspective view of an example raised section 646 shown in FIG. 6-5.

[0084] Returning to FIG. 1, each of the sections 122 may be located above a corresponding feature, such as the features 156 shown in FIG. 2. The sections 122 may extend through circumferential regions or sectors of arc that may vary depending on the particular flow conductance characteristics desired, e.g., as shown by the three different sizes of feature sections. In the example shown, the sections 122 annular sectors of the inner portion of the edge ring 100. In some embodiments, the sections 122 may be rectangles that extend to the inner edge 108.

[0085] Similarly, the notch section 118 is located above the notch 120 of the semiconductor wafer 102. The notch section 118 may extend through circumferential regions or sectors of arc that may vary depending on the particular flow conductance characteristics desired, e.g., as shown

CLAIMS

1. An edge ring for use with a wafer having a diameter D and a thickness T comprising:

an outer portion having an outer bottom surface; and

an inner portion having a top surface, an inner bottom surface, and an inner edge, wherein:

the outer bottom surface defines a first reference plane that is coplanar with at least a portion thereof;

the inner bottom surface defines a second reference plane that is parallel to the first reference plane and coincident with at least a portion of the inner bottom surface;

the inner bottom surface is between the first reference plane and the top surface;

the inner bottom surface is at least a distance T away from the first reference plane;

the inner edge has a nominal inner diameter less than D; and

the edge ring includes one of the following:

(a) one or more raised sections, each raised section located within the inner portion and having a raised section bottom surface between the first reference plane and the second reference plane;

(b) an overhang section with material within a circular region centered within the edge ring and having a diameter equal to the nominal inner diameter, wherein the portion of the inner edge defining the overhang section has a non-linear profile;

(c) one or more recessed sections, each recessed section having a recessed bottom surface between the second reference plane and the top surface;

(d) any two of (a), (b), or (c); or

(e) all three of (a), (b), and (c).

2. The edge ring of claim 1, wherein the one or more recessed sections includes a plurality of recessed stations.

3. The edge ring of claim 2, wherein the inner portion has three recessed sections.

4. The edge ring of claim 1, wherein the edge ring includes at least the one or more recessed sections and each recessed section starts at the inner edge of the inner portion and extends towards an outer edge of the inner portion.

5. The edge ring of claim 1, wherein the edge ring includes at least the one or more recessed sections and each recessed bottom surface is at least 10 um away from the second reference plane.

6. The edge ring of claim 1, wherein the edge ring includes at least the one or more recessed sections and each recessed section has an arcuate outer edge.

7. The edge ring of claim 1, wherein the edge ring includes at least the one or more recessed sections and each recessed section has a straight outer edge.

8. The edge ring of claim 1, wherein the inner portion has one or more angular sectors in which the inner edge is between the circular region and an outer edge of the inner portion.

9. The edge ring of claim 8, wherein the inner portion has three angular sectors.

10. The edge ring of claim 8, wherein the inner edge at each of the one or more angular sectors is between the circular region and a reference circle concentric with the circular region and a diameter D.

11. The edge ring of claim 8, wherein the inner edge at each of the one or more angular sectors is an arcuate shape.

12. The edge ring of claim 8, wherein the inner edge at each of the one or more angular sectors is straight.

13. The edge ring of claim 1, wherein the raised section bottom surface is at least 300 um above the first reference plane.

14. The edge ring of claim 1, wherein the overhang section has an overhang inner edge that is a chord of the circular region.

15. The edge ring of claim 1, wherein the overhang section is sector-shaped.

16. The edge ring of claim 1, wherein the overhang section is U-shaped.

17. The edge ring of claim 1, wherein the overhang section has an overhang section bottom surface between the first reference plane and the second reference plane.

18. The edge ring of claim 1, wherein the inner edge has a nominal inner diameter within 95% and 99.9% of D.

19. The edge ring of claim 1, wherein the edge ring is made of a ceramic material.

20. The edge ring of claim 1 further comprising a plurality of fingers, wherein:

each finger has a base, a radially inward-extending portion supported by the base, and a roller configured to rotate relative to the inward-extending portion, and

the base of each finger is connected with the outer bottom surface.

21. The edge ring of claim 1 wherein D is approximately 300 mm.

22. The edge ring of claim 1 wherein T is approximately 775 um.