

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO THE MANUFACTURE OF TRANSISTOR STRUCTURES

(71) We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION, of 464 Ellis Street, Mountain View, California 94040, United States of America, a corporation organised and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and the following statement:—

This invention relates to the manufacture of transistor structures and in particular to the manufacture of double-diffused, lateral transistor structures.

Lateral transistors are well known and have been employed in integrated circuit technology for some time as appears, for example from U.S. Patent 3,571,674. Conventional lateral transistors, however, and to particular PNP lateral transistors, have operated at frequencies much lower than desirable for modern integrated circuits. This relatively low frequency response have been substantially attributed to two factors. First, the relatively large base width of the lateral transistor increases the transit time for minority carriers passing through the base from the emitter. The relatively large base width results principally from the minimum photoresist line width consistently available during manufacture of the devices. Second, for a given amount of base impurity, the uniform base concentration profile further increases the transit time over that achievable in devices having graded base concentration profiles.

Double-diffused vertical transistors are also well known for example, from U. S. Patent 3,025,589 and U. S. Patent 3,648,125. The process by which vertical double-diffused transistors are made has several advantages over other processes, such as the mesa process. First, the base width of the

transistor can be varied by controlling the diffusion processes, rather than by altering the dimensions of the masks used in the diffusion processes. Second, the concentration profile of the base can be graded, that is, the base impurity concentration at the collector base junction, can be made greater than the base impurity concentration at the collectorbase junction. It is well known that increases in this difference for a given amount of base impurity increase the high frequency response of the transistor. See Transistor Engineering, by A. B. Phillips, McGraw-Hill, 1962.

In summary, prior art integrated circuits have included vertical double-diffused NPN and PNP transistors, and lateral NPN and PNP transistors with a uniform concentration of base dopant. Because the frequency response of lateral PNP transistors has been lower than desired, the prior art integrated circuits for applications requiring high frequency response have typically used (1) NPN type lateral transistors, as these are approximately three times faster than PNP type lateral transistors, or (2) complementary double-diffused vertical PNP and NPN devices on the same chip. The first alternative eliminates PNP transistors from many applications where their use would otherwise be beneficial. The second alternative involves the technology of complementary vertical double-diffused transistors—a very complicated technology resulting in many defects in the wafers, and a low yield, high cost product. Additionally, the complementary double-diffused vertical NPN and PNP transistors have large masking tolerances and thus their packing density is lower than desirable.

In accordance with the present invention there is provided a method of manufacturing a double-diffused, lateral transistor structure comprising the steps of:

- a. oxidizing a P-type silicon substrate;
- b. forming an opening in the silicon dioxide layer formed by step (a);
- c. forming a buried layer using an N⁺-type predeposition in the portion of the substrate exposed by said opening;
- d. removing the remaining silicon dioxide formed by step (a) from the surface of said substrate;
- e. epitaxially forming a layer of P-type conductivity on said substrate;
- f. forming a masking layer on the surface of said P-type epitaxial layer;
- g. removing said masking layer from said surface of said P-type epitaxial layer except over a portion of the active transistor structure to be formed;
- h. oxidizing the surface of the remaining exposed epitaxial layer to form an impurity-diffusion masking layer;
- i. defining a base diffusion opening in the silicon dioxide material formed by step (h);
- j. predepositing an N-type impurity in said epitaxial layer through said base diffusion opening;
- k. removing the remaining silicon dioxide material formed by step (h);
- l. applying a thermal oxidation masking material over said active transistor structure to be formed;
- m. etching the portion of said epitaxial layer not covered by said thermal oxidation masking material to approximately one-half its depth;
- n. oxidizing said etched portion of said epitaxial layer so that the surface of the resulting isolation-forming, thermally grown silicon dioxide corresponds approximately to the plane of the original surface of said epitaxial layer and so that said predeposited N-type impurities diffuse to form a base region meeting said buried layer;
- o. removing said thermal oxidation masking material applied by step (l);
- p. reoxidizing said epitaxial layer to form a thin protective silicon dioxide layer;
- q. defining said protective silicon dioxide layer formed by step (p) to form emitter and collector contact openings;
- r. forming with a P-type impurity in said epitaxial layer through said emitter and collector contact openings emitter and collector contact regions, said emitter region stopping short of the diffusion front associated with said base region; and
- s. forming metal contacts for electrical connection to said emitter, base and collector regions.

The method of the invention will be readily understood from the following illustrative description and accompanying drawings, in which:

Figs. 1A and 1B show a double-diffused

lateral transistor structure made using a method, which is not by itself in accordance with the invention, but is included to facilitate the understanding and a typical concentration profile for this transistor, respectively;

Figs. 2 and 3 show cross-sectional and top views, respectively, of a second structure made using the method, comprising a double-diffused, lateral transistor structure fabricated utilizing oxide isolation and a self-aligning mask together with a photoresist mask used for forming the emitter;

Fig. 4 shows means for making top side electrical contact with the base region of a structure made by the method;

Fig. 5A shows a third structure made using a method, which is not by itself in accordance with the invention, but is included to facilitate its understanding, wherein complementary PNP/NPN transistors are formed within the same isolation area;

Fig. 5B shows schematically the circuit represented by the structure of Fig. 5A;

Fig. 5C shows a structure utilizing a plurality of the structure referred to in Fig. 5A;

Figs. 6A to 6F refer to a method of manufacturing a non-oxide isolated, lateral, double-diffused PNP transistor structure, which is not by itself in accordance with the invention, but is included to facilitate understanding of the description relating to Figs. 7A to 7I; and

Figs. 7A to 7I show schematically a method embodying this invention by which a transistor may be formed.

Fig. 1A shows a double-diffused, lateral transistor structure 11. Semiconductor material 12 having a substantially flat surface 13 is subdivided into regions of active and passive material by insulating material 16. Insulating material 16 (of which cross-sections 16a and 16b are shown) is typically formed by removing part of the semiconductor material 12 overlying the field of the semiconductor device, and oxidizing the remaining semiconductor material as disclosed in the above-mentioned U. S. Patent No. 3,648,125. However, other techniques may also be used to form insulating material 16. Insulating material 16 is an integral part of the structure 11. The top surface of insulating material 16 is substantially coplanar with the top surface 13 of semiconductor material 12.

A collector region 17 is formed adjacent to both the flat surface and a portion of insulating material 16. A base region 22 is formed in this collector region 17 by diffusion. Emitter region 19 is formed in base region 22 adjacent another portion of

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insulating material 16 and adjacent surface 13.
Each of the emitter 19, base 22 and collector 17 regions is adjacent the flat surface 13, and the base region 22 separates the emitter region 19 from the collector region 17. Insulating region 16 serves to partially isolate the active region of the transistor 11 shown in Fig. 1A from any other active devices formed to semiconductor material 12. Regions 16a and 16b form a continuous closed path abutting surface 13 and surrounding the active region of transistor 11 but leaving exposed the top surface of the active region. In addition, in some situations semiconductor material 12 will extend beneath insulation 16 to contact the bottom portions of other active regions formed in material 12.
Fig. 1B shows a concentration profile for the transistor structure 11 shown in Fig. 1A. The concentration level 28 of a collector 17 is shown as a horizontal line, while the impurity concentration of the base 22 is represented by line 29, and the impurity concentration of the emitter 19 by line 27. The emitter-base junction occurs at point 31 corresponding to concentration level C_{EB} and distance R_{EB} . The collector-base junction occurs at point 32 and corresponds to concentration level C_{CB} and distance R_{CB} . The distance W between R_{EB} and R_{CB} is known as the base width, while the slope of a straight line connecting points 31 and 32 is called the grade constant α and is defined as $\alpha = (C_{EB} - C_{CB})/W$. It is well known that reductions in W improve the high frequency performance of the transistor, as do increases in the grade constant for a given amount of impurity in the base region. Both of these effects improve the high frequency performance of lateral transistor structures over that heretofore obtained.
Fig. 2 shows a double-diffused lateral transistor structure fabricated utilizing Peltzer's isolation technique described in U. S. Patent 3,648,125 and a self-aligning mask. This lateral transistor structure is a PNP transistor.
Employing Peltzer's technique, an N+ type buried layer 53 is formed at a selected location in P- type substrate 51. Then a P- type epitaxial layer 52 is formed on substrate 51. Hereinafter, substrate 51 and any attached layers of material will be called wafer 50. The PN junction 53a between substrate 51 and N-type buried layer 53 terminates at field oxide isolation regions 55a and 55b. When reverse biased, this PN junction together with insulating material 55 forms a pocket in the wafer and isolates active devices within the pocket.
On the surface of P- type epitaxial layer 52

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is deposited a self-aligning mask 56. This mask prevents diffusion of impurities into P- type epitaxial material 52 throughout the regions it overlies. As will be discussed, however, active semiconductor devices may still be formed underneath mask 56 because impurities may diffuse laterally beneath its edges, for example, edge 57.
As shown in Fig. 2 the base region 58 and emitter region 59 of the lateral PNP transistor are formed by diffusing the N- type base 58 and the P-type emitter 59 laterally into the silicon epitaxial layer 52 beneath edge 57 of mask 56. Mask 56 may be formed from one or more materials; for example, a composite laminate layer of silicon nitride and silicon oxide (typically predominantly silicon dioxide). The choice of individual materials is based on several criteria. First, the mask materials or material must prevent the passage of, or "mask", impurities. Second, the mask material or materials must be electrically non-conductive at the interface with the semiconductor material. Third, the material or materials must resist etching in solutions used to etch compounds of semiconductor material formed by thermal oxidation. These mask materials need not be inert to the etching solution, but must only exhibit a substantially smaller etch rate than the oxide of the semiconductor material. Advantages provided by the mask 56 will be discussed in conjunction with Fig. 3.
The base width of the transistor in Fig. 2 is approximately equal to the difference in distance between the laterally diffused collector-base junction 58a and emitter-base junction 59a. This difference is a function of process parameters and, in general, may be accurately controlled in a well known manner. The effective emitter-base junction area of the semiconductor device is proportional to (1) the depth of emitter-base junction 59a, and (2) the length "e" (see Fig. 3) of that portion of the mask edge 57 under which some of the emitter and base impurities travel, that is, the dimension perpendicular to the plane of the cross-section shown in Fig. 2. A portion 521 (Fig. 2) of P- type epitaxial layer 52 serves as the collector of the PNP lateral transistor. Electrical contact to the collector 521 of the transistor may be made at any suitable location and is shown at 522 in Fig. 2. Emitter region 59 and base region 58 are terminated along isolation wall 541 which typically is formed at the same time isolation region 55 is formed.
Fig. 3 shows a top view of the double-diffused, lateral, oxide-isolated transistor shown in Fig. 2. The emitter region 59, base contact region 581, and collector contact region 522 are shown, surrounded at the

surface of wafer 50 by field oxide insulation 55. Note that a portion of oxide 55 separates base contact 581 from emitter region 59. In one embodiment self-aligning mask 56 is formed from several materials, including silicon nitride. A photoresist mask 61 is shown by a dashed line in Fig. 3 in position for formation of emitter region 59 and collector contact region 522. For diffusion of the emitter region 59 and collector contact region 522, the area within the dashed line is exposed to a mild hydrofluoric acid etch. This removes silicon oxide films from the surface of the silicon within the opening of photoresist mask 61 while not appreciably etching the self-aligning mask 56. The emitter region 59 and the collector contact region 522 are then formed in base region 58 and collector region 521, respectively (see Fig. 2).

The particular self-aligning capability discussed above makes the opening in the photoresist mask 61 expose both insulating material 55 and the mask 56. The locations of edges 57, 95 (Fig. 3) of mask 56 determine the locations of the base region 58 (Fig. 2), emitter region 59, and collector contact region 522. The dimensions and locations of these regions are not substantially dependent upon the position of the photoresist mask 61. Prior art devices typically depended upon accurate repositioning of photoresist masks to define the locations and sizes of the base and emitter regions. Unlike the prior art, mask 56 is not removed from the wafer 50 and then redeposited later in the manufacturing process. Thus it provides a self-aligning positional accuracy for formation of both the base and emitter regions of the transistor structure. When the base and emitter regions are formed, the positions of the collector-base junction 58a (Fig. 2) and emitter-base junction 59a (Fig. 2) are controlled by the impurity concentrations used in, and the duration of, the process used to form these regions. Mask 56 typically comprises silicon nitride, at least over its top surface.

Fig. 4 shows a double-diffused, lateral, oxide isolated transistor with provision for topside contact to base region 58. As shown in Fig. 4 from the top, emitter region 59 no longer extends the full length e of edge 57 (Fig. 3) but rather terminates part-way along the edge. Masking material 56 can be given an appendage 58b as shown in Fig. 4. Base region 58 is contacted through a window (not shown) in mask 58B. Emitter 59 and base 58 are shown separated by line 58c. Electrical contact with the emitter is made at region 59 and with the collector at region 521.

Fig. 5A shows a complementary PNP/NPN transistor structure formed

within the same isolation area. Both devices have graded base impurity concentrations. The PNP transistor structure includes emitter region 59, base region 58, and collector region 521. The NPN transistor structure includes emitter region 92, base regions 91, 521, and collector region 53. Note that the collector region 521 of the PNP transistor structure and base region 91 of the NPN transistor structure are common, as are the PNP base region 58 and the NPN collector region 53. Region 94 is the electrical contact for both the PNP base region 58 and the NPN collector region 53. Fig. 5B shows the transistor structure of Fig. 5A schematically.

The complementary PNP/NPN transistor structure of this form provides substantial advantages over the prior art. First, the complementary PNP/NPN structure allows very high packing densities because the addition of the NPN transistor consumes no extra space over that required for just the PNP transistor. This results directly from the formation of a part of the NPN base region 91 and formation of the NPN emitter region 92 approximately at the location which would be the PNP collector contact in a noncomplementary structure. This advantage can readily be seen by comparing Fig. 5A with Fig. 2. Another advantage of the complementary PNP/NPN structure is that it may be formed very simply once the PNP transistor structure is fabricated. Once the PNP structure is formed only one extra manufacturing operation is necessary, that of forming the PNP emitter region 92 and NPN collector region-PNP base region contact 94. Note that the NPN base region 91 is formed at the same time the PNP emitter region 59 is formed. During formation of the NPN base region 91 and NPN emitter region 92 the edge 95 of mask 56 will perform a self-aligning function similar to that described above in conjunction with edge 57 of mask 56.

A further advantage of the complementary PNP/NPN transistor structure is its compatibility for inclusion in semiconductor devices which utilize arrays of complementary transistors. The ease with which arrays of complementary PNP/NPN transistor structures may be formed is shown in Fig. 5C.

A portion of wafer 400 is shown on which a plurality of complementary PNP/NPN transistor structures are formed. In Fig. 5C, five pairs of complementary devices are shown for illustrative purposes only. Each of the devices shown in plan view in Fig. 5C has the cross-section shown in Fig. 5A. A typical embodiment according to this invention employing an array of complementary PNP/NPN transistors may

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In Fig. 5C the complementary transistor structures are formed at intersections of buried layers 53R—V with other regions formed in the wafer 400. Each of the buried layers 53R—V acts as a common PNP base-NPN collector. Also shown in Fig. 5C are the self-aligned mask 56, PNP emitter region 59, a metal contact 403 to the PNP emitter region 59, NPN emitter region 92, and a metal contact 405 to the NPN emitter region 92. Electrical contacts to other regions of the PNP/NPN complementary structure are not shown in Fig. 5C; however, they could be made at any suitable location on wafer 400. The five pairs of complementary transistor structures are thus formed approximately at the intersections of emitter regions 59, 92 with the top surface of the semiconductor material. The PNP base region and the NPN base region are not shown, however, they separate the PNP emitter and collector regions and the NPN emitter and collector regions.

Figs. 6A to 5F refer to a method of manufacturing a non-oxide isolated, lateral, double-diffused PNP transistor structure, which, although not by itself in accordance with the invention, is included to facilitate understanding of the description relating to Figs. 7A to 7I.

1. Oxidize a P-type silicon substrate wafer 51 to form a silicon dioxide impurity diffusion mask (Fig. 6A, layer 101).

2. Form an opening 100 in the silicon dioxide layer 101 where the buried N-type layer is desired.

3. Form the buried layer 53 using an N+ predeposition.

4. Remove the oxide 101 from the surface of the substrate 51.

5. Grow a P-type epitaxial layer (Fig. 6B, layer 52).

6. Form a mask 104 on the surface of P-type epitaxial layer 52. Mask 104 is comprised of material meeting the specifications set forth herein, and, in one embodiment is silicon nitride.

7. Utilizing photo masking techniques, define openings in mask 104 which will be the emitter/base diffusion opening 105, the base contact opening 106, and the collector contact opening 107.

8. Oxidize the wafer to form a silicon dioxide film over the exposed silicon surface. This film will serve as an impurity diffusion mask (layers 108, 109, 110, Fig. 6B).

9. Form the emitter/base mask 111 using well known photoresist material. Note this is an oversize mask, that is, the edges of the mask do not define the openings discussed in step

7 above. Remove oxide 110, 108 from emitter/base region 105 and base contact region 106 (Fig. 6C).

10. Form the base region predeposition using N-type impurity (not shown).

11. Perform the base diffusion 112 (Fig. 6D) at an elevated temperature, thereby causing the base impurity to contact the N+ buried layer 53 (Fig. 6D). During this operation silicon dioxide films 113, 115, 116 are formed.

12. Form the emitter and collector mask 114 using well-known photoresist material. Note this is also an oversized mask. Remove the silicon dioxide 115, 116 shown in Fig. 6D.

13. Form the collector contact 117 and emitter 118 (Fig. 6E) predepositions and oxidize the wafer (layers 119, 120, 121 in Fig. 6E).

14. Remove oxide 119, 120, 121 to allow electric contact to be made to emitter region 118, base region 112A, and collector region 117.

15. Deposit and define metal contacts (122, Fig. 6F).

The above-described process uses one masking layer 104 to form the collector, base and emitter regions 52A, 112B and 118, respectively, of a lateral, double-diffused PNP transistor with a graded base. Isolation is provided by backbiasing the PN junction between P regions 51, 52 and N-type regions 112A, 112B and 53 (Fig. 6E). Buried layer 53 serves as a low resistance contact to base region 112B. Of interest, if the cross-section shown in Fig. 6F is rotated 360 degrees about a vertical line through the centre of the emitter region, a circular structure is obtained with the emitter at the centre, surrounded by the base region which in turn is surrounded by the collector region. The low resistivity buried N region underlies the structure and a circular base sink region surrounds the collector. In other words, the cross-section shown in Fig. 6F to the left of a vertical centerline through the centre of the emitter region represents the cross-section of one half of a disk-shaped structure.

A method of manufacturing a transistor, in accordance with the invention, will now be described with reference to Figs. 7A to 7I, the method using, in part, the process of Peltzer, referred to above, to form the isolation regions. This method results in a double-diffused, lateral, oxide-isolated PNP structure. The steps of this method are as follows:

1. Follow steps 1—6 of the method just discussed with reference to Figs. 6A to 6F.

2. Remove mask 104 from everywhere on the surface of P-type epitaxial layer 52 except where the transistor structure is desired.

3. Oxidize the wafer to grow an impurity-diffusion masking layer 201 of silicon dioxide (Fig. 7A).

5 4. Mask the base region using a photoresist mask 205 which overlaps the mask 104. Remove the exposed silicon dioxide.

10 5. Remove mask 205. Form the base region 206 N-type predeposition into the exposed silicon surface (Figs. 7B, 7C).

6. Remove the thermal oxide 201 (Fig. 7C).

15 7. Deposit a second mask of a material with characteristics similar or identical to the material of mask 104, i.e., silicon nitride (Fig. 7C, layer 207).

20 8. Using photomasking techniques, defined mask 207 into islands as described be Peltzer in the above-mentioned U. S. Patent (Fig. 7D is a top view, while 7E is a cross-sectional view).

25 9. Etch the exposed silicon to a depth approximately equal to one-half the epitaxial layer 52 thickness using a solution which does not appreciably the mask 104 or mask 207 (See Fig. 7F).

30 10. Oxidize the silicon to the extent that the upper surface of silicon dioxide 208 corresponds substantially to the plane of the original silicon surface. The lower surface of the silicon dioxide film 208 should intersect the buried N⁺ layer 53. During this oxidation, N-type region 206 diffuses downward to meet the upward diffusing N⁺ buried layer 53 (Fig. 7G).

35 11. Remove mask 207 leaving mask 104 intact.

40 12. Reoxidize the wafer to grow a thin protective oxide layer 209 (Fig. 7H).

45 13. Use an oversized photoresist mask 212 to expose the silicon in emitter 210 and collector 211 contact regions. Etch through the layer 209 of the silicon dioxide (Fig. 7H).

50 14. Form with a P-type impurity emitter region 213 and collector contact regions 214. Remove the silicon dioxide 209 covering base contact region 206 (Fig. 7I).

55 15. Form metal contacts 216A, 216B and 216C (or contacts of any other suitable conductive material) for electrical connection to the emitter, base, and collector regions, respectively.

The resulting structure shown in cross-section in Fig. 7I, is similar to, and has the features and advantages of the structure shown in Fig. 2.

60 This invention has been described as using a mask of a material such as silicon nitride which etches at a different rate in a given etch than does silicon dioxide. However, instead of using silicon nitride for the mask such as mask 56 (Fig. 2), silicon dioxide formed to a greater thickness than the adjacent layers of silicon dioxide

formed on the device can be used as the mask. In this situation, mask 56 must be at least thick enough to allow the silicon dioxide an adjacent portions of the top surface of the wafer to be removed while still leaving a thick enough layer of silicon dioxide on the surface to mask the impurities to be diffused or otherwise placed in the underlying semiconductor material.

Attention is hereby drawn to our copending patent application 14326/74 (Serial No. 1470211) that is directed to a semiconductor device such as hereinbefore described.

WHAT WE CLAIM IS:—

1. A method of manufacturing a double-diffused, lateral transistor structure comprising the steps of:

- a. oxidizing a P-type silicon substrate;
- b. forming an opening in the silicon dioxide layer formed by step (a);
- c. forming a buried layer using an N⁺-type predeposition in the portion of the substrate exposed by said opening;
- d. removing the remaining silicon dioxide formed by step (a) from the surface of said substrate;
- e. epitaxially forming a layer of P-type conductivity on said substrate;
- f. forming a masking layer on the surface of said P-type epitaxial layer;
- g. removing said masking layer from said surface of said P-type epitaxial layer except over a portion of the active transistor structure to be formed;
- h. oxidizing the surface of the remaining exposed epitaxial layer to form an impurity-diffusion masking layer;
- i. defining a base diffusion opening in the silicon dioxide material formed by step (h);
- j. predepositing an N-type impurity in said epitaxial layer through said base diffusion opening;
- k. removing the remaining silicon dioxide material formed by step (h);
- l. applying a thermal oxidation masking material over said active transistor structure to be formed;
- m. etching the portion of said epitaxial layer not covered by said thermal oxidation masking material to approximately one-half its depth;
- n. oxidizing said etched portion of said epitaxial layer so that the surface of the resulting isolation-forming, thermally grown silicon dioxide corresponds approximately to the plane of the original surface of said epitaxial layer and so that said predeposited N-type impurities diffuse to form a base region meeting said buried layer;
- o. removing said thermal oxidation masking material applied by step (l);

3. Oxidize the wafer to grow an impurity-diffusion masking layer 201 of silicon dioxide (Fig. 7A).

4. Mask the base region using a photoresist mask 205 which overlaps the mask 104. Remove the exposed silicon dioxide.

5. Remove mask 205. Form the base region 206 N-type predeposition into the exposed silicon surface (Figs. 7B, 7C).

6. Remove the thermal oxide 201 (Fig. 7C).

7. Deposit a second mask of a material with characteristics similar or identical to the material of mask 104, i.e., silicon nitride (Fig. 7C, layer 207).

8. Using photomasking techniques, defined mask 207 into islands as described be Peltzer in the above-mentioned U. S. Patent (Fig. 7D is a top view, while 7E is a cross-sectional view).

9. Etch the exposed silicon to a depth approximately equal to one-half the epitaxial layer 52 thickness using a solution which does not appreciably the mask 104 or mask 207 (See Fig. 7F).

10. Oxidize the silicon to the extent that the upper surface of silicon dioxide 208 corresponds substantially to the plane of the original silicon surface. The lower surface of the silicon dioxide film 208 should intersect the buried N+ layer 53. During this oxidation, N-type region 206 diffuses downward to meet the upward diffusing N+ buried layer 53 (Fig. 7G).

11. Remove mask 207 leaving mask 104 intact.

12. Reoxidize the wafer to grow a thin protective oxide layer 209 (Fig. 7H).

13. Use an oversized photoresist mask 212 to expose the silicon in emitter 210 and collector 211 contact regions. Etch through the layer 209 of the silicon dioxide (Fig. 7H).

14. Form with a P-type impurity emitter region 213 and collector contact regions 214. Remove the silicon dioxide 209 covering base contact region 206 (Fig. 7I).

15. Form metal contacts 216A, 216B and 216C (or contacts of any other suitable conductive material) for electrical connection to the emitter, base, and collector regions, respectively.

The resulting structure shown in cross-section in Fig. 7I, is similar to, and has the features and advantages of the structure shown in Fig. 2.

This invention has been described as using a mask of a material such as silicon nitride which etches at a different rate in a given etch than does silicon dioxide. However, instead of using silicon nitride for the mask such as mask 56 (Fig. 2), silicon dioxide formed to a greater thickness than the adjacent layers of silicon dioxide

formed on the device can be used as the mask. In this situation, mask 56 must be at least thick enough to allow the silicon dioxide on adjacent portions of the top surface of the wafer to be removed while still leaving a thick enough layer of silicon dioxide on the surface to mask the impurities to be diffused or otherwise placed in the underlying semiconductor material.

Attention is hereby drawn to our copending patent application 14326/74 (Serial No. 1470211) that is directed to a semiconductor device such as hereinbefore described.

WHAT WE CLAIM IS:—

1. A method of manufacturing a double-diffused, lateral transistor structure comprising the steps of:

- a. oxidizing a P-type silicon substrate;
- b. forming an opening in the silicon dioxide layer formed by step (a);
- c. forming a buried layer using an N+ type predeposition in the portion of the substrate exposed by said opening;
- d. removing the remaining silicon dioxide formed by step (a) from the surface of said substrate;
- e. epitaxially forming a layer of P-type conductivity on said substrate;
- f. forming a masking layer on the surface of said P-type epitaxial layer;
- g. removing said masking layer from said surface of said P-type epitaxial layer except over a portion of the active transistor structure to be formed;
- h. oxidizing the surface of the remaining exposed epitaxial layer to form an impurity-diffusion masking layer;
- i. defining a base diffusion opening in the silicon dioxide material formed by step (h);
- j. predepositing an N-type impurity in said epitaxial layer through said base diffusion opening;
- k. removing the remaining silicon dioxide material formed by step (h);
- l. applying a thermal oxidation masking material over said active transistor structure to be formed;
- m. etching the portion of said epitaxial layer not covered by said thermal oxidation masking material to approximately one-half its depth;
- n. oxidizing said etched portion of said epitaxial layer so that the surface of the resulting isolation-forming, thermally grown silicon dioxide corresponds approximately to the plane of the original surface of said epitaxial layer and so that said predeposited N-type impurities diffuse to form a base region meeting said buried layer;
- o. removing said thermal oxidation masking material applied by step (l);



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cp (1);

7
p. reoxidizing said epitaxial layer to form
a thin protective silicon dioxide layer;
q. defining said protective silicon dioxide
layer formed by step (p) to form emitter and
5 collector contact openings;
r. forming a P-type impurity in said
epitaxial layer through said emitter and
collector contact openings emitter and
collector contact regions, said emitter
10 region stopping short of the diffusion front
associated with said base region; and
s. forming metal contacts for electrical
connection to said emitter, base and
collector regions.
15 2. A method of manufacturing a double-
diffused, lateral transistor structure in
accordance with claim 1, wherein step (f)
comprises forming a silicon nitride mask
on the surface of said P-type epitaxial layer.
20 3. A method of manufacturing a double-

diffused, lateral transistor structure in
accordance with claim 1 or 2, wherein step
(1) comprises applying silicon nitride
masking material over said active tran-
sistor structure to be formed. 25
4. A double-diffused lateral transistor
structure manufactured in accordance with
any preceding claim.

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