WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of second interlayer insulating layers and a plurality of conductive patterns, alternately disposed under a first interlayer insulating layer;

a doped semiconductor layer over the first interlayer insulating layer;

a spacer pattern between the doped semiconductor layer and the first interlayer insulating layer;

a hole penetrating the spacer pattern, the first interlayer insulating layer, the plurality of second interlayer insulating layers, and the plurality of conductive patterns;

a memory pattern on a sidewall of the hole;

a core insulating pattern in a central region of the hole; and

a channel pattern between the core insulating pattern and the memory pattern,

wherein the doped semiconductor layer extends to the inside of the hole, and

wherein the semiconductor device further comprises a bit line, the channel pattern connects the bit line and the doped semiconductor layer.

2. The semiconductor memory device of claim 1, wherein the spacer pattern includes a semiconductor layer.

3. The semiconductor memory device of claim 2, wherein the spacer pattern includes single crystalline silicon.

4. The semiconductor memory device of claim 1, wherein the spacer pattern includes a material having an etch selectivity with respect to a semiconductor layer.

5. The semiconductor memory device of claim 4, wherein the spacer pattern includes at least one of a silicon carbide nitride (SiCN) layer and a silicon nitride (SiN) layer.

6. The semiconductor memory device of claim 1, wherein the doped semiconductor layer includes:

a horizontal pattern on the spacer pattern; and

a core pattern protruding to the inside of the hole toward the core insulating pattern from the horizontal pattern.

7. The semiconductor memory device of claim 6, wherein the doped semiconductor layer further includes a sidewall pattern extending along the sidewall of the hole toward the memory pattern from the horizontal pattern.

8. The semiconductor memory device of claim 7, wherein a conductive pattern, from the plurality of conductive patterns, that is

adjacent to the first interlayer insulating layer is a source select line, and

wherein an interface between the memory pattern and the sidewall pattern of the doped semiconductor layer is disposed at a level higher than a level at which the source select line is disposed.

9. The semiconductor memory device of claim 7, wherein the sidewall pattern of the doped semiconductor layer is shorter than the core pattern of the doped semiconductor layer.

10. The semiconductor memory device of claim 1, wherein the core insulating pattern includes a material having an etch selectivity with respect to the memory pattern.

11. The semiconductor memory device of claim 10, wherein the core insulating pattern includes a porous insulating material.

12. The semiconductor memory device of claim 1, wherein the channel pattern is in contact with the doped semiconductor layer, and includes a junction including the same conductivity type impurity as the doped semiconductor layer.

13. The semiconductor memory device of claim 1, wherein the first interlayer insulating layer is thicker than at least one of the plurality of second interlayer insulating layers.

14. The semiconductor memory device of claim 13, wherein the spacer pattern is thinner than the first interlayer insulating layer.

15. The semiconductor memory device of claim 1, wherein the spacer pattern is thicker than the first interlayer insulating layer.