INTEGRATED CIRCUITRY COMPONENTS, SWITCHES, AND MEMORY CELLS

RELATED PATENT DATA

[0001] This patent resulted from a divisional application of U.S. Patent Application No. 13/400,518, filed February 20, 2012, entitled "Integrated Circuitry Components, Switches, and Memory Cells", naming Gurtej S. Sandhu as inventor, the disclosure of which is incorporated by reference.

BACKGROUND

[0002] A switch is a component utilized to reversibly open and close a circuit. A switch may be considered to have two operational states, with one of the states being an "on" state and the other being an "off" state. Current flow through the switch will be higher in the "on" state that in the "off" state, and some switches may permit essentially no current flow in the "off" state. Switches may be utilized anywhere in an integrated circuit where it is desired to reversibly open and close a portion of the circuit.

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[0004] One type of memory cell is a so-called cross-point memory cell, which comprises programmable material between two electrically conductive electrodes. Numerous programmable materials are known which can be suitable for utilization in cross-point memory. For instance, phase change materials (such as, for example, various chalcogenides) may be utilized as programmable materials. Memory that utilizes phase change material as the programmable material is sometimes referred to as phase change random access memory (PCRAM). As another example, some programmable materials may utilize ions as mobile charge carriers to transition from one memory state to another. Such programmable materials may be incorporated into Resistive Random Access Memory (RRAM).

[0005] A difficulty in utilizing cross-point memory is that there can be substantial leakage of current through the cross-point memory cells, and such may adversely lead to errors during retrieval of stored data from a memory device. Accordingly, diodes or other select devices are commonly paired with the memory cells to assist in control of current through the memory cells. A switch can be a suitable select device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Fig. 1 is a diagrammatic, cross-sectional side view of an example embodiment of the invention.

[0007] Fig. 2 is a diagrammatic, three-dimensional view of an example embodiment graphene structure and ferroelectric material that may be utilized in the embodiment of Fig. 1.

[0008] Fig 3 is a diagrammatic, cross sectional view taken through line 3-3 in Fig. 1.

[0009] Fig. 4 is a diagrammatic, cross-sectional side view of an example embodiment of the invention.

[0010] Fig. 5 is a diagrammatic, cross-sectional side view of an example embodiment of the invention.

[0011] Fig. 6 is a diagrammatic, cross-sectional side view of an example embodiment of the invention.

[0012] Fig. 7 is a diagrammatic, cross-sectional side view of an example embodiment of the invention.

[0013] Fig. 8 is a diagrammatic, cross-sectional side view of an example embodiment of the invention.

[0014] Fig. 9 is a diagrammatic, cross-sectional side view of an example embodiment of the invention.

[0015] Fig. 10 is a diagrammatic, cross-sectional side view of an example embodiment of the invention.

[0016] Fig. 11 is a diagrammatic, cross-sectional side view of an example embodiment of the invention.

[0017] Fig. 12 is a diagrammatic, cross-sectional side view of an example embodiment of the invention.

[0018] Fig 13 is a diagrammatic, cross sectional view taken through line 13-13 in Fig. 12.

[0019] Fig. 14 is a graphical illustration of operational characteristics of an example embodiment.

[0020] Fig. 15 is a diagrammatic, cross-sectional side view of an example embodiment of the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0021] Some embodiments utilize graphene (for instance, bilayer graphene) as a current-conducting wire through a switch, and utilize an electric field transverse to the current-conducting wire to change a bandgap within the graphene. Increasing the bandgap turns the switch "off", and decreasing the bandgap turns the switch "on". Such switches may have very high current flow when the transverse electric field is low (or absent), since the graphene may, in some embodiments, have no effective bandgap in the absence of a sufficient transverse electric field to impart the bandgap. A relationship between a transverse electric field and the bandgap of bilayer graphene is described in several articles by Feng Wang (for instance, Zhang, et. al., Nature 459, 820-823 (11 June 2009)).

[0022] Another way of imparting a bandgap to graphene is to form the graphene be a strip having a narrow dimension (for instance, a dimension of less than or equal to about 20 nanometers, less than about 10 nanometers, or even less than or equal to about 5 nanometers). A relationship between graphene strip dimensions and bandgap is described in several articles by H. Dai (for instance, Li et. al., Science 319, 1229-1232 (2008)). In some embodiments, bilayer graphene within a switch may be formed to have each individual layer be a strip configured to have an inherent bandgap (i.e., a bandgap which is present even in the absence of any transverse electric field), which may provide additional control over current flow through the switch than can be achieved with graphene structures lacking an inherent bandgap.

[0023] Another way of imparting a bandgap to graphene is to form the graphene to be a strip having a narrow dimension (for instance, a dimension of less than or equal to about 20 nanometers, less than about 10 nanometers, or even less than or equal to about 5 nanometers). A relationship between graphene strip dimensions and bandgap is described in several articles by H. Dai (for instance, Li et. al., Science 319, 1229-1232 (2008)). In some embodiments, bilayer graphene within a switch may be formed to have each individual layer be a strip configured to have an inherent bandgap (i.e., a bandgap which is present even in the absence of any transverse electric field), which may provide additional control over current flow through the switch than can be achieved with graphene structures lacking an inherent bandgap.

[0024] A portion of an integrated circuit construction 10 is illustrated in Figs. 1-3, and includes an example component of integrated circuitry (e.g., a switch 12) supported by a base 14. Although the base is shown to be homogeneous, the base may comprise numerous components and materials in various embodiments. For instance, the base may comprise a semiconductor substrate supporting various materials and components associated with integrated circuit fabrication. Example materials that may be associated with the substrate include one or more of refractory metal materials, barrier materials, diffusion materials, insulator materials, etc. The semiconductor substrate may, for example, comprise, consist essentially of, or consist of monocrystalline silicon. The terms "semiconductive substrate," "semiconductor construction" and "semiconductor substrate" mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0025] Electrodes 16 and 18 comprise electrically conductive electrode material 20. Such electrode material may comprise any suitable electrically conductive composition, or combination of compositions; and may, for example, comprise one or more of various metals (for instance, tungsten, titanium, copper, etc.), metal-containing materials (for instance, metal silicide, metal carbide, metal nitride, etc.), and conductively-doped semiconductor materials (for instance, conductively-doped silicon, conductively-doped germanium, etc.). Although both of electrodes 16 and 18 are shown comprising the same electrically conductive material, in other embodiments electrodes 16 and 18 may comprise different conductive materials relative to one another.

[0026] A graphene structure 24 extends between the electrodes. The graphene structure may be referred to as extending longitudinally between the electrodes; with the term "longitudinally" being used to designate an orientation of the graphene structure to which other components may be compared. For instance, electrodes 16 and 18 may be considered to be spaced from one another along the longitudinal dimension of the graphene structure; and the graphene structure may be considered to have a thickness, "T", along a lateral dimension which extends orthogonally to the longitudinal dimension. The "longitudinal" dimension of the graphene structure may be any part of the graphene structure designated as such; and may or may not be the longest dimension of the graphene structure.

[0027] In the shown embodiment, graphene structure 24 extends across the space 22, and directly contacts both of electrodes 16 and 18. In some embodiments, the graphene structure will comprise more than one layer of graphene. For instance, the graphene structure may be a bilayer structure. A dashed-line 25 is shown within structure 24 to diagrammatically illustrate that such structure may comprise two layers of graphene in some embodiments. The layers may be the same thickness as one another, or may be different thicknesses relative to one another.

[0028] In operation, current flows along the graphene structure 24 between the electrodes 16 and 18 when the switch 12 is in an "on" state. Such current flow may be considered to be along the direction of an axis 27.

[0029] Switch 12 comprises a pair of first and second electrically conductive structures 26 and 28 (i.e., conductive nodes), with such conductive structures being laterally outward of graphene structure 24 and on opposing sides of graphene structure 24 in the shown embodiment. Conductive structures 26 and 28 comprise electrically conductive material 30. Such electrically conductive material may comprise any suitable composition, including any of the compositions described above with reference to electrodes 16 and 18. Although first and second conductive structures 26 and 28 are shown comprising a same composition as one another, in other embodiments the conductive structures may comprise different compositions relative to one another.

[0030] First and second conductive structures 26 and 28 are connected to circuitry 32 and 34, respectively, with such circuitry being configured to generate an electric field (EF) between the conductive structures. Such electric field is transverse to a direction of current flow along graphene structure 24. Although the electric field is illustrated as being oriented from electrode 28 toward electrode 26, the electric field may be oriented in an opposite direction in other embodiments. The field EF may be comprised by an electric field that is primarily orthogonal to the graphene structure (as shown), or may be comprised by an electric field that is primarily at an angle other than orthogonal to the graphene structure. If an electric field is primarily at an angle other than parallel to the direction of current flow along the graphene structure (i.e., a direction other than along axis 27), such electric field will have a vector component that corresponds to the illustrated field EF which is transverse to the direction of current flow along graphene structure 24. Thus, the generation of an electric field that is directed primarily along any direction other than parallel to axis 27 may be considered to comprise generation of an electric field transverse to the direction of current flow along graphene structure 24. It is noted that an electric field component along axis 27 (i.e., parallel to a direction of current flow along graphene structure 24) may be useful to assist in moving electrons from electrode 16 to 18, or vice versa, in the "on" state of switch 12.

[0031] First and second conductive structures 26 and 28 may be considered together as an electrical component configured to alter a bandgap within graphene of the graphene structure 24. Specifically, the electric field generated between the

conductive structures may alter the bandgap within graphene of the graphene structure 24 by taking advantage of the relationship described by Feng Wang.

[0032] Manipulation of the magnitude of the electric field transverse to current flow within the graphene structure 24 may be used to control the state of switch 12. A relatively high transverse electric field may be utilized to maintain switch 12 in an "off" state, while a relatively low transverse electric field may be utilized to maintain switch 12 in an "on" state. The terms "relatively high transverse electric field" and "relatively low transverse electric field" are utilized to indicate that the transverse electric fields are low and high relative to one another. In some embodiments, the total voltage differential between first and second conductive structures 26 and 28 may be changed by about 0.25 eV to transition the switch from the "on" state to the "off" state, or vice versa. In some embodiments, the transition from the "on" state to the "off" state may be achieved by providing a transverse electric field of less or equal to about 3 volts/nanometer, and in some embodiments may be achieved by providing a transverse electric field of less or equal to about 2 volts/nanometer.

[0033] Graphene structure 24 has a length "L" from electrode 16 to electrode 18, and the thickness "T" along a direction orthogonal to the length. The length and thickness of the graphene structure may be tailored to achieve desired performance characteristics; and additionally the spacing between first and second conductive structures 26 and 28, and the direction of the electric field generated between such conductive structures, may be tailored to achieve desired performance characteristics.

[0034] In some embodiments, graphene structure 24 will have a maximum overall lateral thickness between first and second conductive structures 26 and 28 of from about 1 nanometer to about 10 nanometers. In some embodiments, the graphene structure will comprise two or more layers, and at least one of the layers will have a maximum lateral thickness between the conductive structures of less than about 5 nanometers; and in some embodiments all of such layers will have a maximum lateral thickness between the conductive structures of less about 5 nanometers. In some embodiments, the individual layers of graphene will have maximum lateral thicknesses within a range of from about 1 nanometer to about 5 nanometers. Thickness "T" may be uniform or may be non-uniform along length "L". Regardless, in some embodiments, graphene structure 24 will have a length "L" within a range of from at least about 10 nanometers to at least about 50 nanometers.

[0035] In some embodiments, graphene structure 24 may be rectangular-shaped. An example rectangular-shaped graphene structure is shown in Figs. 1-3. Such

structure has length "L" and thickness "T" discussed above, and in addition has a width "W". The width may be tailored, in addition to the thickness and length, to achieve desired bandgap characteristics in the graphene, and desired performance characteristics of switch 12 (Figs. 1 and 3). In some embodiments, graphene structure 24 will have a width "W" of from at least about 5 nanometers to at least about 20 nanometers.

[0036] Graphene structure 24 may be configured relative to the electric field "EF" of switch 12 of Figs. 1 and 3 so that the electric field extends primarily along thickness "T" of the graphene structure (as shown in Fig. 1), or may be rotated relative to the configuration of Fig. 1 so that the electric field extends primarily along the width "W" of the graphene structure, or may be rotated so that the electric field extends through the graphene structure along a primary direction which is angled relative to both the thickness and the width of the graphene structure.

[0037] In some embodiments, graphene structure 24 may comprise two or more graphene layers which are dimensionally configured to take advantage of the relationship described by H. Dai so that the graphene has an inherent bandgap in the absence of a transverse electric field. Such can provide an additional parameter to tailor the conductivity of the "on" state mode of switch 12 for particular applications. In other embodiments, graphene structure 24 may comprise one or more layers which all individually have dimensions too large for a significant bandgap to be within the graphene of the structure 24 in the absence of an applied transverse electric field. Such can enable the graphene structure to have very high conductance in the "on" state mode of the switch.

[0038] Ferroelectric material is laterally between the graphene structure and at least one of the first and second electrically conductive structures. The ferroelectric material may be homogenous or non-homogenous. Further, any existing or yet-to-be-developed ferroelectric material may be used, with a lithium niobate (e.g., $LiNbO_3$) being one example. In a switch, application of an electric field across the graphene structure and the ferroelectric material is used to provide the switch into "on" and "off" states. Figs. 1-3 depict an example embodiment wherein ferroelectric material is laterally between the graphene structure and only one of the first and second electrically conductive structures on one of the opposing sides. Specifically, ferroelectric material 31 is laterally between graphene structure 24 and first conductive structure 26. In one embodiment, the ferroelectric material on the at least one side of the graphene structure has a minimum lateral thickness of from about 1 nanometer to about 10 nanometers, and in one embodiment from about 3 nanometers

to about 5 nanometers. In some embodiments, the ferroelectric material on the at least one side of the graphene structure has minimum and/or maximum lateral thickness which is/are less than that of the graphene of the graphene structure. The ferroelectric material need not be of constant lateral thickness, although constant lateral thickness is shown in Figs. 1-3.

[0039] In one embodiment, the ferroelectric material is longitudinally continuous between electrode 16, 18, and in one embodiment spans at least about 50% of the distance (i.e., dimension "L") between electrodes 16 and 18. In one embodiment, the ferroelectric material is directly against at least one of the pair of electrodes, with ferroelectric material 31 in Figs. 1-3 being directly against both of electrodes 16 and 18. Figs 1-3 also show an example embodiment wherein ferroelectric material 31 is coextensive with the graphene of graphene structure 24 along dimensions "L" and "W".

[0040] A dielectric material 40 is shown within the space between electrodes 16 and 18, and surrounding first and second conductive structures 26 and 28. Dielectric material 40 may comprise any suitable composition or combination of compositions, and in some embodiments may comprise one or more of silicon dioxide, silicon nitride, and any of various doped glasses (for instance, borophosphosilicate glass, phosphosilicate glass, fluorosilicate glass, etc.). Although the dielectric material 40 is shown to be homogeneous throughout switch 12, in other embodiments multiple different dielectric materials may be utilized.

[0041] Fig. 4 depicts an alternate integrated circuit construction 10a wherein ferroelectric material is laterally between the graphene structure and both of the first and second electrically conductive structures on the opposing sides of the graphene structure. Like numerals from the above described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "a" or with different numerals. Switch 12a comprises ferroelectric material 31 between graphene structure 24 and first conductive structure 26 as well as ferroelectric material 33 between graphene structure 24 and second conductive structure 28. Ferroelectric material 33 may be homogenous or non-homogenous, and may be of the same composition as ferroelectric material 31 or be of different composition from that of ferroelectric material 31. Ferroelectric materials 31 and 33 may be everywhere spaced from each other or may be directly against one another, for example contacting on another at one or both end edges (not shown) of graphene structure 24.

[0042] Fig. 4 depicts an alternate integrated circuit construction 10a wherein ferroelectric material is laterally between the graphene structure and both of the first and second electrically conductive structures on the opposing sides of the graphene structure. Like numerals from the above described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "a" or with different numerals. Switch 12a comprises ferroelectric material 31 between graphene structure 24 and first conductive structure 26 as well as ferroelectric material 33 between graphene structure 24 and second conductive structure 28. Ferroelectric material 33 may be homogenous or non-homogenous, and may be of the same composition as ferroelectric material 31 or be of different composition from that of ferroelectric material 31. Ferroelectric materials 31 and 33 may be everywhere spaced from each other or may be directly against one another, for example contacting one another at one or both end edges (not shown) of graphene structure 24.

[0043] Likewise where ferroelectric material is laterally between the graphene structure and both of the first and second electrically conductive structures, the ferroelectric material on each side may or may not be directly against graphene of the graphene structure. Fig. 4 depicts an example embodiment where ferroelectric material 31 and ferroelectric material 33 are both directly against graphene of graphene structure 24. Fig. 6 depicts an alternate example embodiment integrated circuit construction 10c having switch 12c with each of ferroelectric material 31 and ferroelectric material 33 being everywhere laterally spaced from graphene of graphene structure 24. Like numerals from the above described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "c" or with different numerals.

[0044] Fig. 7 depicts another example embodiment integrated circuit construction 10d having switch 12d with ferroelectric material 31 being everywhere spaced from graphene of graphene structure 24 and ferroelectric material 33 being directly against the graphene of graphene structure 24. Like numerals from the above described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "d" or with different numerals. Alternately as another example, ferroelectric material 31 may be directly against the graphene of graphene structure 34 and ferroelectric material 33 may be everywhere spaced from the graphene of graphene structure 34 (not shown). Regardless, where one or both of ferroelectric materials 31 and 33 are directly against the graphene, such does not need to be coextensive or completely against all of the graphene. Where ferroelectric material is everywhere laterally spaced from the graphene, in one embodiment such minimum spacing is no more than about 1 nanometer, and in one embodiment no more than about 0.5 nanometer.

[0045] Fig. 7 depicts another example embodiment integrated circuit construction 10d having switch 12d with ferroelectric material 31 being everywhere spaced from graphene of graphene structure 24 and ferroelectric material 33 being directly against the graphene of graphene structure 24. Like numerals from the above described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "d" or with different numerals. Alternately as another example, ferroelectric material 31 may be directly against the graphene of graphene structure 24 and ferroelectric material 33 may be everywhere spaced from the graphene of graphene structure 24 (not shown). Regardless, where one or both of ferroelectric materials 31 and 33 are directly against the graphene, such does not need to be coextensive or completely against all of the graphene. Where ferroelectric material is everywhere laterally spaced from the graphene, in one embodiment such minimum spacing is no more than about 1 nanometer, and in one embodiment no more than about 0.5 nanometer.

[0046] The above Figs. 1-8 embodiments show examples wherein the ferroelectric material is longitudinally continuous between electrodes 16 and 18. Alternately, the ferroelectric material may be longitudinally discontinuous between electrodes 16 and 18, for example as shown in Fig. 9 with respect to integrated circuit construction 10f having switch 12f. Like numerals from the above described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "f" or with different numerals. Fig. 9 shows two longitudinally spaced segments of ferroelectric material 31f which are spaced from conductive electrodes 16 and 18. Alternately, one or both of longitudinally spaced segments 31f may be received directly against electrode 16 and/or electrode 18 (not shown in Fig. 9). For example, Fig. 10 depicts an alternate example integrated circuit construction 10g having switch 12g wherein two ferroelectric material segments 31g are each against one of electrode 16 or 18. Like numerals from the above described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "g" or with different numerals.

[0047] Fig. 11 depicts an alternate example embodiment integrated circuit construction 10h with switch 12h wherein more than two (e.g., three) longitudinally spaced segments of ferroelectric material 31h have been used. Like numerals from the above described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "h" or with different numerals.

[0048] Any one or more of the above attributes with respect to ferroelectric material, whether on one or both sides of graphene structure 24, may be used or combined in any possible combination(s) as might be selected by the artisan to achieve any desired effect of a residual electrical field against graphene structure 24 applied by an appropriate polarization and charging of the ferroelectric material. For

example, the ferroelectric material may be directly against or everywhere spaced from the graphene of graphene structure 24.

[0049] First and second conductive structures 26 and 28 may be connected to any suitable circuitry 32, 34 to enable the transverse electric field to be generated across the ferroelectric material and graphene structure 24. In some embodiments, the first conductive structure may be conductively coupled to one of electrodes 16 and 18 and the second conductive structure may be conductively coupled to the other of electrodes 16 and 18. Examples of such embodiments are described with reference to an integrated circuit construction 10i shown in Figs. 12 and 13. Like numerals from the above described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "i" or with different numerals. Construction 10i comprises switch 12i analogous to the switch 12 described above with reference to Figs. 1-3, but comprising a first conductive projection 42 and a second conductive projection 44 extending from electrodes 16 and 18, respectively. First projection 42 extends from electrode 16 and partially across the space 22 between the electrodes, and second projection 44 extends from electrode 18 and partially across the space 22 between electrodes. First and second conductive structures 26 and 28 are effectively comprised by portions of the projections 42 and 44 that vertically overlap one another in the illustrated configuration. In the shown embodiment, projections 42 and 44 comprise the same material 20 as electrodes 16 and 18. In other embodiments, either or both of projections 42 and 44 may comprise a different composition than the electrode that such projection extends from. In one embodiment, projections 42 and 44 comprise conductive structures that project orthogonally from a respective one of electrodes 16 and 18.

[0050] Any attribute, or any combination of more than one of the above attributes, described and shown with respect to the ferroelectric material in Figs. 1-11 may be utilized in the embodiment of Figs. 12 and 13. Regardless, in operation, switch 12i may be considered to have at least three different operational modes.

[0051] In a first mode, there is no voltage differential between electrodes 16 and 18. Accordingly, electrodes 16 and 18 apply no electric field (EF) across ferroelectric material 31 and graphene structure 24. Depending upon the polarization state and charge (if any) retained by ferroelectric material 31, some electric field may or may not be applied across graphene structure 24. Regardless, bandgap within graphene of the graphene structure 24 will thus be small. Yet, there will be no current flow within the graphene structure due to the lack of the voltage differential between electrodes 16 and 18.

[0052] In a second mode, a voltage differential is provided between electrodes 16 and 18, and such differential is small enough so that the switch remains in an "on" state. In other words, the electric field between first and second conductive structures 26 and 28 is kept small enough that a bandgap within graphene of graphene structure 24 does not increase to a level which would effectively stop current flow along structure 24. This includes additive effect, if any, applied by any electric field resulting from charge, if any, within the ferroelectric material. While switch 12i remains in the second mode, current flow along structure 24 may or may not increase proportionally to an increasing voltage differential between electrodes 16 and 18. The relationship of the current flow along structure 24 to the voltage differential between electrodes 16 and 18 will depend, at least in part, on the distance between projections 42 and 44, the compositions of the projections, the compositions of the dielectric material and ferroelectric material between the projections, whether ferroelectric material is on one or both sides of graphene structure 24, the dimensions and construction(s) of the ferroelectric material, composition of structure 24, and the dimension and orientation of the region of structure 24 between the projections. Any or all of such parameters may be tailored to achieve a desired relationship of the current flow along structure 24 to the voltage differential between the electrodes 16 and 18.

[0053] In a third mode, the voltage differential between electrodes 16 and 18 reaches a level that causes the switch to be in an "off" state. In other words, the electric field between first and second conductive structures 26 and 28, including additive effect (if any) from charge (if any) retained by ferroelectric material 31, becomes large enough to increase the bandgap of graphene within graphene structure 24 to a level which effectively stops current flow along structure 24.

[0054] In some embodiments, the current flow along structure 24 in the "off" state of the switch will be 0 milliamps. In other embodiments, the current flow along structure 24 in the "off" state may be a non-zero value, but such current flow will still be low relative to the current flow along the structure in the "on" state of the switch.

[0055] In some embodiments, the pulse shape of the voltage increase or decrease utilized to transition between the "on" and "off" states of a switch may be tailored for desired performance characteristics of the switch. In some embodiments, the rise time or fall time of the voltage change utilized to transition between the "on" and "off" states of a switch may be tailored for desired performance characteristics of the switch. In some embodiments, the switch may be tailored so that current flow along graphene structure 24 increases with an increasing voltage differential between

electrodes 16 and 18 while the switch remains in the "on" state, and then the current flow may abruptly cease when the voltage differential reaches a level which transitions the switch to the "off" state. In some embodiments, the switch may be tailored to gradually taper current flow along structure 24 during the transition of the switch from the "on" state to the "off" state.

[0056] Fig. 14 graphically illustrates operation of an example embodiment switch of the type shown in Figs. 12 and 13. Specifically, the solid graph line of Fig. 14 shows the current through the switch increasing with an initial increase in the voltage differential between electrodes 16 and 18 above a level of zero (V_0); then decreasing after the voltage differential reaches a transition level (V_{a1}), and finally ceasing altogether when the voltage differential reaches a level V_{b1}.

[0057] Ferroelectric material on one or both sides of the graphene structure may, in certain operational regimes, store charge in one state of polarization versus in another state of polarization. For example, an electric field applied through ferroelectric material by a suitable voltage differential between structures 26 and 28, or between projections 42 and 44, may be sufficient to polarize the ferroelectric material into a charge-storage capable state and/or actually store charge within the ferroelectric material in that charge-storage capable state. That electric field may be sufficient to transform graphene structure 24 from a longitudinally conducive state to a longitudinally resistive state. Removing the voltage differential from between the conductive structures/projections may leave a residual charge from the ferroelectric material that applies a residual electric field to the graphene structure. That residual electric field may facilitate maintaining the graphene structure in a longitudinally resistive state. Reversing the polarization may dissipate the charge and apply an electric field that places the graphene structure back into a longitudinally conductive state.

[0058] Ferroelectric material on one or both sides of the graphene structure may, in certain operational regimes, store charge in one state of polarization versus in another state of polarization. For example, an electric field applied through ferroelectric material by a suitable voltage differential between structures 26 and 28, or between projections 42 and 44, may be sufficient to polarize the ferroelectric material into a charge-storage capable state and/or actually store charge within the ferroelectric material in that charge-storage capable state. That electric field may be sufficient to transform graphene structure 24 from a longitudinally conductive state to a longitudinally resistive state. Removing the voltage differential from between the conductive structures/projections may leave a residual charge from the ferroelectric material that applies a residual electric field to the graphene structure. That residual electric field may facilitate maintaining the graphene structure in a longitudinally resistive state. Reversing the polarization may dissipate the charge and apply an electric field that places the graphene structure back into a longitudinally conductive state.

[0059] Presence of ferroelectric material on one or both sides of the graphene structure may enable a lower Va1 and/or Vb1 than would otherwise occur with an identical construction in the absence of ferroelectric material. As an example, the dashed graph line in Fig. 14 shows an example operational profile of the same construction switch in the absence of any ferroelectric material substituting for some of dielectric material 40. Such a construction is shown and described in the Appendix hereto, with the Appendix hereto hereby formally constituting part of this invention disclosure as if it appeared herein as separate or additional parts of the specification, claims, and drawings. Further, this invention disclosure encompasses use of any of the constructions herein in any of the constructions and methods of the Appendix. The Appendix is U.S. Patent Application Serial No. 13/050,630, as-filed, and having a filing date of March 17, 2011 (now U.S. Patent Publication No. 2012/0230128).

[0060] The switches described with respect to Figs. 12 and 13 comprise a single graphene structure 24. In other embodiments, switches may be configured to comprise two or more graphene structures. Fig. 15 shows an integrated circuit construction 10j having switch 12j which comprises two graphene structures. Like numerals from the above described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "j" or with different numerals.

[0061] Switch 12j comprises electrodes 16 and 18, graphene structure 24, ferroelectric material 31, and projections 42 and 44 discussed above relative to Figs. 12 and 13. Additionally, switch 12b comprises another graphene structure 48 on an opposite side of projection 44 from graphene structure 24, ferroelectric material 35, and another projection 50 extending upwardly from the electrode 16. Ferroelectric material 35 may have any of the attributes described above with respect to ferroelectric materials 33. Any one attribute, or any combination of more than one of the above attributes, described and shown with respect to the ferroelectric material in Figs. 1-11 may be utilized in the embodiment of Fig. 15.

[0062] Switch 12j comprises electrodes 16 and 18, graphene structure 24, ferroelectric material 31, and projections 42 and 44 discussed above relative to Figs. 12 and 13. Additionally, switch 12j comprises another graphene structure 48 on an opposite side of projection 44 from graphene structure 24, ferroelectric material 35, and another projection 50 extending upwardly from the electrode 16. Ferroelectric material 35 may have any of the attributes described above with respect to ferroelectric materials 33. Any one attribute, or any combination of more than one of the above attributes, described and shown with respect to the ferroelectric material in Figs. 1-11 may be utilized in the embodiment of Fig. 15.

[0063] A region of projection 44 vertically overlaps with regions of projections 42 and 50, and in operation first and second electric fields EF_1 and EF_2 may be generated between such vertically-overlapping regions (as shown). The electric fields are transverse to the direction that current is conducted through graphene structures

24 and 48, and may be utilized to control whether the switch is in an "on" state or an "off" state -- analogously to the utilization of the electric field EF of Fig. 12. Although the fields EF_1 and EF_2 are illustrated as being comprised by electric fields that are primarily orthogonal to the graphene structures, in other embodiments, one or both of the fields EF_1 and EF_2 may be a vector component of an electric field that extends primarily along a direction other than orthogonal the graphene structures. Also, although the graphene structures are shown to be substantially parallel to one another, in other embodiments they may not be. Regardless, switch 12b of Fig. 15 is an example of a configuration in which there are three projections for every two graphene structures.

[0064] A region of projection 44 vertically overlaps with regions of projections 42 and 50, and in operation first and second electric fields EF_1 and EF_2 may be generated between such vertically-overlapping regions (as shown). The electric fields are transverse to the direction that current is conducted through graphene structures 24 and 48, and may be utilized to control whether the switch is in an "on" state or an "off" state -- analogously to the utilization of the electric field EF of Fig. 12. Although the fields EF_1 and EF_2 are illustrated as being comprised by electric fields that are primarily orthogonal to the graphene structures, in other embodiments, one or both of the fields EF_1 and EF_2 may be a vector component of an electric field that extends primarily along a direction other than orthogonal to the graphene structures. Also, although the graphene structures are shown to be substantially parallel to one another, in other embodiments they may not be. Regardless, switch 12j of Fig. 15 is an example of a configuration in which there are three projections for every two graphene structures.

[0065] The embodiment of Fig. 15 may be manufactured with only one of ferroelectric materials 31 or 35 (not shown). Regardless in one embodiment, ferroelectric material is laterally between at least one of a) the overlapping regions of the first and second projections, and b) the overlapping regions of the second and third projections.

[0066] The embodiments described above with respect to Figs. 1-15 were primarily with respect to a component of integrated circuitry in the form of a switch or switches. However, any alternate existing or yet-to-be-developed component of circuitry may be fabricated. As but one example, the component of integrated circuitry might comprise a memory cell. For example, such a memory cell may comprise a graphene structure extending longitudinally between a pair of electrodes and which is conductively connected to both electrodes of the pair. First and second electrically conductive structures may be laterally outward of the graphene structure and on opposing sides of the graphene structure from one another. Ferroelectric material may be laterally outward of the graphene structure and laterally between the graphene structure and at least one of the first and second electrically conductive structures. The first and second electrically conductive structures may be configured to provide the memory cell into one of at least two memory states by application of an

electric field across the graphene structure and the ferroelectric material. Any one attribute, or any combination of more than one of the above attributes, described and/or shown with respect to Figs. 1-15 may be utilized in a memory cell embodiment of the invention.

[0067] Memory cells fabricated herein in accordance with the invention using ferroelectric material may enable use of lower read voltage and/or write voltage for the memory cell. Lower read voltage may be desirable to minimize risk of changing state of the memory cell during read operations, and which is commonly referred to as "read disturb". By way of example only, consider a manner of writing a "1" to any of memory cells 12, 12a, 12b, 12c, 12d, 12e, 12f, 12g, 12h, or 12i by application of zero voltage to conductive structure 28/projection 44 and a positive voltage "V" to conductive structure 26/projection 42. Consider that such is sufficient to polarize and store charge within the ferroelectric material, as well as to render the graphene structure(s) to be longitudinally non-conductive. Erasing back to a "0" state may occur by applying zero voltage to conductive structure 26/projection 42 and negative voltage "V" to conductive structure 28/projection 44. Regardless of being in a "0" or "1" state, the memory cell may be read by application of a voltage differential (positive or negative) of 1/3V between conductive structure 26/projection 42 and conductive structure 28/projection 44.

[0068] Memory cells of the invention may or may not use an individual select device with each individual memory cell in an array of memory cells. Regardless, a select device is a component of integrated circuitry that may be fabricated in accordance with the invention described herein. Regardless, where memory circuitry includes memory cells in accordance with the invention herein that include one or more select devices, those select devices may have a construction as described herein, as described in the Appendix, or some other existing or yet-to-be-developed construction.

[0069] The inventive components disclosed herein may be incorporated into integrated circuits suitable for utilization in any of numerous electronic systems. For instance, such integrated circuits may be suitable for utilization in one or more of clocks, televisions, cell phones, personal computers, automobiles, industrial control systems, aircraft, etc.

[0070] The particular orientation of the various embodiments in the drawings is for illustrative purposes only, and the embodiments may be rotated relative to the shown orientations in some applications. The description provided herein, and the claims that follow, pertain to any structures that have the described relationships

between various features, regardless of whether the structures are in the particular orientation of the drawings, or are rotated relative to such orientation.

[0071] The cross-sectional views of the accompanying illustrations only show features within the planes of the cross-sections, and do not show materials behind the planes of the cross-sections in order to simplify the drawings.

[0072] When a structure is referred to above as being "on" or "against" another structure, it can be directly on the other structure or intervening structures may also be present. In contrast, when a structure is referred to as being "directly on" or "directly against" another structure, there are no intervening structures present. When a structure is referred to as being "connected" or "coupled" to another structure, it can be directly connected or coupled to the other structure, or intervening structures may be present. In contrast, when a structure is referred to as being "directly connected" or "directly coupled" to another structure, there are no intervening structures present.

Conclusion

[0073] When a structure is referred to as being "on" or "against" another structure, it can be directly on the other structure or intervening structures may also be present. In contrast, when a structure is referred to as being "directly on" or "directly against" another structure, there are no intervening structures present. When a structure is referred to as being "connected" or "coupled" to another structure, it can be directly connected or coupled to the other structure, or intervening structures may be present. In contrast, when a structure is referred to as being "directly connected" or "directly coupled" to another structure, there are no intervening structures present.

[0074] In some embodiments, a component of integrated circuitry comprises a first electrode and a second electrode. The first and second electrodes are separated from one another by a space. A graphene structure is conductively connected to both of the first and second electrodes, and extends across the space. A first electrically conductive projection extends into the space from the first electrode, and extends only partially across the space. A second electrically conductive projection extends into the space from the second electrode, and extends only partially across the space. A region of the first projection overlaps a region of the second projection. The graphene structure is between the overlapping regions of the first and second projections. Ferroelectric material is laterally between the graphene structure and at least one of the first and second projections within the overlapping regions.

[0075] In some embodiments, a memory cell comprises a graphene structure extending longitudinally between a pair of electrodes and is conductively connected to both electrodes of said pair. First and second electrically conductive structures are laterally outward of the graphene structure and on opposing sides of the graphene structure from one another. Ferroelectric material is laterally outward of the graphene structure. The ferroelectric material is laterally between the graphene structure and at least one of the first and second electrically conductive structures. The first and second electrically conductive structures are configured to provide the memory cell into one of at least two memory states by application of an electric field across the graphene structure and the ferroelectric material.

[0076] In some embodiments, a component of integrated circuitry comprises a first electrode and a second electrode. The first and second electrodes are separated from one another by a space. First and second graphene structures are conductively connected to both of the first and second electrodes, and extend across the space. The first and second graphene structures are spaced-apart from one another by a gap. A first electrically conductive projection extends into the space from the first electrode, and extends only partially across the space. The first electrically conductive projection is on one side of the first graphene structure. A second electrically conductive projection extends into the space from the second electrode, and extends only partially across the space. The second electrode is between the first and second graphene structures, and is on an opposing side of the first graphene structure from the first electrically conductive projection. A third electrically conductive projection extends into the space from the first electrode, and extends only partially across the space. The third electrically conductive projection is on an opposing side of the second graphene structure from the second electrically conductive projection. A region of the first projection overlaps a region of the second projection. The first graphene structure is between the overlapping regions of the first and second projections. A region of the second projection overlaps a region of the third projection. The second graphene structure is between the overlapping regions of the second and third projections. Ferroelectric material is laterally between at least one of a) the overlapping regions of the first and second projections, and b) the overlapping regions of the second and third projections.

[0077] In some embodiments, a component of integrated circuitry comprises a first electrode and a second electrode. The first and second electrodes are separated from one another by a space. First and second graphene structures are conductively connected to both of the first and second electrodes, and extend across the space. The first and second graphene structures are spaced-apart from one another by a gap. A first electrically conductive projection extends into the space from the first electrode, and extends only partially across the space. The first electrically conductive projection is on one side of the first graphene structure. A second electrically conductive projection extends into the space from the second electrode, and extends only partially across the space. The second electrically conductive projection is between the first and second graphene structures, and is on an opposing side of the first graphene structure from the first electrically conductive projection. A third electrically conductive projection extends into the space from the first electrode, and extends only partially across the space. The third electrically conductive projection is on an opposing side of the second graphene structure from the second electrically conductive projection. A region of the first projection overlaps a region of the second projection. The first graphene structure is between the overlapping regions of the first and second projections. A region of the second projection overlaps a region of the third projection. The second graphene structure is between the overlapping regions of the second and third projections. Ferroelectric material is laterally between at least one of a) the overlapping regions of the first and second projections, and b) the overlapping regions of the second and third projections.

CLAIMS

1. A component of integrated circuitry, comprising:

a first electrode and a second electrode, the first and second electrodes being separated from one another by a space;

a graphene structure conductively connected to both of the first and second electrodes, and extending across the space;

a first electrically conductive projection extending into the space from the first electrode, and extending only partially across the space;

a second electrically conductive projection extending into the space from the second electrode, and extending only partially across the space;

a region of the first projection overlapping a region of the second projection; the graphene structure being between the overlapping regions of the first and second projections; and

ferroelectric material laterally between the graphene structure and at least one of the first and second projections within the overlapping regions.

2. The component of claim 1 wherein the component comprises a switch, the first and second electrically conductive projections being configured to provide the switch into "on" and "off" states by application of an electric field across the graphene structure and the ferroelectric material.

3. The component of claim 1 wherein the component comprises a memory cell, the first and second electrically conductive projections being configured to provide the memory cell into one of at least two memory states by application of an electric field across the graphene structure and the ferroelectric material.

4. A component of integrated circuitry, comprising:

a first electrode and a second electrode, the first and second electrodes being separated from one another by a space;

first and second graphene structures conductively connected to both of the first and second electrodes, and extending across the space; the first and second graphene structures being spaced-apart from one another by a gap;

a first electrically conductive projection extending into the space from the first electrode, and extending only partially across the space, the first electrically conductive projection being on one side of the first graphene structure;

a second electrically conductive projection extending into the space from the second electrode, and extending only partially across the space; the second electrode being between the first and second graphene structures, and being on an opposing side of the first graphene structure from the first electrically conductive projection;

a third electrically conductive projection extending into the space from the first electrode, and extending only partially across the space; the third electrically conductive projection being on an opposing side of the second graphene structure from the second electrically conductive projection;

a region of the first projection overlapping a region of the second projection; the first graphene structure being between the overlapping regions of the first and second projections;

a region of the second projection overlapping a region of the third projection; the second graphene structure being between the overlapping regions of the second and third projections; and

ferroelectric material laterally between at least one of a) the overlapping regions of the first and second projections, and b) the overlapping regions of the second and third projections.

5. The component of claim 1 wherein the ferroelectric material on one side of the graphene structure has a minimum lateral thickness which is less than that of the graphene of the graphene structure.

6. The component of claim 1 wherein the ferroelectric material on one side of the graphene structure has a maximum lateral thickness which is less than that of the graphene of the graphene structure.

7. The component of claim 1 wherein the ferroelectric material on one side of the graphene structure has a minimum lateral thickness of from about 1 nanometer to about 10 nanometers.

8. The component of claim 7 wherein the ferroelectric material on one side of the graphene structure has a minimum lateral thickness of from about 3 nanometers to about 5 nanometers.

9. The component of claim 1 wherein the ferroelectric material is directly against graphene of the graphene structure.

10. The component of claim 1 wherein ferroelectric material is laterally between the graphene structure and only one of the first and second electrically conductive structures on one of the opposing sides of the graphene structure.

11. The component of claim 1 wherein the ferroelectric material is longitudinally continuous between the pair of electrodes.

12. The component of claim 11 wherein the ferroelectric material spans at least about 50% of the distance between the pair of electrodes.

13. The component of claim 11 wherein the ferroelectric material is coextensive with the graphene of the graphene structure.

14. A memory cell comprising:

a base substrate;

a pair of electrodes supported above and by the base substrate, one of the electrodes being elevationally outward of the other of the electrodes relative to the base substrate;

a graphene structure extending longitudinally and vertically between the pair of elevationally spaced electrodes and being electrical conductively connected to both electrodes of said pair;

first and second electrically conductive structures supported above and by the base substrate laterally outward of the vertically extending graphene structure and on opposing sides of the vertically extending graphene structure, the first and second electrically conductive structures comprising elevational thicknesses that vertically overlap in a horizontal plane; and

vertically extending ferroelectric material laterally between the vertically extending graphene structure and at least one of the first and second electrically conductive structures, the first and second electrically conductive structures comprising circuitry to apply a voltage to the first electrically conductive structure that is different from an applied voltage to the second electrically conductive structure in the horizontal plane to provide the memory cell into one of at least two memory states by application of a programming electric field across the graphene structure and the ferroelectric material in the horizontal plane due to said different applied voltages which changes a polarization state of the ferroelectric material.

15. The memory cell of claim 14 wherein the ferroelectric material on one side of the graphene structure has a minimum lateral thickness which is less than that of the graphene of the graphene structure.

16. The memory cell of claim 14 wherein the ferroelectric material on one side of the graphene structure has a maximum lateral thickness which is less than that of the graphene of the graphene structure.

17. The memory cell of claim 14 wherein the ferroelectric material is directly against graphene of the graphene structure.

18. The memory cell of claim 14 wherein the ferroelectric material is everywhere spaced from graphene of the graphene structure.

19. The memory cell of claim 14 wherein the ferroelectric material is longitudinally continuous between the pair of electrodes.

20. The memory cell of claim 19 wherein the ferroelectric material spans at least about 50% of the distance between the pair of electrodes.

21. The memory cell of claim 14 wherein the ferroelectric material is longitudinally discontinuous between the pair of electrodes.

22. The memory cell of claim 21 wherein the ferroelectric material spans at least about 50% of the distance between the pair of electrodes.

23. The memory cell of claim 21 wherein the ferroelectric material comprises more than two longitudinally spaced segments.

24. A memory cell comprising:

a graphene structure extending longitudinally between a pair of electrodes and being electrical conductively connected to both electrodes of said pair;

first and second electrically conductive structures laterally outward of the graphene structure and on opposing sides of the graphene structure from one another, the first electrically conductive structure being electrical conductively connected to one of the electrodes and the second electrically conductive structure being electrical conductively connected to the other of the electrodes; and

ferroelectric material laterally between the graphene structure and at least one of the first and second electrically conductive structures, the first and second electrically conductive structures being configured to provide the memory cell into one of at least two memory states by application of an electric field across the graphene structure and the ferroelectric material.

25. A memory cell comprising:

a base substrate;

a pair of electrodes supported above and by the base substrate, one of the electrodes being elevationally outward of the other of the electrodes relative to the base substrate;

a graphene structure extending longitudinally and vertically between the pair of elevationally spaced electrodes and being electrical conductively connected to both electrodes of said pair, the graphene structure comprising two physically contacting layers of graphene;

first and second electrically conductive structures supported above and by the base substrate laterally outward of the vertically extending graphene structure and on opposing sides of the vertically extending graphene structure, the first and second electrically conductive structures comprising elevational thicknesses that vertically overlap in a horizontal plane; and

vertically extending ferroelectric material laterally between the vertically extending graphene structure and at least one of the first and second electrically conductive structures, the first and second electrically conductive structures being configured to provide the memory cell into one of at least two memory states by application of a programming electric field across the graphene structure and the ferroelectric material in the horizontal plane which changes a polarization state of the ferroelectric material.

26. A memory cell comprising:

at least two graphene structures extending longitudinally between a pair of electrodes and being electrical conductively connected to both electrodes of said pair, the two graphene structures being laterally spaced apart relative one another by solid dielectric material;

first and second electrically conductive structures laterally outward of the graphene structure and on opposing sides of the graphene structure from one another, the first and second electrically conductive structures comprising elevational thicknesses that vertically overlap in a horizontal plane; and

ferroelectric material laterally between the graphene structure and at least one of the first and second electrically conductive structures, the first and second electrically conductive structures comprising circuitry to apply a voltage to the first electrically conductive structure that is different from an applied voltage to the second electrically conductive structure in the horizontal plane to provide the memory cell into one of at least two memory states by application of an electric field across the graphene structure and the ferroelectric material in the horizontal plane due to said different applied voltages.