signal supplied to the initial stage is activated and (ii) ends at a time when an output of the final stage changes from activation to inactivation (or an operation period starts at a time when a shift start signal is activated and ends at a time when the final stage is reset); when the clock signal supplied to the first input terminal of the second intermediate stage is initially activated after the operation period starts, the clock signal supplied to the second input terminal of the second intermediate stage is inactive.

By providing the setting circuit in the second intermediate stage, it is possible to prevent malfunction of the second intermediate stage even in a case where the clock signal supplied to the second input terminal of the second intermediate stage is inactive when the clock signal supplied to the first input terminal of the second intermediate stage is initially activated after the operation period starts.

There is also provided a driver circuit comprising the above shift register and a control line via which the control signal is supplied; a first clock line via which the clock signal is supplied to the first input terminal; and a second clock line via which the clock signal is supplied to the second input terminal.

Advantageous Effects of Invention

It is possible to prevent malfunction of a shift register in which a plurality of clock signals are supplied to each stage.

Brief Description of Drawings

Fig. 1 is a circuit diagram illustrating a unit stage of a shift register of Example 1.

Fig. 2 is a block diagram illustrating an example