

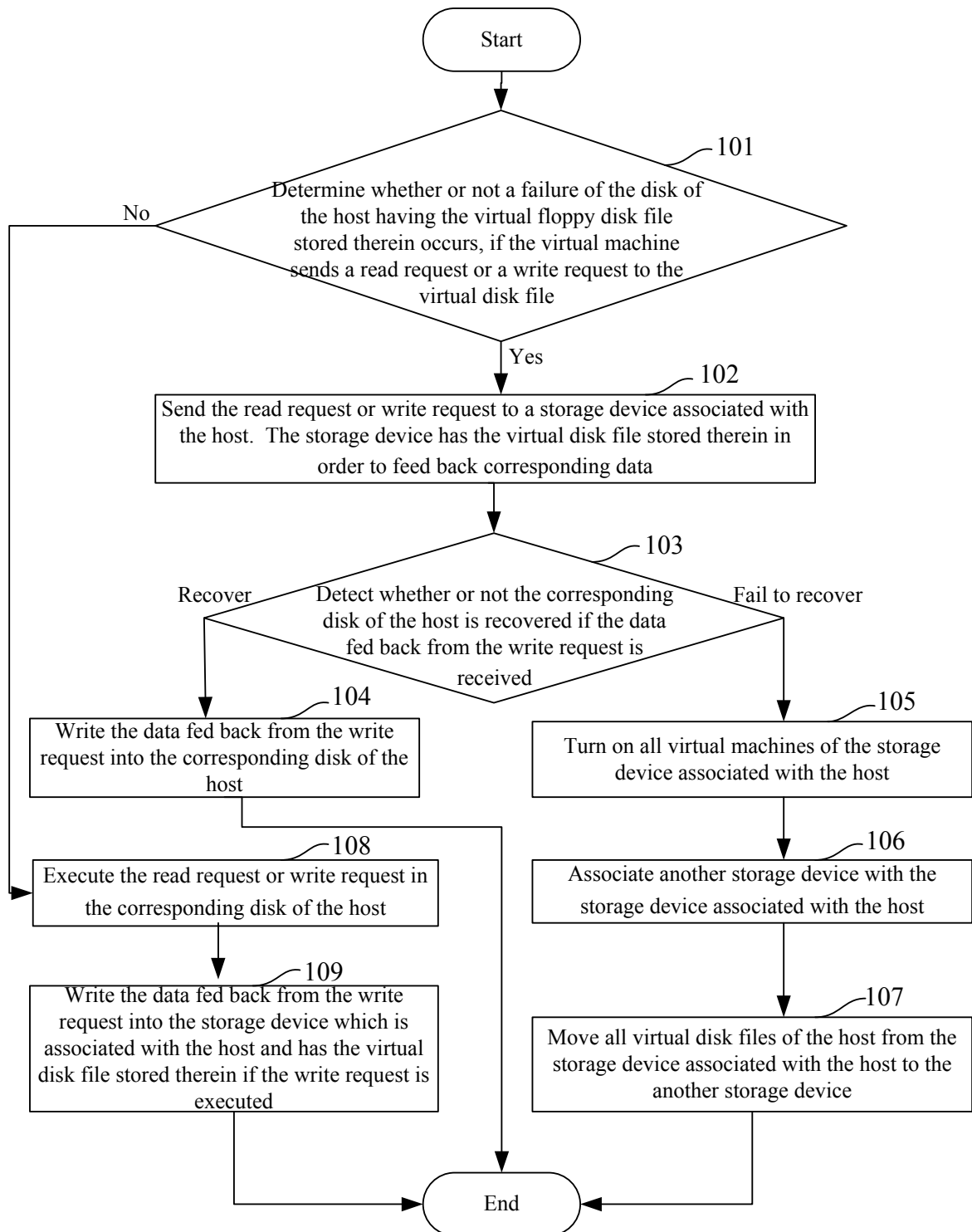


FIG. 1

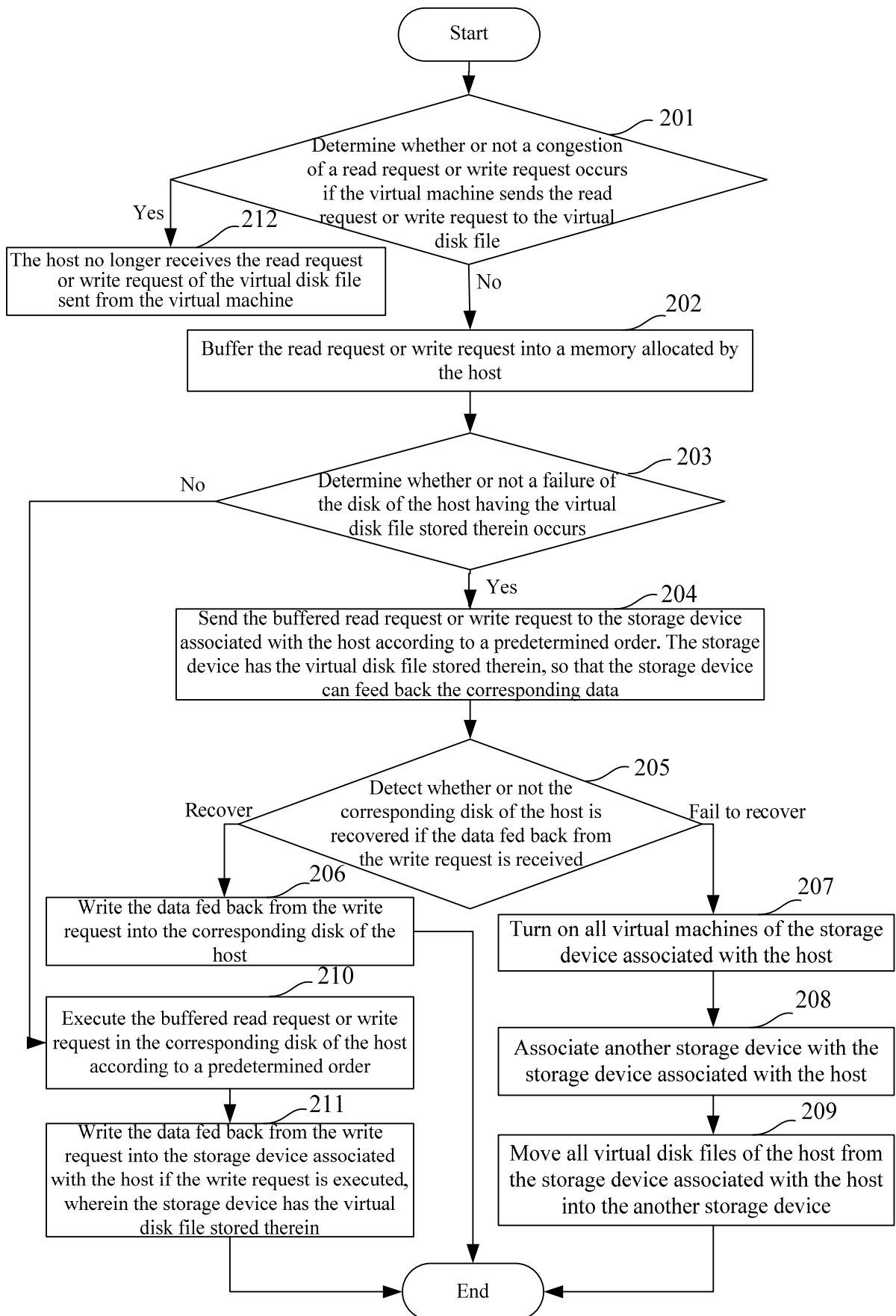


FIG. 2

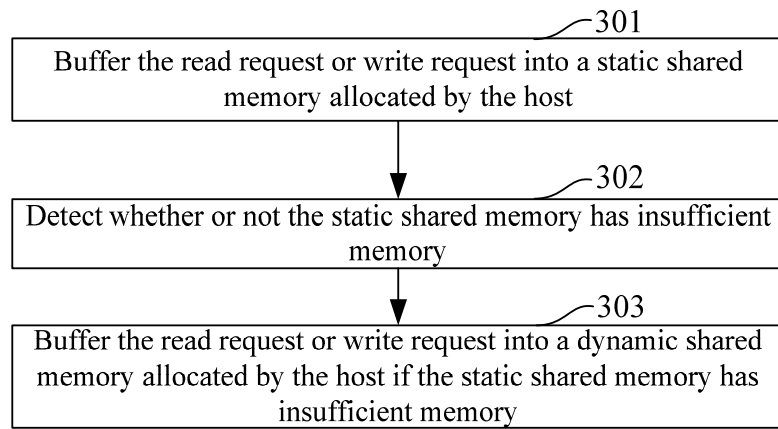


FIG. 3

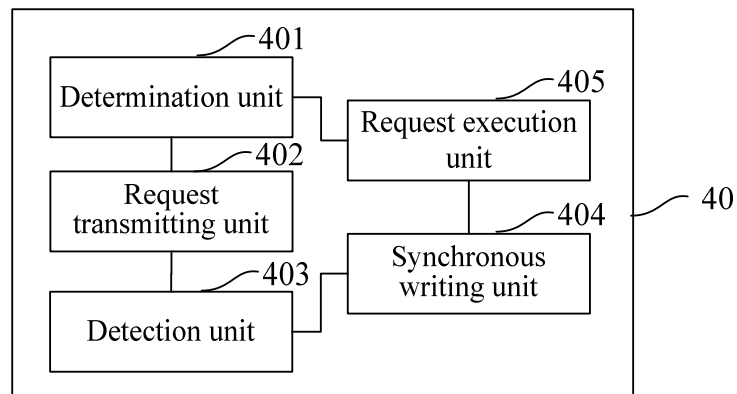


FIG. 4

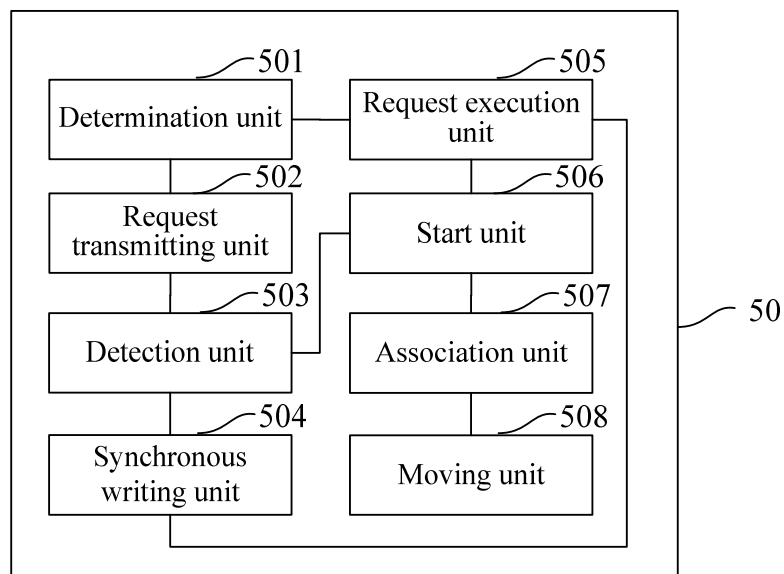


FIG. 5

Diagram illustrating the structure of the memory detection unit 609. The unit 609 is composed of three main components connected in series:

- 701: First buffer unit
- 702: Memory detection unit
- 703: Second buffer unit

The components are connected sequentially, with the output of the first buffer unit (701) feeding into the memory detection unit (702), which in turn feeds into the second buffer unit (703).

The diagram illustrates a system architecture. At the top, there is an 'Input device' (labeled 801) and an 'Output device' (labeled 802). Below these, there is a horizontal line representing a bus (labeled 805). At the bottom, there is a 'Processor' (labeled 804) and 'Memory' (labeled 803). Bidirectional arrows connect the Input device to the bus, the Output device to the bus, the Processor to the bus, and the Memory to the bus. A large arrow points from the label '80' to the entire system.

FIG. 8