What is claimed is:

1. A semiconductor device, comprising:

a substrate having a first region and a second region, the first region including memory cells, and the second region including transistors for driving the memory cells;

device isolation regions disposed within the substrate to define active regions of the substrate; and

contact plugs connected to the active regions,

wherein the active regions include:

a first guard active region surrounding the first region;

a second guard active region surrounding a portion of the second region; and

at least one dummy active region disposed between the first guard active region and the second guard active region,

wherein the contact plugs include:

a first contact plug connected to the first guard active region, and

a second contact plug connected to the second guard region;

wherein the at least one dummy active region is not connected to any contact plugs.

2. The semiconductor device of claim 1, wherein the substrate includes:

a first well disposed in the first region, the first well including first conductivity-type impurities; and

a second well disposed within the substrate to surround the first well, the second well including the first guard active region, and the second well including second conductivity-type impurities.

3. The semiconductor device of claim 1 or claim 2, wherein the second guard active region surrounds at least a transistor of the second region that is closest to the first region.

4. The semiconductor device of any one of claims 1 to 3, wherein the second guard active region is closest to the first guard active region among the active regions disposed in the second region, except for the at least one dummy active region.

5. The semiconductor device of any one of claims 1 to 4, wherein the substrate includes a third well disposed in the second region, the third well being disposed adjacent to the second guard active region.

6. The semiconductor device of any one of claims 1 to 5, wherein the first guard active region and the second guard active region include different conductivity-type impurities.

7. The semiconductor device of any one of claims 1 to 6, wherein the active regions further include a cell active region disposed in the first region, and the at least one dummy active region is further disposed between the cell active region and the first guard active region.

8. The semiconductor device of any one of claims 1 to 7, wherein the at least one dummy active region is spaced apart from a boundary between the first region and the second region, and extends along the boundary.

9. The semiconductor device of any one of claims 1 to 8, wherein each dummy active region of the at least one dummy active region has a line shape on a plane.

10. The semiconductor device of any one of claims 1 to 8, wherein each dummy active region of the at least one dummy active region has a plurality of quadrangular patterns disposed in a row on a plane.

11. The semiconductor device of any one of claims 1 to 10, wherein the at least one dummy active region includes a plurality of regions, the plurality of regions being spaced apart from one another, and the plurality of regions extending in parallel in one direction.

12. The semiconductor device of any one of claims 1 to 11, further comprising:

a dummy gate electrode disposed on a first dummy active region of the at least one dummy active region.

13. The semiconductor device of claim 12, wherein the dummy gate electrode extends in one direction along the first dummy active region.

14. The semiconductor device of claim 12 or claim 13, wherein a width of the dummy gate electrode is greater than a width of the first dummy active region.

15. The semiconductor device of any one of claims 1 to 14, further comprising:

a channel region extending vertically in the first region; and

gate electrodes spaced apart from one another and stacked along the channel

region, the gate electrodes extending to have different lengths toward a boundary between the first region and the second region.

16. The semiconductor device of claim 15, wherein the gate electrodes extend in a first direction, and the at least one dummy active region extends in a second direction, perpendicular to the first direction.

17. The semiconductor device of any one of claims 1 to 16, wherein, between the first guard active region and the second guard active region, a distance between the first guard active region or the second guard active region and the at least one dummy active region adjacent to the first guard active region or the second guard active region is less than 3 μm.

18. The semiconductor device of any one of claims 1 to 17, wherein each of the first guard active region and the second guard active region has a quadrangular ring shape.

19. A semiconductor device, comprising:

a gate electrode structure including gate electrodes, the gate electrodes spaced apart from one another and stacked on a substrate in a first direction perpendicular to the substrate, and the gate electrodes extending to have different lengths in a second direction, perpendicular to the first direction;

a guard active region disposed within the substrate to surround the gate electrode structure;

at least one dummy active region disposed on at least one side of the guard active region in the second direction, the at least one dummy active region being disposed within

the substrate to extend parallel to the guard active region; and

a dummy gate electrode disposed on a first dummy active region of the at least one dummy active region and extending in one direction along the first dummy active region.

20. The semiconductor device of claim 19, wherein the at least one dummy active region extends in a third direction, perpendicular to the first direction and the second direction.