

Circuits with Linear Finfet Structures

by inventors

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Background

[0001] It is known that optical lithography has reached the end of its capability at the 193 nm light wavelength and 1.35 numerical aperture (NA) immersion system. The minimum straight line resolution capability of this equipment is approximately 40 nm with an approximate 80 nm feature-to-feature pitch. A feature-to-feature pitch requirement lower than about 80 nm would require multiple patterning steps for a given structure type within a given chip level. Also, line end resolution becomes more challenging as lithography is pushed toward its resolution limits. In semiconductor device layout, a typical metal line pitch at the 32 nm critical dimension is approximately 100 nm. In order to achieve the cost benefit of feature scaling, a scaling factor of 0.7 to 0.75 is desirable. The scaling factor of about 0.75 to reach the 22 nm critical dimension would require a metal line pitch of about 75 nm, which is below the capability of current single exposure lithography systems and technology. It is within this context that the present invention arises.

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Summary

[0002] In one embodiment, a semiconductor device includes a substrate, a first transistor, and a second transistor. The first transistor has a source region and a drain region within a first diffusion fin. The first diffusion fin is structured to project from a surface of the substrate. The first diffusion fin is structured to extend lengthwise in a first direction from a first end of the first diffusion fin to a second end of the first diffusion fin. The second transistor has a source region and a drain region within a second diffusion fin. The second diffusion fin is structured to project from the surface of the substrate. The second diffusion fin is structured to extend lengthwise in the first direction from a first end of the second diffusion fin to a second end of the second diffusion fin. The second diffusion fin is positioned next to and spaced apart from the first diffusion fin. Also, either the first end or the second end of the second diffusion fin is positioned in the first direction between the first end and the second end of the first diffusion fin.

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[0003] In one embodiment, a method of fabricating a semiconductor device is disclosed. The method includes providing a substrate. The method also includes forming a first transistor on the substrate, such that the first transistor has a source region and a drain region within a first

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diffusion fin, and such that the first diffusion fin is formed to project from a surface of the substrate, and such that the first diffusion fin is formed to extend lengthwise in a first direction from a first end of the first diffusion fin to a second end of the first diffusion fin. The method also includes forming a second transistor on the substrate, such that the second transistor has a source region and a drain region within a second diffusion fin, and such that the second diffusion fin is formed to project from the surface of the substrate, and such that the second diffusion fin is formed to extend lengthwise in the first direction from a first end of the second diffusion fin to a second end of the second diffusion fin, and such that the second diffusion fin is formed at a position next to and spaced apart from the first diffusion fin. Also, the first and second transistors are formed such that either the first end or the second end of the second diffusion fin is formed at a position in the first direction between the first end and the second end of the first diffusion fin.

[0004] In one embodiment, a data storage device has computer executable program instructions stored thereon for rendering a layout of a semiconductor device. The data storage device includes computer program instructions for defining a first transistor to be formed on a substrate, such that the first transistor is defined to have a source region and a drain region within a first diffusion fin, and such that the first diffusion fin is defined to project from a surface of the substrate, and such that the first diffusion fin is defined to extend lengthwise in a first direction from a first end of the first diffusion fin to a second end of the first diffusion fin. The data storage device also includes computer program instructions for defining a second transistor to be formed on the substrate, such that the second transistor is defined to have a source region and a drain region within a second diffusion fin, and such that the second diffusion fin is defined to project from the surface of the substrate, and such that the second diffusion fin is defined to extend lengthwise in the first direction from a first end of the second diffusion fin to a second end of the second diffusion fin, and such that the second diffusion fin is defined to be positioned next to and spaced apart from the first diffusion fin, and such that the second diffusion fin is defined to have either its first end or its second end positioned in the first direction between the first end and the second end of the first diffusion fin.

Brief Description of the Drawings

[0005] Figures 1A and 1B show an example layout view of a finfet transistor, in accordance with some embodiments of the present invention.

[0006] Figure 1C shows a variation of the finfet transistor of Figures 1A/1B in which the diffusion fin 102 is more pyramid-shaped in the vertical cross-section view A-A, in accordance with some embodiments of the present invention.

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[0007] Figure 1D shows a simplified vertical cross-section view of the substrate having a number of finfet transistors formed thereon, in accordance with some embodiments of the present invention.

[0008] Figure 1E shows a diagram of fin pitch relationship in which the internal fin pitch Ps1 is substantially equal to the external fin pitch Ps2, in accordance with some embodiments of the present invention.

[0009] Figure 1F shows a variation of the fin pitch relationship diagram of Figure 1E in which the denominator (y) of the rational number is two, in accordance with some embodiments of the present invention.

[0010] Figure 1G shows a variation of the fin pitch relationship diagram of Figure 1E in which the denominator (y) of the rational number is three, in accordance with some embodiments of the present invention.

[0011] Figure 1H shows a more generalized version of the fin pitch relationship diagram of Figure 1E in which the internal fin pitch Ps1 and external fin pitch Ps2 are different, in accordance with some embodiments of the present invention.

[0012] Figure 2A shows an exemplary cell layout incorporating finfet transistors, in accordance with some embodiments of the present invention.

[0013] Figure 2B shows a circuit diagram corresponding to the 2-input NAND configuration of Figure 2D, in accordance with some embodiments of the present invention..

[0014] Figure 2C shows a circuit diagram corresponding to the 2-input NOR configuration of Figure 2E, in accordance with some embodiments of the present invention..

[0015] Figure 2D shows the layout of Figure 2A in which the diffusion fins 201A are formed of an n-type diffusion material and the diffusion fins 201B are formed of a p-type diffusion material, in accordance with some embodiments of the present invention..

[0016] Figure 2E shows the layout of Figure 2A in which the diffusion fins 201A are formed of a p-type diffusion material and the diffusion fins 201B are formed of an n-type diffusion material, in accordance with some embodiments of the present invention..

[0017] Figure 2F shows a variation of the layout of Figure 2A in which the gate electrode structures have their ends substantially aligned on the top of the cell and on the bottom of the cell, in accordance with some embodiments of the present invention.

[0018] Figure 2G shows a variation of the layout of Figure 2A in which contacts are formed to extend from the met1 interconnect structure to the horizontal local interconnect structure under the power rail at the top of the cell and at the bottom of the cell, in accordance with some embodiments of the present invention.

[0019] Figure 2H shows a variation of the cell of Figure 2A in which two different diffusion fin pitches are used, in accordance with some embodiments of the present invention.

[0020] Figure 2I shows a variation of the layout of Figure 2A in which the diffusion fins and horizontal local interconnect structures under the power rails at the top and bottom of the cell are extended to the full width of the met1 interconnect structures that serve as the power rails, in accordance with some embodiments of the present invention.

[0021] Figure 3 shows a variation of the layout of Figure 2A in which the met1 power rails are connected to vertical local interconnect, such that the met1 power rails serve as local power supplies, in accordance with some embodiments of the present invention.

[0022] Figure 4 shows a variation of the layout of Figure 2A in which a two-dimensionally varying met1 interconnect structure is used within the cell for intra-cell routing, in accordance with some embodiments of the present invention.

[0023] Figure 5 shows a variation of the layout of Figure 2A in which the met1 power rails are connected to vertical local interconnect and in which a two-dimensionally varying met1 interconnect structure is used within the cell for intra-cell routing, in accordance with some embodiments of the present invention.

[0024] Figure 6 shows a variation of the layout of Figure 2A in which fixed, minimum width, shared local met1 power supplies are used, along with a two-dimensionally varying met1 interconnect structure within the cell for intra-cell routing, in accordance with some embodiments of the present invention.

[0025] Figure 7 shows a variation of the layout of Figure 2A having shared local and global power supplies with hard connections in the cell, and a two-dimensionally varying met1 interconnect structure within the cell for intra-cell routing, in accordance with some embodiments of the present invention.

[0026] Figure 8A shows a layout of an example standard cell in which input pins are placed between diffusion fins of the same type to ease routing congestion, and in which some diffusion fins are used as interconnect conductors, in accordance with some embodiments of the present invention.

[0027] Figure 8B shows a variation of Figure 8A in which two different gate electrode pitches are used, in accordance with some embodiments of the present invention.

[0028] Figure 8C shows a circuit schematic of the layout of Figure 8A, in accordance with some embodiments of the present invention..

[0029] Figure 9A shows an example standard cell layout in which diffusion fins are utilized as interconnect conductors, in accordance with some embodiments of the present invention.

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[0030] Figure 9B shows the layout of Figure 9A with three sets of cross-coupled transistors identified, in accordance with some embodiments of the present invention.

[0031] Figure 9C shows a circuit schematic of the layout of Figure 9A, in accordance with some embodiments of the present invention..

5 [0032] Figure 10 shows an example standard cell layout with gate electrode contacts positioned substantially over the diffusion fins, in accordance with some embodiments of the present invention.

[0033] Figure 11 shows an example cell layout implementing diffusion fins, in accordance with some embodiments of the present invention.

10 [0034] Figures 12A/B show a variation of the layout of Figure 11 having minimum width met1 power rails, in accordance with some embodiments of the present invention.

[0035] Figures 13A/B show a variation of the layout of Figures 12A/B that does not have contacts from each of local interconnect and gate electrode structures to met1, in accordance with some embodiments of the present invention.

15 [0036] Figures 14A/B show a variation of the layout of Figure 11 having minimum width met1 power rails, with all met1 structures of the same width and on the same pitch, including the power rails, in accordance with some embodiments of the present invention.

[0037] Figures 15A/B show a variation of the layout of Figures 14A/B having met1 routing structures populated so each (y) location has a met1 structure, in accordance with some
20 embodiments of the present invention.

[0038] Figures 16A/B show a variation of the layout of Figure 11 having gate electrode structure contacts placed between p-type diffusion fins, in accordance with some embodiments of the present invention.

[0039] Figures 17A/B show an example cell layout implementing diffusion fins, in accordance
25 with some embodiments of the present invention.

[0040] Figures 18A/B show a variation of the layout of Figures 17A/B in which the contacts connect to the horizontal local interconnect, and in which the horizontal local interconnect connects directly to the vertical local interconnect, in accordance with some embodiments of the present invention.

30 [0041] Figures 19A/B show a variation of the layout of Figures 17A/B in which the power rail contact to local interconnect are not shared, and in which there is no shared local interconnect under the power rails, in accordance with some embodiments of the present invention.

[0042] Figures 20A/B show a variation of the layout of Figures 19A/B in which the diffusion fins are offset by a diffusion fin half-pitch with respect to the cell boundary, in accordance with some embodiments of the present invention.

[0043] Figures 21A/B show a variation of the layout of Figures 20A/B having minimum width power rails and negative vertical local interconnect overlap of the diffusion fins, in accordance with some embodiments of the present invention.

[0044] Figures 22A/B show a variation of the layout of Figures 17A/B having minimum width power rails, no shared local interconnect or diffusion fins under the power rails, and a larger space between p-fins and n-fins, in accordance with some embodiments of the present invention.

[0045] Figures 23A/B show a variation of the layout of Figures 17A/B, in accordance with some embodiments of the present invention.

[0046] Figures 24A/B show a variation of the layout of Figures 23A/B, in accordance with some embodiments of the present invention.

[0047] Figures 25A/B show a variation of the layout of Figures 23A/B, in which the cell is doubled in height, in accordance with some embodiments of the present invention.

[0048] Figures 26A/B show an example cell layout implementing diffusion fins, in accordance with some embodiments of the present invention.

[0049] Figures 27A/B show a variation of the layout of Figures 26A/B, in accordance with some embodiments of the present invention.

[0050] Figures 28A/B show an example cell layout implementing diffusion fins, in accordance with some embodiments of the present invention.

[0051] Figures 29A/B show a variation of the layout of Figures 28A/B in which there are no local interconnect structures present between two gate electrode structures of n-type transistors, in accordance with some embodiments of the present invention.

[0052] Figures 30A/B show an example cell layout implementing diffusion fins, in accordance with some embodiments of the present invention.

[0053] Figure 31A shows an example sdf cell layout with gate electrode and local interconnect line end gaps centered substantially between diffusion fins, in accordance with some embodiments of the present invention.

[0054] Figure 31B shows the example sdf cell layout of Figure 31A, with the local interconnect line end gaps centered substantially between the diffusion fins circled, in accordance with some embodiments of the present invention..

[0055] Figure 31C shows the example sdff cell layout of Figures 31A and 31B with annotation of the region between two adjacent gate electrode structures in which the diffusion fin ends overlap each other in the x direction, in accordance with some embodiments of the present invention.

5 [0056] Figure 32 shows an example layout in which all contact layer structures are placed between the diffusion fins, in accordance with some embodiments of the present invention..

[0057] Figures 33 and 34 shows example layouts in which all contact layer structures are placed on the diffusion fins, in accordance with some embodiments of the present invention..

10 [0058] Figures 35A/B through 47A/B show cross-couple transistor configurations having transmission gate in both logic paths, requiring all the internal nodes to have a connection between p-type and n-type, in accordance with some embodiments of the present invention..

[0059] Figure 35C shows a circuit schematic of the layouts of Figures 35A/B through 47A/B and 63A/B through 67A/B, in accordance with some embodiments of the present invention.

15 [0060] Figures 48A/B through 57A/B show cross-couple transistor configurations having transmission gate in the logic path with larger transistors, and tristate gate in other paths, in accordance with some embodiments of the present invention..

[0061] Figure 48C shows a circuit schematic of the layouts of Figures 48A/B through 58A/B, in accordance with some embodiments of the present invention.

20 [0062] Figures 58A/B through 59A/B show cross-couple transistor configurations having transmission gate in the logic path with smaller transistors, and tristate gate in other paths, in accordance with some embodiments of the present invention..

[0063] Figure 59C shows a circuit schematic of the layout of Figures 59A/B, in accordance with some embodiments of the present invention.

25 [0064] Figures 60A/B through 62A/B show cross-couple transistor configurations having tristate gate in both logic paths, in accordance with some embodiments of the present invention..

[0065] Figure 60C shows a circuit schematic of the layouts of Figures 60A/B through 62A/B and Figures 68A/B through 69A/B, in accordance with some embodiments of the present invention.

30 [0066] Figures 63A/B through 67A/B show cross-couple transistor configurations having transmission gate in both logic paths, requiring all the internal nodes to have a connection between p-type and n-type, in accordance with some embodiments of the present invention..

[0067] Figures 68A/B through 69A/B show cross-couple transistor configurations having tristate gate in both logic paths, in accordance with some embodiments of the present invention..

[0068] Figure 70A shows an example of gate electrode tracks 70-1A through 70-1E defined within the restricted gate level layout architecture, in accordance with some embodiments of the present invention.

[0069] Figure 70B shows the exemplary restricted gate level layout architecture of Figure 70A with a number of exemplary gate level features 7001-7008 defined therein, in accordance with some embodiments of the present invention.

[0070] Figures 71A/B through 77A/B show a number of example SDFE circuit layouts that utilize both tri-state and transmission gate based cross-coupled circuit structures, in accordance with some embodiments of the present invention.

[0071] Figure 71C shows a circuit schematic of the layouts of Figures 71A/B and 77A/B, in accordance with some embodiments of the present invention.

[0072] Figure 72C shows a circuit schematic of the layouts of Figures 72A/B through 76A/B, in accordance with some embodiments of the present invention.

Detailed Description

[0073] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention. Additionally, it should be understood that the various circuit and/or layout features depicted in a given figure presented herein can be utilized in combination with other circuit and/or layout features depicted in other figures presented herein.

[0074] A "finfet" is a transistor constructed from a vertical silicon island, i.e., fin. The finfet transistor can also be referred to as a tri-gate transistor. The term "finfet" transistor as used herein refers to any transistor configuration that includes a diffusion structure that projects upward from an underlying substrate. Figures 1A and 1B show an example layout view of a finfet transistor 100, in accordance with some embodiments of the present invention. The finfet transistor 100 is constructed from a diffusion fin 102 and a gate electrode layer 104. The diffusion fin 102 projects vertically upward from a substrate 105, as shown in Figure 1B. A gate oxide layer 106 is disposed between the diffusion fin 102 and the gate electrode layer 104. The diffusion fin 102 can be doped to form either a p-type transistor or an n-type transistor.

The portion of the gate electrode layer 104 that covers the diffusion fin 102 forms the gate electrode of the finfet transistor 100. Therefore, the gate electrode of the finfet transistor 100 can exist on three or more sides of the diffusion fin 102, thereby providing for control of the finfet transistor channel from three or more sides, as opposed to from one side as in a non-
5 finfet transistor. Also, in some embodiments, the finfet transistor is formed as a "wrap-around" transistor in which the gate oxide layer 106 and the gate electrode layer 104 also extend beneath the diffusion fin 102.

[0075] It should be understood that the example finfet transistor 100 depicted in Figures 1A and 1B is provided by way of example and does not represent any limitation on the manner in
10 which a finfet transistor, as referenced herein, may be designed and/or fabricated. Specifically, in some embodiments, the diffusion fin (e.g., 102) can be formed as a layering of different materials, including but not limited to Si (silicon), SiGe (silicon germanium), Ge (germanium), InP (indium phosphide), CNT (carbon nanotube), SiNT (silicon nanotube), or any combination thereof, among others. The gate oxide layer 106 can be formed from many different types of
15 dielectric materials. For example, in some embodiments, the gate oxide layer 106 may be formed as a layer of hafnium oxide on a layer of silicon dioxide. In other embodiments, the gate oxide layer 106 can be formed by one or more other dielectric materials. In some embodiments, the gate electrode layer 104 can be formed by any number of electrically conductive materials. For example, in some embodiments, the gate electrode layer 104 can be
20 formed as a film of TiN (titanium nitride) or TaN (tantalum nitride) covered by polysilicon. It should be understood, however, that in other embodiments the gate electrode layer 104 can be formed by other materials.

[0076] Also, while the example diffusion fin 102 of Figure 1B is shown as having a substantially vertically projecting rectangular structure relative to the substrate 105 in the
25 vertical cross-section view A-A, it should be understood that diffusion fins 102 in an "as-fabricated" state on a semiconductor chip may or may not have the substantially vertically projecting rectangular structure relative to the substrate 105. For example, in some embodiments, the diffusion fins 102 in their "as-fabricated" state may have a more triangular or pyramid-like shape in the vertical cross-section view A-A. Figure 1C shows a variation of
30 the finfet transistor 100 in which the diffusion fin 102 is more pyramid-shaped in the vertical cross-section view A-A. As depicted in Figure 1C, in some embodiments, the sides of the diffusion fins 102 that extend upward from the substrate 105 may extend upward from the substrate at an angle to the substrate 105, so as to be non-perpendicular to the substrate 105. Also, it should be understood that such a non-perpendicular relationship between the substrate

105 and the sides of the diffusion fins 102 that extend upward from the substrate 105 may be by design or may be a result of fabrication.

[0077] Additionally, in some embodiments, a vertical projection distance of the diffusion fins 102 above the substrate 105 will be substantially equal across a region of the semiconductor chip. However, in other embodiments, some diffusion fins 102 may be designed and fabricated to have multiple different vertical projection distances above the substrate 105 across one or more regions of the semiconductor chip. Because the channel area of the finfet transistor 100 is a function of the diffusion fin 102 vertical projection distance above the substrate 105, such a variation in diffusion fin 102 vertical projection distance above the substrate 105 can be used to adjust a drive strength of selected finfet transistors 100 relative to others on the semiconductor chip. In one example, selective variation in diffusion fin 102 height can be provided through selective etching/overetching of the diffusion fin 102 structures during fabrication.

[0078] Figure 1D shows a simplified vertical cross-section view of the substrate 105 having a number of finfet transistors 100 formed thereon, in accordance with some embodiments of the present invention. During fabrication of the finfet transistors 100, a series of cores 107 are formed to facilitate formation of side spacers 109 for each of the cores 107. The side spacers 109 are utilized as masking features to facilitate formation of the underlying finfet transistors 100. It should be understood that the cores 107, the side spacers 109, and the finfet transistors 100 extend lengthwise in a parallel manner, i.e., into the page as shown in Figure 1D. It should be understood that the cores 107 and side spacers 109 are ultimately removed so as not to be present in the final as-fabricated semiconductor chip/device. The relative spacing of the finfet transistors 100 to each other is a function of the sizes and spacings of the cores 107 and side spacers 109.

[0079] Figure 1D shows the cores 107 as having a width W_b and a pitch P_b . Also, Figure 1D shows the side spacers 109 as having a width W_s . The finfet transistors 100 can then be characterized as having an alternating pair of fin pitches Ps_1 , Ps_2 , where Ps_1 is an average centerline-to-centerline pitch between side spacers 109 of a given core 107 (Ps_1 is referred to as an internal fin pitch), and where Ps_2 is an average centerline-to-centerline pitch between neighboring side spacers 109 of a adjacently positioned cores 107 (Ps_2 is referred to as an external fin pitch). Assuming uniformity in each of the core 107 width W_b , the core 107 pitch P_b , and the side spacer 109 width W_s , the internal fin pitch Ps_1 is equal to the sum of the core 107 width W_b and side spacer 109 width W_s . And, the external fin pitch Ps_2 is equal to the core 107 pitch P_b minus the sum of the core 107 width W_b and side spacer 109 width W_s .

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Therefore, both the internal fin pitch $Ps1$ and the external fin pitch $Ps2$ will vary as each of the core 107 pitch Pb , core 107 width Wb , and/or side spacer 109 width Ws varies. Thus, it should be understood that reference to a given "fin pitch" refers to an average of a given fin pitch, i.e., fin pitch Ps_{ave} is equal to an average of the internal fin pitch $Ps1$ and the external fin pitch $Ps2$, where each of the internal fin pitch $Ps1$ and the external fin pitch $Ps2$ are themselves averages.

[0080] Figure 1E shows a diagram of fin pitch relationship in which the internal fin pitch $Ps1$ is substantially equal to the external fin pitch $Ps2$, in accordance with some embodiments of the present invention. A cell height Hc is equal to the average fin pitch multiplied by a rational number, i.e., multiplied by a ratio of integers x and y , where x is the numerator of the rational number and y is the denominator of the rational number. In the case of Figure 1E where the internal fin pitch $Ps1$ and external fin pitch $Ps2$ are equal, the average fin pitch is equal to each of $Ps1$ and $Ps2$. Therefore, the cell height Hc is equal to either the internal fin pitch $Ps1$ or the external fin pitch $Ps2$ multiplied by the rational number. It should be understood that the denominator (y) of the rational number indicates a number of cells required to obtain a repetition of a fin-to-cell boundary spacing when the number of cells are positioned in an abutting manner in the direction of the cell height Hc , i.e., in the direction perpendicular to the lengthwise direction of the fins. Also, when the numerator (x) of the rational number is evenly divisible by the denominator (y) of the rational number, the top and bottom cell boundaries can have the same fin-to-cell boundary spacing when the internal fin pitch $Ps1$ and/or the external fin pitch $Ps2$ is aligned with (indexed to) the cell boundary.

[0081] Figure 1F shows a variation of the fin pitch relationship diagram of Figure 1E in which the denominator (y) of the rational number is two, in accordance with some embodiments of the present invention. Therefore, in Figure 1F the fin-to-cell boundary spacing will repeat every two cell heights Hc . Also, in the example of Figure 1F, the numerator (x) of the rational number is not evenly divisible by the denominator (y) of the rational number. Therefore, the top and bottom fin-to-cell boundary spacings will be different when the internal fin pitch $Ps1$ and/or the external fin pitch $Ps2$ is aligned with (indexed to) the cell boundary.

[0082] Figure 1G shows a variation of the fin pitch relationship diagram of Figure 1E in which the denominator (y) of the rational number is three, in accordance with some embodiments of the present invention. Therefore, in Figure 1G the fin-to-cell boundary spacing will repeat every three cell heights Hc . Also, in the example of Figure 1G, the numerator (x) of the rational number is not evenly divisible by the denominator (y) of the rational number. Therefore, the top and bottom fin-to-cell boundary spacings will be different when the internal

fin pitch Ps1 and/or the external fin pitch Ps2 is aligned with (indexed to) the cell boundary. It should be appreciated that the rational number can be defined in any manner necessary to obtain any desired fin-to-cell boundary spacing repetition frequency in the direction of the cell height Hc and/or any desired fin-to-cell boundary spacing specification.

5 [0083] Figure 1H shows a more generalized version of the fin pitch relationship diagram of Figure 1E in which the internal fin pitch Ps1 and external fin pitch Ps2 are different, in accordance with some embodiments of the present invention. In this example, the external fin pitch Ps2 is greater than the internal fin pitch Ps1. It should be understood that the cell height Hc is equal to the average fin pitch Ps_ave multiplied by the rational number (x/y), where x and y are integers. Also, it should be understood that the integer y indicates the fin-to-cell boundary spacing repetition frequency in the direction of the cell height Hc. Also, it should be understood that the top and bottom fin-to-cell boundary spacings can be equal to each other when the rational number (x/y) reduces to an integer value, i.e., when x is evenly divisible by y. If the rational number (x/y) does not reduce to an integer value, different fin phasing variations of a given cell may be defined in a cell library, where each fin phasing variation corresponds to a different possible fin-to-cell boundary spacing relationship for the given cell. Also, the number of possible fin phasing variations for a given cell will be equal to the denominator (y) of the rational number (x/y) in its most mathematically reduced form.

15 [0084] As discussed above, Figure 1H shows use of two different diffusion fin pitches Ps1 and Ps2, in accordance with some embodiments of the present invention. More specifically, in Figure 1H every other pair of adjacently positioned diffusion fin structures is placed according to a smaller pitch Ps1. In some embodiments, the larger diffusion fin pitch Ps2 is about 80 nanometers (nm) and the smaller diffusion fin pitch Ps1 is about 60 nm. However, it should be understood that in other embodiments, the smaller diffusion fin pitch Ps1 can be any size, and the larger diffusion fin pitch Ps2 can be any size. It should be understood that some embodiments can utilize more than two diffusion fin pitches within a given cell or block. And, some embodiments may utilize a single diffusion fin pitch within a given cell or block. Also, it should be understood that any layer of the semiconductor device, or portion thereof, can be formed in a manner similar to that described herein with regard to the diffusion fin pitch(es).

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30 For example, a local interconnect layer or a higher-level interconnect layer of the semiconductor device, or portion thereof, can include interconnect conductive structures formed on one or more corresponding pitch(es) in a manner similar to that described herein with regard to the diffusion fin pitch(es).

[0085] Transistor scaling has slowed below the 45 nanometers (nm) critical dimension due to gate oxide limitations and/or source/drain leakage scaling issues. The finfet transistor mitigates these issues by controlling the channel of the finfet transistor from three sides. The increased electrical fields in the channel of the finfet transistor improve the relationship between I-on (on drive current) and I-off (sub-threshold leakage current). Finfet transistors can be employed at the 22 nm critical dimension and below. However, due to their vertical projection, finfet transistors can have restricted placement in various circuit layouts. For instance, there can be a required finfet-to-finet minimum spacing and/or a required finfet-to-finet minimum pitch, among other restrictions. Embodiments are disclosed herein for cell layouts that utilize finfet transistors in a manner which complements layout scaling.

[0086] A cell, as referenced herein, represents an abstraction of a logic function, and encapsulates lower-level integrated circuit layouts for implementing the logic function. It should be understood that a given logic function can be represented by multiple cell variations, wherein the cell variations may be differentiated by feature size, performance, and process compensation technique (PCT) processing. For example, multiple cell variations for a given logic function may be differentiated by power consumption, signal timing, current leakage, chip area, OPC (optical proximity correction), RET (reticle enhancement technology), etc. It should also be understood that each cell description includes the layouts for the cell in each level (or layer) of a chip within the associated vertical column of the chip, as required to implement the logic function of the cell. More specifically, a cell description includes layouts for the cell in each level of the chip extending from the substrate level up through a particular interconnect level.

[0087] Figure 2A shows an exemplary cell layout incorporating finfet transistors, in accordance with some embodiments of the present invention. The cell layout includes a diffusion level within which a number of diffusion fins 201A/201B are defined for subsequent formation of finfet transistors and associated connections. In some embodiments, in an as-drawn layout state, the diffusion fins 201A/201B are linear-shaped. The diffusion fins 201A/201B are oriented to be parallel to each other such that their lengths extend in a first direction (x), and such that their widths extend in a second direction (y) perpendicular to the first direction (x).

[0088] In some embodiments, such as shown in Figure 2A, the diffusion fins 201A/201B are placed in accordance with a fixed lengthwise centerline-to-lengthwise centerline pitch 203, as measured in the second direction (y). In this embodiment, the pitch 203 of the diffusion fins 201A/201B may be related to the cell height as measured in the second direction (y), such that

the diffusion fin pitch 203 can be continued across cell boundaries. In Figure 2A, the cell abutment edges represent the cell boundaries that run parallel to the diffusion fins 201A/201B. In some embodiments, the diffusion fins for multiple neighboring cells will be placed in accordance with a common global diffusion fin pitch, thereby facilitating chip level manufacturing of the diffusion fins in multiple cells.

[0089] It should be understood that other embodiments may utilize multiple diffusion fin pitches within a given cell or among a collection of cells. For example, Figure 2H shows a variation of the cell of Figure 2A in which two different diffusion fin pitches 203 and 205 are used, in accordance with some embodiments of the present invention. It should be understood in some embodiments the diffusion fins 201A/201B can be placed in accordance with one or more lengthwise centerline-to-lengthwise centerline pitches, or may be placed in an unrestricted manner with regard to lengthwise centerline-to-lengthwise centerline spacing. Also, in some embodiments, the diffusion fins 201A/201B can be placed in accordance with a given pitch and some pitch locations may be vacant with regard to diffusion fin placement. Additionally, in some embodiments, diffusion fins can be placed in a spaced apart, end-to-end manner at a given diffusion fin pitch location within a cell.

[0090] In each Figure presented herein, each diffusion fin, e.g., diffusion fins 201A/201B in Figure 2A, is of either an n-type diffusion material or a p-type diffusion material. Also, depending on the particular cell implementation, the type of material of the diffusion fins may be swapped to obtain a different cell logic function. Therefore, the notation type1_diff and type2_diff is used in the Figures to denote different material types for the diffusion fins. For example, if the type1_diff material is an n-type material, then the type2_diff material is a p-type material, vice-versa.

[0091] The cell layout also includes a number of linear-shaped gate electrode structures 207. The linear-shaped gate electrode structures 207 extend in a substantially perpendicular direction to the diffusion fins 201A/201B, i.e., in the second direction (y). When fabricated, the linear-shaped gate electrode structures 207 wrap over the diffusion fins 201A/201B to form gate electrodes of finfet transistors. It should be understood that an appropriate gate oxide material is disposed, i.e., positioned/deposited, between the diffusion fins 201A/201B and the gate electrode structures 207 formed thereover.

[0092] In some embodiments, the linear-shaped gate electrode structures 207 are placed in accordance with a fixed gate pitch 209 as measured in the first direction (x) between lengthwise centerlines of adjacently positioned gate electrode structures 207. In some embodiments, the gate pitch 209 is related to the cell width as measured in the first direction

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(x), such that the gate pitch can be continued across cell boundaries. Therefore, in some embodiments, the gate electrode structures 207 for multiple neighboring cells can be placed in accordance with a common global gate pitch, thereby facilitating chip level manufacturing of the linear-shaped gate electrode structures 207 in multiple cells.

5 [0093] It should be understood that some of the gate pitch locations in a given cell may be occupied by gate electrode structures 207, while other gate pitch locations in the given cell are left vacant. Also, it should be understood that multiple gate electrode structures 207 can be placed in a spaced apart, end-to-end manner along any of the gate electrode pitch locations within a given cell. It should be further understood that in some embodiments, the gate
10 electrode structures 207 can be placed in accordance with one or more gate pitches, or can be placed in an unrestricted manner with regard to gate pitch.

[0094] The cell layout can also include a number of horizontal linear-shaped local interconnect structures (lih) 211, and/or a number of vertical linear-shaped local interconnect structures (liv) 213. The vertical local interconnect structures 213 are oriented parallel to the gate electrode
15 structures 207. The horizontal local interconnect structures 211 are oriented parallel to the diffusion fins 201A/201B. In some embodiments, placement of the vertical local interconnect structures 213 is defined to be out of phase from placement of the gate electrode structures 207 by one-half of the gate pitch. Thus, in this embodiment, each vertical local interconnect structure 213 is centered between its neighboring gate electrode structures 207, when the
20 neighboring gate electrode structures 207 are positioned on the gate pitch. Therefore, in this embodiment, adjacently placed vertical local interconnect structures 213 will have a center-to-center spacing equal to a local gate pitch or a global gate pitch, where the local gate pitch is applied within a given cell, and the global gate pitch is applied across multiple cells.

[0095] In some embodiments, placement of the horizontal local interconnect structures 211 is
25 defined to be out of phase from placement of the diffusion fins 201A/201B by one-half of the diffusion fin pitch. Thus, in this embodiment, the horizontal local interconnect structures 211 can be centered between its neighboring diffusion fins 201A/201B, when the neighboring diffusion fins 201A/201B are positioned on the diffusion fin pitch. Therefore, in this embodiment, adjacently placed horizontal local interconnect structures 211 will have a center-
30 to-center spacing equal to a local diffusion fin pitch or a global diffusion fin pitch, where the local diffusion fin pitch is applied within a given cell, and the global diffusion fin pitch is applied across multiple cells.

[0096] In some embodiments, the cell layout also includes a number of linear-shaped metal 1 (met1) interconnect structures 215. The met1 interconnect structures 215 are oriented parallel

to the diffusion fins 201A/201B and perpendicular to the gate electrode structures 207. In some embodiments, placement of the met1 interconnect structures 215 is defined to be out of phase from placement of the diffusion fins 201A/201B by one-half of the diffusion fin pitch. Thus, in this embodiment, each met1 interconnect structure 215 is centered between its neighboring diffusion fins, when its neighboring diffusion fins are positioned on the diffusion fin pitch, albeit within a higher chip level. Therefore, in this embodiment, adjacently placed met1 interconnect structures 215 will have a center-to-center spacing equal to a local diffusion fin pitch or a global diffusion fin pitch, where the local diffusion fin pitch is applied within a given cell, and the global diffusion fin pitch is applied across multiple cells. In some embodiments, the met1 interconnect structure 215 pitch, and hence the diffusion track pitch, is set at the single exposure lithographic limit, e.g., 80 nm for 193 nm wavelength light and 1.35 NA. In this embodiment, no double exposure lithography, i.e., multiple patterning, is required to manufacture the met1 interconnect structures 215. It should be understood that other embodiments can utilize met1 interconnect structures 215 that are oriented perpendicular to the diffusion fins 201A/201B and parallel to the gate electrode structures 207.

[0097] The cell layout also includes a number of contacts 217 defined to connect various met1 interconnect structures 215 to various local interconnect structures 211/213 and gate electrode structures 207, thereby providing electrical connectivity between the various finfet transistors as necessary to implement the logic function of the cell. In some embodiments, the contacts 217 are defined to satisfy single exposure lithographic limits. For example, in some embodiments, layout features to which the contacts 217 are to connect are sufficiently separated to enable single exposure manufacture of the contacts 217. For instance, the met1 interconnect structures 215 are defined such that their line ends which are to receive contacts 217 are sufficiently separated from neighboring met1 interconnect structure 215 line ends which are also to receive contacts 217, such that a spatial proximity between the contacts 217 is sufficiently large to enable single exposure lithography of the contacts 217. In some embodiments, neighboring contacts 217 are separated from each other by at least 1.5 times the gate pitch. It should be appreciated that line end cutting and the associated increased expense of double exposure lithography can be eliminated by sufficiently separating opposing line ends of the met1 interconnect structures 215. It should be understood that contact separation and line end separation on metal layers can be independent of each other in some embodiments, depending on choices made in the manufacturing process.

[0098] In some embodiments, the cell layout also includes a number of linear-shaped metal 2 (met2) interconnect structures 219. The met2 interconnect structures 219 are oriented parallel

to the gate electrodes 207 and perpendicular to the diffusion fins 201A/201B. The met2 interconnect structures 219 can be physically connected to the met1 interconnect structures 215 by via 1 structures (v1) 221, as necessary to implement the logic function of the cell. Although the example cell of Figure 2A shows the met1 interconnect structures 219 extending in a lengthwise manner perpendicular to the gate electrode structures 207 and the met 2 interconnect structures 219 extending in a lengthwise manner parallel to the gate electrode structures 207, it should be understood that in other embodiments the met1 interconnect structures 219 and met 2 interconnect structures 219 can be defined to extend in any orientation relative to the gate electrode structures 207. It should be understood that other embodiments can utilize met2 interconnect structures 219 are oriented perpendicular to the gate electrodes 207 and parallel to the diffusion fins 201A/201B.

[0099] The cell of Figure 2A represents a multi-input logic gate having substantially aligned input gate electrodes, i.e., the center three gate electrode structures 207 that are co-aligned in the direction (y). Depending on the assignment of diffusion material type to the diffusion fins of type1 and type2, the cell of Figure 2A can have a different logic function. For example, Figure 2D shows the layout of Figure 2A in which the diffusion fins 201A are formed of an n-type diffusion material and the diffusion fins 201B are formed of a p-type diffusion material. The layout of Figure 2D is that of a 2-input NAND gate. Figure 2B shows a circuit diagram corresponding to the 2-input NAND configuration of Figure 2D. Figure 2E shows the layout of Figure 2A in which the diffusion fins 201A are formed of a p-type diffusion material and the diffusion fins 201B are formed of an n-type diffusion material. The layout of Figure 2E is that of a 2-input NOR gate. Figure 2C shows a circuit diagram corresponding to the 2-input NOR configuration of Figure 2E. In Figures 2B-2E, each of P1 and P2 identifies a respective p-type transistor (e.g., PMOS transistor), each of N1 and N2 identifies a respective n-type transistor (e.g., NMOS transistor), each of A and B identifies a respective input node, and Q identifies an output node. It should be understood that similar notation for p-type transistors, n-type transistors, input nodes, and output nodes is also used in other figures herein.

[00100] Based on the foregoing, it should be appreciated that the logic function of a given cell layout can be changed by swapping the material types of the diffusion fins. Therefore, for each cell layout present herein, it should be understood that multiple logic functions can be represented depending on the assignment of n-type and p-type materials to the diffusion fins.

[00101] Figures 3 through 7 and 11 through 29 show variations on the layout of Figure 2A, in accordance with some embodiments of the present invention. Therefore, each of the

cells depicted in Figures 3 through 7 and 11 through 29 represent either a 2-input NAND gate or a 2-input NOR gate, depending on the assignment of n-type and p-type materials to the type1_diff and type2_diff diffusion fins. Each of cell layouts shown in Figures 2A through 7 and 11 through 29 have the following features:

- a multi-input logic gate with all its input electrodes substantially aligned,
- a local diffusion fin layer power supply,
- a global higher level interconnect power supply,
- a horizontal interconnect used to connect gate electrode to vertical local interconnect and to help improve manufacturability of the contact layers by enabling greater flexibility in contact placement.

[00102] It should be appreciated that each of the layouts in Figures 2A through 7 and 11 through 29 shows a different implementation of the same logic function. The layout of Figure 2A shows the following features:

- gate electrodes for two or more inputs, with the gate electrodes substantially aligned,
- gate electrode end line spaces located between diffusion fins of the same diffusion type,
- gate electrode contacts between diffusion fins of the same diffusion type,
- type1_diff and type2_diff diffusion fins used for a local power supply, i.e., to the local interconnect of the cell, with met1 used for higher level interconnect (global) power supply, with both local and global power supplies shared with abutting cells,
- diffusion fins of type1_diff and type2_diff supply current to cell on a local level and can be connected to the higher level interconnect, e.g., met1, at prescribed intervals to support multiple chip power strategies,
- use of horizontal local interconnect for connection to gate electrode,
- a substantially horizontal local interconnect that connects the vertical local interconnect layer to the gate electrode layer can be used to shift locations of the gate electrode contacts, thereby serving to increase flexibility in the contact mask patterns, which can ease potential lithography issues.

[00103] Figure 2F shows a variation of the layout of Figure 2A in which the gate electrode structures have their ends substantially aligned on the top of the cell, as indicated by the oval 250, and on the bottom of the cell, as indicated by the oval 251, in accordance with some embodiments of the present invention.

[00104] Figure 2G shows a variation of the layout of Figure 2A in which contacts are formed to extend from the met1 interconnect structure to the horizontal local interconnect

structure under the power rail at the top of the cell, as indicated by circle 260, and at the bottom of the cell, as indicated by circle 261, in accordance with some embodiments of the present invention.

[00105] As previously mentioned, Figure 2H shows a variation of the cell of Figure 2A in which two different diffusion fin pitches 203 and 205 are used, in accordance with some
5 embodiments of the present invention.

[00106] It should be understood that the diffusion fins and horizontal local interconnect structures under the power rails at the top and bottom of the cells in the various layouts depicted herein extend continuously in the horizontal direction (x) so as to service multiple
10 cells that are positioned in a row, and possibly in adjacent rows. To illustrate this point, Figure 2I shows a variation of the layout of Figure 2A in which the diffusion fins and horizontal local interconnect structures under the power rails at the top and bottom of the cell are extended to the full width of the met1 interconnect structures 215A/215B that serve as the power rails, in accordance with some embodiments of the present invention. It should be understood that the
15 diffusion fins and horizontal local interconnect structures under the power rails 215A/215B, along with the power rails 215A/215B themselves, extend continuously in the (x) direction, as indicated by arrows 270.

[00107] Figure 3 shows a variation of the layout of Figure 2A in which the met1 power rails are connected to vertical local interconnect, such that the met1 power rails serve as local
20 power supplies, in accordance with some embodiments of the present invention. It should be understood that the met1 power rails can be of variable width based on the cell library requirements. As with the layout of Figure 2A, the layout of Figure 3 uses multi-input logic gate with input electrodes substantially aligned.

[00108] Figure 4 shows a variation of the layout of Figure 2A in which a two-
25 dimensionally varying met1 interconnect structure is used within the cell for intra-cell routing, in accordance with some embodiments of the present invention. As with the layout of Figure 2A, the layout of Figure 4 uses multi-input logic gate with input electrodes substantially aligned and shared local and global power supplies. In some embodiments, bends in met1, i.e., the two-dimensional changes in direction of met1, occur on a fixed grid. In some
30 embodiments, this met 1 fixed grid can include horizontal grid lines positioned between and extending parallel to the diffusion fins and positioned on the same pitch as the diffusion fins. Also, in some embodiments, this met 1 fixed grid can include vertical grid lines extending perpendicular to the diffusion fins and positioned so as to be centered on the vertical local interconnect.

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[00109] Figure 5 shows a variation of the layout of Figure 2A in which the met1 power rails are connected to vertical local interconnect, such that the met1 power rails serve as local power supplies, and in which a two-dimensionally varying met1 interconnect structure is used within the cell for intra-cell routing, in accordance with some embodiments of the present invention. As with the layout of Figure 2A, the layout of Figure 5 uses multi-input logic gate with input electrodes substantially aligned.

[00110] Figure 6 shows a variation of the layout of Figure 2A in which fixed, minimum width, shared local met1 power supplies are used, along with a two-dimensionally varying met1 interconnect structure within the cell for intra-cell routing, in accordance with some embodiments of the present invention. As with the layout of Figure 2A, the layout of Figure 6 uses multi-input logic gate with input electrodes substantially aligned.

[00111] Figure 7 shows a variation of the layout of Figure 2A having shared local and global power supplies with hard connections in the cell, and a two-dimensionally varying met1 interconnect structure within the cell for intra-cell routing, in accordance with some embodiments of the present invention. As with the layout of Figure 2A, the layout of Figure 7 uses multi-input logic gate with input electrodes substantially aligned.

[00112] Figure 8A shows a layout of an example standard cell in which input pins are placed between diffusion fins of the same type to ease routing congestion, and in which some diffusion fins are used as interconnect conductors, in accordance with some embodiments of the present invention. Figure 8C shows a circuit schematic of the layout of Figure 8A, including input pins 8a, 8b, 8c, and 8d. Planar standard cells, i.e., non-finfet cells, typically have input pins located between diffusion features of the opposite type, i.e., n-type versus p-type, or between the diffusion features and the neighboring power rail, thereby creating a higher concentration of input pins in local areas of the planar cells. As demonstrated in Figure 8A, by utilizing diffusion fins and placing some input pins between diffusion fins of the same diffusion type, the input pins can be spread apart in a more even manner over a larger area, thereby easing routing congestion for the cell. Also, as demonstrated in Figure 8A, by selectively removing some gate electrode structures, as shown in the region 8001, the diffusion fin layers can be utilized as a substantially horizontal routing layer to connect to transistors or local interconnect that is not neighboring. For example, in the region 8001, the diffusion fins 8003 are used as horizontal routing conductors.

[00113] Figure 8B shows a variation of Figure 8A in which two different gate electrode pitches p1 and p2 are used, in accordance with some embodiments of the present invention. More specifically, in Figure 8B every other pair of adjacently positioned gate electrode

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structures is placed according to a smaller pitch p2. In some embodiments, the larger gate electrode pitch p1 is about 80 nanometers (nm) and the smaller gate electrode pitch p2 is about 60 nm. It should be understood that some embodiments can utilize more than two gate electrode structure pitches within a given cell or block. And, some embodiments may utilize a single gate electrode structure pitch within a given cell or block. Also, it should be understood that any layer of the semiconductor device, or portion thereof, can be formed in a manner similar to that described herein with regard to the gate electrode pitch(es). For example, a local interconnect layer or a higher-level interconnect layer of the semiconductor device, or portion thereof, can include interconnect conductive structures formed on one or more corresponding pitch(es) in a manner similar to that described herein with regard to the gate electrode pitch(es).

[00114] Additionally, conductive structures in different layers (a.k.a. levels) of the semiconductor device, or portion thereof, can be positioned on respective pitch arrangements where a defined relationship exists between the conductive structure pitch arrangements of the different layers. For example, in some embodiments, diffusion fins in the diffusion fin layer are positioned in accordance with a diffusion fin pitch arrangement that can include one or more diffusion fin pitches, and metal 1 (met1) interconnect structures in the met1 layer are positioned in accordance with a met1 pitch arrangement that can include one or more met1 pitches, where one or more of the diffusion fin pitches are related to one or more of the met1 pitches by a rational number (x/y), where x and y are integer values. In some embodiments, a relationship between a diffusion fin pitch and a met1 pitch is defined by a rational number within a range extending from $(1/4)$ to $(4/1)$.

[00115] Also, in some embodiments, vertical local interconnect structures (liv) can be positioned in accordance with a vertical local interconnect pitch that is substantially equal to the gate electrode pitch. In some embodiments, the gate electrode pitch is less than 100 nanometers. Also, in a manner similar to that discussed above with regard to the diffusion fin pitch-to-met1 pitch relationship, in some embodiments the diffusion fin pitch arrangement can be related to the horizontal local interconnect pitch arrangement by a rational number (x/y), where x and y are integer values. That is, one or more diffusion fin pitches can be related to one or more horizontal local interconnect pitches by a rational number (x/y).

[00116] Figure 9A shows an example standard cell layout in which diffusion fins are utilized as interconnect conductors, in accordance with some embodiments of the present invention. Figure 9C shows a circuit schematic of the layout of Figure 9A. The example standard cell layout of Figure 9A includes multiple gate electrode line ends in a single track,

such as in the gate electrode track 9001. Figure 9B shows the layout of Figure 9A with three sets of cross-coupled transistors identified. The first set of cross-coupled transistors is identified by the pair of lines cc1a and cc1b. The second set of cross-coupled transistors is identified by the pair of lines cc2a and cc2b. The third set of cross-coupled transistors is identified by the pair of lines cc3a and cc3b.

[00117] Figure 10 shows an example standard cell layout with gate electrode contacts positioned substantially over the diffusion fins, instead of between the diffusion fins, in accordance with some embodiments of the present invention. The example standard cell layout of Figure 10 also shows variable-width met1 local power structures. In the example standard cell layout of Figure 10, the contact layer is vertically aligned over the diffusion fins instead of between them. This technique could enable sharing on an abutment edge between diffusion fin structures without a dummy diffusion fin, providing a more efficient layout. It should be understood that a dummy diffusion fin is a diffusion fin that does not form a transistor. Also, it should be appreciated that this technique of vertically aligning the contact layer over the diffusion fins can change the vertical alignment relationship between the met1 interconnect structures and the diffusion fins.

[00118] Figure 11 shows an example cell layout implementing diffusion fins, in accordance with some embodiments of the present invention. In the example layout of Figure 11, the gate electrode layer includes the following features:

- substantially linear gate electrode structures,
- three or more linear-shaped gate electrode structures on gate electrode layer, two of which are dummies, i.e., gate electrode level structures that do not form a gate electrode of a transistor,
- three or more gate electrode structures on gate electrode layer that have the same vertical dimension (length), i.e., same length in the y direction perpendicular to the lengthwise direction of the diffusion fins (x direction),
- gate electrode structures on gate electrode layer substantially evenly spaced at substantially equal lengthwise centerline-to-lengthwise centerline pitch,
- dummy gate electrode structures shared with adjacent cell on left and/or right, and
- dummy gate electrode structures cut under met1 power rails.

[00119] In the example layout of Figure 11, the diffusion fins include the following features:

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- substantially evenly spaced diffusion fins in accordance with substantially equal pitch, diffusion fins can be on a grid, diffusion fin pitch less than 90 nm in some embodiments,
- one or more diffusion fins for each of p-type and n-type, Figure 11 shows two diffusion fins of n-type and two diffusion fins of p-type, but other embodiments can include any number of diffusion fins of either type,
- same number of p-type and n-type diffusion fins, other embodiments may have different number of p-type versus n-type diffusion fins
- one or more diffusion fins omitted under power rails,
- one or more diffusion fins omitted between p-type and n-type sections, and
- each diffusion fin of substantially equal width and length.

[00120] In the example layout of Figure 11, the local interconnect include the following features:

- gate electrodes and diffusion fin source/drain connections are on different conductor layers, and these different conductor layers are isolated from each other,
- substantially linear conductor layer parallel to gate for source drain connection; in some embodiments, on same pitch as gate layer; and in some embodiments, this linear conductor layer may be offset by the gate half-pitch.
- positive overlap of local interconnect with diffusion fins.

[00121] In the example layout of Figure 11, the higher level met1 interconnect layer includes the following features:

- gate conductor contact between p-type and n-type diffusion fins,
- contacts gridded in both directions,
- contacts connect local interconnect and gate conductors to the metal layer above,
- substantially linear metal; metal on a pitch; metal on a pitch that is same as diffusion fin pitch with half-pitch offset vertically,
- output node and input node pins on same layer,
- wide power rails on top and bottom edges, each shared; power rails connect to left and right by abutment,
- output and input nodes on highest metal level; contacts positioned between p-type and n-type diffusion fins, and
- power rail contacts to local interconnect shared with abutting cells on top and bottom.

[00122] Figures 12A/B show a variation of the layout of Figure 11 having minimum width met1 power rails, in accordance with some embodiments of the present invention. Figure 12B shows the same layout as Figure 12A, with the layout depicted in a merged format for clarity. The example layout of Figures 12A/B also has all met1 of the same width, on the same pitch, including the power rails. Also, in the layout of Figures 12/B, met1 is positioned at the same (y) direction locations as the diffusion fin pitch.

[00123] Figures 13A/B show a variation of the layout of Figures 12A/B that does not have contacts from each of local interconnect and gate electrode structures to met1, in accordance with some embodiments of the present invention. Figure 13B shows the same layout as Figure 13A, with the layout depicted in a merged format for clarity. In this embodiment, met1 is formed to directly connect with the local interconnect and gate electrode structures. Also, in other embodiments, either the local interconnect structure, gate electrode structures, or both local interconnect and gate electrode structures can directly connect to met1.

[00124] Figures 14A/B show a variation of the layout of Figure 11 having minimum width met1 power rails, with all met1 structures of the same width and on the same pitch, including the power rails, in accordance with some embodiments of the present invention. Figure 14B shows the same layout as Figure 14A, with the layout depicted in a merged format for clarity.

[00125] Figures 15A/B show a variation of the layout of Figures 14A/B having met1 routing structures populated so each (y) location has a met1 structure, in accordance with some embodiments of the present invention. Figure 15B shows the same layout as Figure 15A, with the layout depicted in a merged format for clarity.

[00126] Figures 16A/B show a variation of the layout of Figure 11 having gate electrode structure contacts placed between p-type diffusion fins, in accordance with some embodiments of the present invention. Figure 16B shows the same layout as Figure 16A, with the layout depicted in a merged format for clarity. The example layout of Figures 16A/B also shows diffusion fins positioned under the met1 power rails and connected to VSS/VDD. Also, the diffusion fin VDD/VSS structures are shared with the cells above and/or below. For ease of illustration, the contact layer is not shown in the layout of Figures 16A/B.

[00127] Figures 17A/B show an example cell layout implementing diffusion fins, in accordance with some embodiments of the present invention. Figure 17B shows the same layout as Figure 17A, with the layout depicted in a merged format for clarity. In the example layout of Figures 17A/B, the gate electrode layer includes the following features:

- substantially linear gate electrode structures,

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- three or more linear structures on gate electrode layer, at least two of which are dummies,
- dummy structures on gate electrode layer are of same vertical dimension (length), i.e., same length in the y direction perpendicular to the lengthwise direction of the diffusion fins (x direction),
- structures on gate electrode layer substantially evenly spaced and/or equal pitched in x direction,
- dummy structures shared with adjacent cell on left and/or right,
- dummy structures as well as gate electrode structures drawn as a single line and then cut under power rails as well as where needed; gate electrode structure cuts drawn on separate layer; gate electrode layer shown as final result with cuts in Figures 17A/B,
- three or more segments of gate electrode, controlling two or more type p-type and n-type transistors,
- multiple gate electrodes structures in the same x location, each connected to a different net; and connected to two different input nets.

[00128] In the example layout of Figures 17A/B, the diffusion fins include the following features:

- substantially evenly spaced diffusion fins in accordance with substantially equal pitch, diffusion fins can be on a grid, diffusion fin pitch less than 90 nm in some embodiments,
- one or more diffusion fins for each of p-type and n-type,
- same number of p-type and n-type diffusion fins,
- shared diffusion fins under power rails,
- diffusion fins may or may not be omitted between p-type and n-type sections; Figures 17A/B show all fins present,
- each diffusion fin of substantially equal width and length, with the diffusion fin width measured in the y direction and the diffusion fin length measured in the x direction,
- diffusion fins drawn as continuous lines; separate cut mask drawn to separate them into segments; Figures 17A/B show diffusion fin segments after separation; it should be understood that in some embodiments the diffusion fin line ends can be drawn in the diffusion fin level layout or formed using the cut mask.

[00129] In the example layout of Figures 17A/B, the local interconnect include the following features:

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- gate electrodes and diffusion fin source/drain connections are on different conductor layers; these different conductor layers may be merged during fabrication,
- substantially linear conductor layer parallel to gate for source drain connection; in some embodiments, on same pitch as gate layer; and in some embodiments, this linear conductor layer may be offset by the gate half-pitch.
- positive, zero, or negative overlap of local interconnect with diffusion fins,
- direct connection of local interconnect to diffusion fin source/drain and gate electrode structures,
- shared local interconnect under power rail; local interconnect under power rail may be omitted in some embodiments.

[00130] In the example layout of Figures 17A/B, the higher level met1 interconnect layer includes the following features:

- gate electrode structure contact between diffusion fins,
- contacts gridded in one or both of the x and y directions,
- contacts connect local interconnect and gate conductors to the metal layer above,
- metal locations may be fixed in one or both of x and y directions,
- output node and input node pins on same layer,
- wide power rails on top and bottom are shared; power rails connect to left and right by abutment; power rails contact to local interconnect are shared,
- metal can have bends. In some embodiments, the bends in metal interconnect can be centered between adjacent diffusion fins. Also, in some embodiments, the vertical segments of the metal interconnect that extend in the y direction can be aligned with the vertical local interconnect so as to extend along an over the vertical local interconnect in the y direction.

[00131] Figures 18A/B show a variation of the layout of Figures 17A/B in which the contacts connect to the horizontal local interconnect, and in which the horizontal local interconnect connects directly to the vertical local interconnect, in accordance with some embodiments of the present invention. Figure 18B shows the same layout as Figure 18A, with the layout depicted in a merged format for clarity. In the layout of Figures 18A/B, the cuts on diffusion fin, gate electrode, and local interconnect layers are not shown.

[00132] Figures 19A/B show a variation of the layout of Figures 17A/B in which the power rail contact to local interconnect are not shared, and in which there is no shared local interconnect under the power rails, in accordance with some embodiments of the present

invention. Figure 19B shows the same layout as Figure 19A, with the layout depicted in a merged format for clarity.

[00133] Figures 20A/B show a variation of the layout of Figures 19A/B in which the diffusion fins are offset by a diffusion fin half-pitch with respect to the cell boundary, in accordance with some embodiments of the present invention. Figure 20B shows the same layout as Figure 20A, with the layout depicted in a merged format for clarity. The layout of Figures 20A/B also includes diffusion fin locations which are the same as the met1 locations. Also, the diffusion fins are not shared on the top and bottom of the cell. Figures 20A/B also show the contacts positioned on the top of the gate electrodes and diffusion fins. Figures 20A/B also show different diffusion fin/local interconnect overlaps. It should be understood that in the particular layout of Figures 20A/B, although the horizontal local interconnect lih and vertical local interconnect liv are shown to overlap each other in region 2001, the horizontal local interconnect lih and vertical local interconnect liv do not contact each other in region 2001. This is also true for region 2001 in Figures 21A/B to follow. However, it should also be understood that in some other layouts, the horizontal local interconnect lih and vertical local interconnect liv can be made to contact each other at locations where they cross each other.

[00134] Figures 21A/B show a variation of the layout of Figures 20A/B having minimum width power rails and negative vertical local interconnect overlap of the diffusion fins, in accordance with some embodiments of the present invention. Figure 21B shows the same layout as Figure 21A, with the layout depicted in a merged format for clarity.

[00135] Figures 22A/B show a variation of the layout of Figures 17A/B having minimum width power rails, no shared local interconnect or diffusion fins under the power rails, and a larger space between p-fins and n-fins, in accordance with some embodiments of the present invention. Figure 22B shows the same layout as Figure 22A, with the layout depicted in a merged format for clarity.

[00136] Figures 23A/B show a variation of the layout of Figures 17A/B, in accordance with some embodiments of the present invention. Figure 23B shows the same layout as Figure 23A, with the layout depicted in a merged format for clarity. The layout of Figures 23A/B has the following features:

- uni-directional metal interconnect structures, i.e., linear-shaped metal interconnect structures,
- no shared local interconnect or fins under power rails,

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- one input pin on highest metal layer, and another input pin and the output pin on the metal layer below,
- gate electrode contact isolated from local interconnect.

[00137] Also, Figures 23A/B show the diffusion fins before they are cut on the left and
5 right edges.

[00138] Figures 24A/B show a variation of the layout of Figures 23A/B, in accordance with some embodiments of the present invention. Figure 24B shows the same layout as Figure 24A, with the layout depicted in a merged format for clarity. The layout of Figures 24A/B has the following features:

- 10 • diffusion fin pitch smaller than metal pitch; diffusion fin pitch one-half of the metal pitch,
- gate electrode and local interconnect cuts shown between diffusion fins; an alternate implementation can have cuts above diffusion fin cuts; this would reduce number of diffusion fins in one or more transistors,
- 15 • one input pin on highest metal layer, another input pin and the output pin on the metal layer below,
- spacing between p-type and n-type diffusion fins larger than minimum; one or more diffusion fins omitted between p-type and n-type diffusion fin sections,
- gate electrode contact placed on diffusion fin,
- 20 • local interconnect contact placed on diffusion fin, and
- vertical met2 has a different offset in the x direction within the cell.

[00139] Figures 25A/B show a variation of the layout of Figures 23A/B, in which the cell is doubled in height, in accordance with some embodiments of the present invention. Figure 25B shows the same layout as Figure 25A, with the layout depicted in a merged format
25 for clarity. The layout of Figures 25A/B includes twice the total number of diffusion fins in the layout of Figure 23A/B. The diffusion fin cuts are shown in the layout of Figure 25A/B.

[00140] Figures 26A/B show an example cell layout implementing diffusion fins, in accordance with some embodiments of the present invention. Figure 26B shows the same layout as Figure 26A, with the layout depicted in a merged format for clarity. In the example
30 layout of Figures 26A/B, the gate electrode layer includes the following features:

- substantially linear gate electrode structures,
- three or more linear structures on gate electrode layer, at least two of which are dummies,

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- dummy structures on gate electrode layer are of same dimension,
- structures on gate electrode layer substantially evenly spaced and/or equal pitched in x direction,
- dummy structures shared with adjacent cell on left and/or right,
- 5 • dummy structures cut under power rails,
- single gate electrode structure controlling two or more p-type and n-type transistors, to be separated later in the manufacturing process to form two or more distinct gate electrodes, such as depicted by gate electrode structures 2601 and 2603,
- gate electrodes in the same x location connected to two or more different nets,
- 10 connected to two or more different input nets, such as depicted by gate electrode structure 2601 connected to input net 2605, and by gate electrode structure 2603 connected to input net 2607, and
- two or more dummy segments in same x location.

[00141] In the example layout of Figures 26A/B, the diffusion fins include the following
15 features:

- substantially evenly spaced diffusion fins in accordance with substantially equal pitch, diffusion fins can be on a grid, diffusion fin pitch less than 90 nm in some embodiments,
- one or more diffusion fins for each of p-type and n-type,
- 20 • same number of p-type and n-type diffusion fins,
- one or more diffusion fins omitted under power rails,
- no diffusion fins omitted between p-type and n-type sections,
- each diffusion fin of substantially equal width and length, and
- p-type diffusion fins positioned between n-type diffusion fins, vice-versa.

25 [00142] In the example layout of Figures 26A/B, the local interconnect include the following features:

- gate electrodes and diffusion fin source/drain connections are on different conductor layers; these different conductor layers are isolated from each other,
- substantially linear conductor layer parallel to gate for source drain connection; in some
30 embodiments, on same pitch as gate layer; and in some embodiments, this linear conductor layer may be offset by the gate half-pitch, and
- positive overlap of local interconnect with diffusion fins.

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[00143] In the example layout of Figures 26A/B, the higher level met1 interconnect layer includes the following features:

- gate electrode structure contact between diffusion fins,
- contacts gridded in one or both of the x and y directions,
- 5 • contacts connect local interconnect and gate conductors to the metal layer above,
- substantially linear-shaped conductor on output node,
- output node and input node pins on different layers,
- power rail in middle, opposite power rail at top and bottom; top and bottom power rails shared; all power rails connect to left and right by abutment, and
- 10 • output node on highest metal level.

[00144] Figures 27A/B show a variation of the layout of Figures 26A/B, in accordance with some embodiments of the present invention. Figure 27B shows the same layout as Figure 27A, with the layout depicted in a merged format for clarity. The layout of Figures 27A/B includes the following features:

- 15 • gate conductor is drawn with a cut layer, such as a cut layer that includes the cut shape 2701,
- two gate conductor segments at same x location, each connecting to a different net, each connected to an input net, each controlling a p-type and an n-type transistor constructed with multiple fins, such as gate conductors 2703 and 2705, and
- 20 • one input pin on highest metal layer, another input pin and the output pin on the metal layer below.

[00145] Figures 28A/B show an example cell layout implementing diffusion fins, in accordance with some embodiments of the present invention. Figure 28B shows the same layout as Figure 28A, with the layout depicted in a merged format for clarity. In the example layout of Figures 28A/B, the gate electrode layer includes the following features:

- substantially linear gate electrode structures,
- three or more linear structures on gate electrode layer, at least two of which are dummies,
- three or more gate electrode structures are of same dimension,
- 30 • structures on gate electrode layer substantially evenly spaced and/or equal pitched in x direction,
- dummy structures shared with adjacent cell on left and/or right,
- dummy structures cut under power rails,

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[00146] It should be understood that any of the figures presented herein, including the example layout of Figures 28A/B, can have the type 1 diffusion fins defined as p-type diffusion fins and the type 2 diffusion fins defined as n-type diffusion fins, or can have the type 1 diffusion fins defined as n-type diffusion fins and the type 2 diffusion fins defined as p-type diffusion fins, depending on the particular implementation embodiment. In the example layout of Figures 28A/B, the diffusion fins include the following features:

- substantially evenly spaced diffusion fins in accordance with substantially equal pitch, diffusion fins can be on a grid, diffusion fin pitch less than 90 nm in some embodiments,
- one or more diffusion fins for each of p-type and n-type,
- different number of p-type and n-type diffusion fins,
- one or more diffusion fins omitted under power rails,
- one or more diffusion fins omitted between p-type and n-type sections,
- each diffusion fin of substantially equal width and length.

[00147] In the example layout of Figures 28A/B, the local interconnect include the following features:

- gate electrodes and diffusion fin source/drain connections are directly from a conductor layer,
- substantially linear conductor layer parallel to gate for source drain connection; in some embodiments, on same pitch as gate layer; and in some embodiments, this linear conductor layer may be offset by the gate half-pitch,
- zero or negative overlap of local interconnect with diffusion fins and gate electrode structures,
- local interconnect can be constructed in two steps, vertical local interconnect structures first, followed by horizontal local interconnect structures; each of the steps creates a set of linear, uni-directional local interconnect structures, and
- alternatively, two separate local interconnect layers -- one vertical local interconnect layer, and one horizontal local interconnect layer.

[00148] In the example layout of Figures 28A/B, the higher level met1 interconnect layer includes the following features:

- diffusion fins can be positioned underneath the power rails
- contacts gridded in one or both of the x and y directions,
- contacts connect all local interconnects to the metal layer above, and

- contacts can be placed anywhere.

[00149] Figures 29A/B show a variation of the layout of Figures 28A/B in which there are no local interconnect structures present between two gate electrode structures of n-type transistors, in accordance with some embodiments of the present invention. Figure 29B shows the same layout as Figure 29A, with the layout depicted in a merged format for clarity.

[00150] Figures 30A/B show an example cell layout implementing diffusion fins, in accordance with some embodiments of the present invention. Figure 30B shows the same layout as Figure 30A, with the layout depicted in a merged format for clarity. In the example layout of Figures 30A/B, the gate electrode layer includes the following features:

- substantially linear gate electrode structures,
- three or more linear structures on gate electrode layer, at least two of which are dummies,
- three or more gate electrode structures are of same dimension,
- structures on gate electrode layer substantially evenly spaced and/or equal pitched in x direction,
- dummy structures shared with adjacent cell on left and/or right,
- dummy structures cut under power rails,

[00151] In the example layout of Figures 30A/B, the diffusion fins include the following features:

- substantially evenly spaced diffusion fins in accordance with substantially equal pitch, diffusion fins can be on a grid, diffusion fin pitch less than 90 nm in some embodiments,
- one or more diffusion fins for each of p-type and n-type,
- same number of p-type and n-type diffusion fins,
- one or more diffusion fins omitted under power rails,
- one or more diffusion fins omitted between p-type and n-type sections,
- each diffusion fin of substantially equal width and length.

[00152] In the example layout of Figures 30A/B, the local interconnect include the following features:

- gate electrodes and diffusion fin source/drain connections are directly from a conductor layer,

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- substantially linear conductor layer parallel to gate for source drain connection; in some embodiments, on same pitch as gate layer; and in some embodiments, this linear conductor layer may be offset by the gate half-pitch,
- zero or negative overlap of local interconnect with diffusion fins and gate electrode structures,
- local interconnect can be constructed in two steps, vertical local interconnect structures first, followed by horizontal local interconnect structures; each of the steps creates a set of linear, uni-directional local interconnect structures, and
- in some embodiments, vertical and horizontal local interconnect structures can be formed to cross and connect with each other, thereby forming a two-dimensionally varying local interconnect structure, i.e., a local interconnect structure with bends,
- alternatively, two separate local interconnect layers -- one vertical local interconnect layer, and one horizontal local interconnect layer.

[00153] In the example layout of Figures 30A/B, the higher level met1 interconnect layer includes the following features:

- diffusion fins can be positioned underneath the power rails
- contacts gridded in one or both of the x and y directions,
- met1 interconnect structures are positioned in accordance with same pitch as gate electrode structures,
- contacts connect all local interconnects to the metal layer above, and
- contacts can be placed anywhere.

[00154] Figure 31A shows an example sdf cell layout with gate electrode and local interconnect line end gaps centered substantially between diffusion fins, in accordance with some embodiments of the present invention. In Figure 31A, the gate electrode line end gaps are circled. Figure 31B shows the example sdf cell layout of Figure 31A, with the local interconnect line end gaps centered substantially between the diffusion fins circled. Based on Figures 31A through 31B, it should be understood that a cell library architecture can be generated in which all gate electrode and vertical interconnect line end gaps are centered substantially between the diffusion fins. Figure 31C shows the example sdf cell layout of Figures 31A and 31B with annotation of the region 3105 between two adjacent gate electrode structures in which the diffusion fin ends overlap each other in the x direction, in accordance with some embodiments of the present invention.

[00155] Figures 32-34 show three examples of a part of a standard cell circuit layout, in accordance with some embodiments of the present invention. Figure 32 shows an example layout in which all contact layer structures are placed between the diffusion fins. Figures 33 and 34 shows example layouts in which all contact layer structures are placed on the diffusion fins. In the example of Figure 32, the gate electrode line end gaps in some instances are substantially centered over the diffusion fins, as noted by circles 3201, and in some instances the gate electrode line end gaps are substantially centered between the diffusion fins, as noted by circles 3203. By using a cell architecture that places all of the contact layer structures over the diffusion fins, all gate electrode line end gaps can be substantially centered between the diffusion fins, as noted by circles 3301 in Figures 33 and 34. One benefit here is that the gate electrode line end gaps are all on a fixed pitch. From a manufacturing perspective, it does not matter whether the gate electrode line end gaps are centered on the diffusion fins or between the diffusion fins. However, it does matter that the gate electrode line end gaps are not mixed, as in the example of Figure 32. Having the gate electrode line end gaps all on the same pitch should result in a gate electrode manufacturing process that is either less expensive, more reliable or both.

[00156] Figures 35A-69A show various cell layouts which demonstrate examples of different ways in which a cross-coupled transistor configuration can be implemented using finfet transistors. The cross-couple layouts of Figures 35A-69A are shown in the context of a two-input multiplexor circuit (MUX2). Figure 35C shows a circuit schematic of the layouts of Figures 35A/B through 47A/B and 63A/B through 67A/B, in accordance with some embodiments of the present invention. Figure 48C shows a circuit schematic of the layouts of Figures 48A/B through 58A/B, in accordance with some embodiments of the present invention. Figure 59C shows a circuit schematic of the layout of Figures 59A/B, in accordance with some embodiments of the present invention. Figure 60C shows a circuit schematic of the layouts of Figures 60A/B through 62A/B and Figures 68A/B through 69A/B, in accordance with some embodiments of the present invention. Figure 71C shows a circuit schematic of the layouts of Figures 71A/B and 77A/B, in accordance with some embodiments of the present invention. Figure 72C shows a circuit schematic of the layouts of Figures 72A/B through 76A/B, in accordance with some embodiments of the present invention. The transistors on the left and right edges are added to the cross-couple to achieve MUX2 functionality. For other functions with cross-couple circuits, these may be different. Figures 35B-69B show the same layouts as Figures 35A-69A, respectively, with the layouts depicted in a merged format for clarity, and

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with the nodes of the circuit identified based on the cell layout's circuit schematic. Also, cross-coupled transistor connections are identified in Figures 35A-69A by lines cc1 and cc2.

[00157] Figures 35A/B through 47A/B and 63A/B through 67A/B show cross-couple transistor configurations having transmission gate in both logic paths, requiring all the internal nodes to have a connection between p-type and n-type. Figures 48A/B through 57A/B show cross-couple transistor configurations having transmission gate in the logic path with larger transistors, and tristate gate in other paths. Tristate gate does not require a connection between p-type diffusion and n-type diffusion on the internal node.

[00158] Figures 58A/B through 59A/B show cross-couple transistor configurations having transmission gate in the logic path with smaller transistors, and tristate gate in other paths. Tristate gate does not require a connection between p-type diffusion and n-type diffusion on the internal node.

[00159] Figures 60A/B through 62A/B and 68A/B through 69A/B show cross-couple transistor configurations having tristate gate in both logic paths.

[00160] Figures 63A/B through 69A/B show cell layouts that have a number of p-type diffusion fins equal to a number of n-type diffusion fins. Some of the other Figures 35A/B through 62A/B show cell layouts that a number of p-type diffusion fins not equal to a number of n-type diffusion fins.

[00161] Figures 40A/B shows a cell layout that utilizes tighter spacing between horizontal/vertical local interconnect structures. Figures 37A/B, 45A/B, and 49A/B show cell layout examples that utilize a larger spacing between diffusion fins. Figures 63A/B through 69A/B show cell layout examples that utilize tighter spacing between diffusion fins. Figures 43A/B and 44A/B show cell layout examples that utilize a diffusion fin as a wire.

[00162] Figures 35A/B through 41A/B, 48A/B through 65A/B, and 68A/B through 69A/B shows cell layout examples that utilize a dense gate electrode structure implementation without split gates. Figures 42A/B through 47A/B and 66A/B through 67A/B show cell layout examples that utilize a split gate implementation with less wiring and larger transistor sizes.

[00163] Figures 35A/B through 69A/B show cell layout examples that demonstrate a number of different wiring examples for various cell layouts. Figures 35A/B through 69A/B show cell layout examples that demonstrate use of a fully populated gate electrode layer, including extension of gate electrode end caps and use of dummy structures where possible within the gate electrode layer. Some of the cell layouts shown in Figures 35A/B through 69A/B show examples of dummy gate electrode layer structures without the cuts at the top and bottom of the cell, i.e., prior to cut mask operation during the fabrication process. Some of the

cell layouts, e.g., Figures 53A/B through 55A/B and 66A/B shows example cell layouts where power buses are omitted.

[00164] These cross-coupled transistor configuration of Figures 35A/B through 69A/B include structures formed on each layer as well as on a combination of layers, and many of the cell layout features mentioned above can be applied independent of each other. It should be understood that the cell layouts of Figures 35A/B through 69A/B show examples of what can be done with the finfet-based cross-coupled transistor configuration, and in no way represent an all inclusive set of possible cell layout configurations. Any of the features demonstrated in the various cell layout examples of Figures 35A/B through 69A/B can be combined to generate additional cell layouts.

[00165] Technologies for which the optical resolution is not sufficient to resolve line patterns directly will use some form of pitch division. The pitch division can be self-aligned, using spacers, or through multiple exposure steps at an achievable resolution. For example, for an ArF excimer laser scanner using water immersion of the final lens and a portion of the wafer to be exposed, the optical resolution is limited to ~40nm. This corresponds to a k_1 value of 0.28 for a wavelength of 193 nm and an effective numerical aperture of 1.35. For diffusion fin layers and gate electrode layers and other layers formed with pitch division (for example, spacer double patterning, spacer quadruple patterning, multiple exposure Litho-Etch-Litho-Etch, etc...), even though the layout is done with uniform pitches (lengthwise centerline-to-lengthwise centerline pitches) for the conductive structures, i.e., for the lines, the as-fabricated conductive structures can end up slightly off target due to processing variations, such that multiple (e.g., two, four, etc...) pitches end up on the wafer.

[00166] Pitch division can be applied multiple times, for example pitch-division-by-2, pitch-division-by-4, with either the self-aligned spacer approach or multiple lithographic exposures. Pitch-division-by-4 has been reported to achieve lines/spaces of about 11 nm. One limitation of pitch division is that the resultant line patterns can have slightly different pitches within a pattern. For pitch-division-by-2, this means that groups of two lines will have one pitch, the next group of two lines can have a slightly different pitch, the next group of two lines will have the same pitch as the first group, etc. The result on a finished wafer will be lines which were intended to be on a uniform, fixed pitch but will end up on two or four or other multiple pitches. For self-aligned spacers, the original core line pattern will be drawn on a fixed, uniform pitch. For multiple exposures, each of the exposures will have lines drawn on a uniform fixed pitch. The non-uniform pitch introduced by the pitch division process may be on

the order of 10% or less of the final pitch. For example, for a final target pitch of 50 nm, the pitches of each group of two lines may differ by less than 5 nm.

Restricted Gate Level Layout Architecture

[00167] The various circuit layouts incorporating finfet transistors, as discussed above,
5 can be implemented within a restricted gate level layout architecture. For the gate level, a number of parallel virtual lines are defined to extend across the layout. These parallel virtual lines are referred to as gate electrode tracks, as they are used to index placement of gate electrodes of various transistors within the layout. In some embodiments, the parallel virtual lines which form the gate electrode tracks are defined by a perpendicular spacing therebetween
10 equal to a specified gate electrode pitch. Therefore, placement of gate electrode segments on the gate electrode tracks corresponds to the specified gate electrode pitch. In another embodiment, the gate electrode tracks can be spaced at variable pitches greater than or equal to a specified gate electrode pitch.

[00168] Figure 70A shows an example of gate electrode tracks 70-1A through 70-1E
15 defined within the restricted gate level layout architecture, in accordance with some embodiments of the present invention. Gate electrode tracks 70-1A through 70-1E are formed by parallel virtual lines that extend across the gate level layout of the chip, with a perpendicular spacing therebetween equal to a specified gate electrode pitch 70-3.

[00169] Within the restricted gate level layout architecture, a gate level feature layout
20 channel is defined about a given gate electrode track so as to extend between gate electrode tracks adjacent to the given gate electrode track. For example, gate level feature layout channels 70-5A through 70-5E are defined about gate electrode tracks 70-1A through 70-1E, respectively. It should be understood that each gate electrode track has a corresponding gate level feature layout channel. Also, for gate electrode tracks positioned adjacent to an edge of a
25 prescribed layout space, e.g., adjacent to a cell boundary, the corresponding gate level feature layout channel extends as if there were a virtual gate electrode track outside the prescribed layout space, as illustrated by gate level feature layout channels 70-5A and 70-5E. It should be further understood that each gate level feature layout channel is defined to extend along an entire length of its corresponding gate electrode track. Thus, each gate level feature layout
30 channel is defined to extend across the gate level layout within the portion of the chip to which the gate level layout is associated.

[00170] Within the restricted gate level layout architecture, gate level features associated with a given gate electrode track are defined within the gate level feature layout channel associated with the given gate electrode track. A contiguous gate level feature can include both

a portion which defines a gate electrode of a transistor, i.e., of a finfet transistor as disclosed herein, and a portion that does not define a gate electrode of a transistor. Thus, a contiguous gate level feature can extend over both a diffusion region, i.e., diffusion fin, and a dielectric region of an underlying chip level.

5 [00171] In some embodiments, each portion of a gate level feature that forms a gate electrode of a transistor is positioned to be substantially centered upon a given gate electrode track. Furthermore, in this embodiment, portions of the gate level feature that do not form a gate electrode of a transistor can be positioned within the gate level feature layout channel associated with the given gate electrode track. Therefore, a given gate level feature can be
10 defined essentially anywhere within a given gate level feature layout channel, so long as gate electrode portions of the given gate level feature are centered upon the gate electrode track corresponding to the given gate level feature layout channel, and so long as the given gate level feature complies with design rule spacing requirements relative to other gate level features in adjacent gate level layout channels. Additionally, physical contact is prohibited between gate
15 level features defined in gate level feature layout channels that are associated with adjacent gate electrode tracks.

[00172] Figure 70B shows the exemplary restricted gate level layout architecture of Figure 70A with a number of exemplary gate level features 7001-7008 defined therein, in accordance with some embodiments of the present invention. The gate level feature 7001 is
20 defined within the gate level feature layout channel 70-5A associated with gate electrode track 70-1A. The gate electrode portions of gate level feature 7001 are substantially centered upon the gate electrode track 70-1A. Also, the non-gate electrode portions of gate level feature 7001 maintain design rule spacing requirements with gate level features 7002 and 7003 defined within adjacent gate level feature layout channel 70-5B. Similarly, gate level features 7002-
25 7008 are defined within their respective gate level feature layout channels, and have their gate electrode portions substantially centered upon the gate electrode track corresponding to their respective gate level feature layout channel. Also, it should be appreciated that each of gate level features 7002-7008 maintains design rule spacing requirements with gate level features defined within adjacent gate level feature layout channels, and avoids physical contact with
30 any another gate level feature defined within adjacent gate level feature layout channels.

[00173] A gate electrode corresponds to a portion of a respective gate level feature that extends over a diffusion structure, i.e., over a diffusion fin, wherein the respective gate level feature is defined in its entirety within a gate level feature layout channel. Each gate level feature is defined within its gate level feature layout channel without physically contacting

another gate level feature defined within an adjoining gate level feature layout channel. As illustrated by the example gate level feature layout channels 70-5A through 70-5E of Figure 70B, each gate level feature layout channel is associated with a given gate electrode track and corresponds to a layout region that extends along the given gate electrode track and perpendicularly outward in each opposing direction from the given gate electrode track to a closest of either an adjacent gate electrode track or a virtual gate electrode track outside a layout boundary.

[00174] Some gate level features may have one or more contact head portions defined at any number of locations along their length. A contact head portion of a given gate level feature is defined as a segment of the gate level feature having a height and a width of sufficient size to receive a gate contact structure. In this instance, "width" is defined across the substrate in a direction perpendicular to the gate electrode track of the given gate level feature, and "height" is defined across the substrate in a direction parallel to the gate electrode track of the given gate level feature. The gate level feature width and height may or may not correspond to the cell width W and cell height H, depending on the orientation of the gate level features within the cell. It should be appreciated that a contact head of a gate level feature, when viewed from above, can be defined by essentially any layout shape, including a square or a rectangle. Also, depending on layout requirements and circuit design, a given contact head portion of a gate level feature may or may not have a gate contact defined thereabove.

[00175] A gate level of the some embodiments disclosed herein is defined as a restricted gate level, as discussed above. Some of the gate level features form gate electrodes of transistor devices. Others of the gate level features can form conductive segments extending between two points within the gate level. Also, others of the gate level features may be non-functional with respect to integrated circuit operation. It should be understood that the each of the gate level features, regardless of function, is defined to extend across the gate level within their respective gate level feature layout channels without physically contacting other gate level features defined with adjacent gate level feature layout channels.

[00176] In some embodiments, the gate level features are defined to provide a finite number of controlled layout shape-to-shape lithographic interactions which can be accurately predicted and optimized for in manufacturing and design processes. In this embodiment, the gate level features are defined to avoid layout shape-to-shape spatial relationships which would introduce adverse lithographic interaction within the layout that cannot be accurately predicted and mitigated with high probability. However, it should be understood that changes in

direction of gate level features within their gate level layout channels are acceptable when corresponding lithographic interactions are predictable and manageable.

[00177] It should be understood that each of the gate level features, regardless of function, is defined such that no gate level feature along a given gate electrode track is configured to connect directly within the gate level to another gate level feature defined along a different gate electrode track without utilizing a non-gate level feature. Moreover, each connection between gate level features that are placed within different gate level layout channels associated with different gate electrode tracks is made through one or more non-gate level features, which may be defined in higher interconnect levels, i.e., through one or more interconnect levels above the gate level, or by way of local interconnect features at or below the gate level.

[00178] Figures 71A/B through 77A/B show a number of example SDFF circuit layouts that utilize both tri-state and transmission gate based cross-coupled circuit structures, in accordance with some embodiments of the present invention. Figure 71C shows a circuit schematic for Figures 71A/B and 77A/B, in accordance with some embodiments of the present invention. Figure 72C shows a circuit schematic for Figures 73A/B through 76A/B, in accordance with some embodiments of the present invention. Figures 71B-77B show the same layouts as Figures 71A-77A, respectively, with the layouts depicted in a merged format for clarity, and with the nodes of the circuit identified based on the cell layout's circuit schematic. The example SDFF circuit layouts of Figures 71A/B through 77A/B include the following features:

1. Gate conductors:

- a. Substantially evenly spaced gate conductors.
- b. Uniform gate conductor line end gaps formed with cut mask, combined with large gate conductor line end gaps to avoid local interconnect, or if there is sufficient space to permit larger gate conductor line end gaps that do not require cuts.
- c. Some gate conductors used as wires in some instances to reduce metal usage, i.e., to reduce higher level interconnect usage.

2. Diffusion fins:

- a. Substantially evenly spaced diffusion fins.
- b. Diffusion fins omitted between p-type and n-type, and on top and bottom cell edges.

- c. Diffusion fin width-to-space relationship may vary, or may have a substantially equal relationship such as depicted in the examples of Figures 71A/B through 77A/B.

3. Local interconnect:

- 5 a. Local interconnect structures can connect directly to diffusion fins and gate conductors.
- b. Local interconnect structures can connect to metal 1 (met1 or M1) through a contact layer.
- 10 c. Horizontal and vertical local interconnect structures, such as shown in Figures 76A/B by way of example, can be fabricated using separate design layers, i.e., fabricated using separate mask layers.
- d. Horizontal and vertical local interconnect structures can be on the same layer, i.e., on the same mask layer, as shown in the examples of Figures 71A/B through 75A/B and 77A/B. Also, during manufacturing, the horizontal and
- 15 vertical local interconnect structures can be fabricated in two distinct steps, or in a single step.
- e. Local interconnect structures can have positive, zero, or negative overlap with diffusion fins and gate conductors.
- f. Vertical local interconnect can be on similar pitch as gate conductor with half-
- 20 pitch offset from gate conductors.

4. Contacts:

- a. Contacts can be defined to connect local interconnect structures to metal 1 (met1 or M1).
- 25 b. Local interconnect structures can have positive, zero, or negative overlap on contact.
- c. Metal 1 (met1 or M1) can have positive, zero, or negative overlap on contact.

5. Metal 2 (met2 or M2)

- a. Metal 2 structures can be uni-directional, i.e., linear-shaped, in some embodiments.
- 30 b. Metal 2 structures can extend in horizontal (x) and/or vertical (y) directions.

[00179] The example SDFF circuit layout of Figures 71A/B shows the following features, among others:

- Metal 2 is not used for internal wiring.
- Metal 2 is used for power rails.

- Tri-state and transmission gate cross-coupled transistor structures are utilized.
 - Local interconnect structures extend in both horizontal (x) and vertical (y) directions.
 - Some gate conductors are used as wires, and do not form a gate electrode of a transistor.
- 5 • Gate conductor cuts are provided in various locations and combinations.
- Gate conductor cuts are uniform in size.
- Gate conductor layer is fully populated, i.e., at least one gate conductor is positioned at each available gate conductor pitch position within the cell.

[00180] The example SDFF circuit layout of Figures 72A/B shows the following
 10 features, among others:

- Metal 2 structures are used for internal wiring in vertical (y) direction.
- Denser circuit layout than the example of Figures 71A/B.
- Both tri-state and transmission gate cross-coupled transistor structures are utilized.
- Gate conductor layer is fully populated, i.e., at least one gate conductor is positioned at
 15 each available gate conductor pitch position within the cell.
- Gate conductor cuts are shown.
- Substantially uniform gate conductor cuts are utilized in various combinations and/or locations to optimize layout.

[00181] The example SDFF circuit layout of Figures 73A/B shows a version of the
 20 SDFF circuit that uses both the gate conductor and metal 2 layers for vertical (y-direction) wiring. The example SDFF circuit layout of Figures 74A/B shows a version of the SDFF circuit that uses horizontally oriented, i.e., in the x-direction, metal 2 structures for internal wiring. The example SDFF circuit layout of Figures 75A/B shows an alternate version of the SDFF circuit that again uses horizontally oriented, i.e., in the x-direction, metal 2 structures for
 25 internal wiring. The example SDFF circuit layout of Figures 76A/B shows a variation of the layout of Figure 72A/B with horizontal local interconnect and vertical local interconnect used as separate conductors to allow for removal of the internal metal 2 conductors. The example SDFF circuit layout of Figures 77A/B shows a partial SDFF layout illustrating an alternate way to define circuit structures so as to minimize use of metal 2 and maximize transistor density.

30 [00182] It should be understood based on the circuit layouts and description provided herein that in some embodiments one or more of the following features can be utilized:

- a separation distance between co-aligned and adjacently positioned diffusion fin ends (i.e., diffusion fin cut distance) can be less than a size of the gate electrode pitch,

- a vertical local interconnect structure may overlap a diffusion fin (that is horizontally oriented) on one edge (horizontally oriented edge) of the diffusion fin; in this case, some cuts (in a cut mask) used to separate vertical local interconnect structures can be defined to touch or overlap a diffusion fin,
- 5 • a horizontal local interconnect structure may overlap a gate electrode structure (that is vertically oriented) on one edge (vertically oriented edge) of the gate electrode structure,
- a size of a gate end cap (i.e., a distance by which a gate electrode structure extends beyond an underlying diffusion fin) can be less than a size of one or more diffusion fin pitches, or less than a size of an average diffusion fin pitch,
- 10 • a separation distance between co-aligned and adjacently positioned gate electrode structure ends (i.e., gate electrode structure cut distance) can be less than or equal to a size of one or more diffusion fin pitches, or less than a size of an average diffusion fin pitch,
- 15 • a lengthwise centerline separation distance between adjacently positioned n-type and p-type diffusion fins (as measured in the direction perpendicular to the diffusion fins) can be defined as an integer multiple of one or more diffusion fin pitches, or as an integer multiple of an average diffusion fin pitch.

[00183] In an example embodiment, a semiconductor device includes a substrate, a first transistor, and a second transistor. The first transistor has a source region and a drain region within a first diffusion fin. The first diffusion fin is structured to project from a surface of the substrate. The first diffusion fin is structured to extend lengthwise in a first direction from a first end of the first diffusion fin to a second end of the first diffusion fin. The second transistor has a source region and a drain region within a second diffusion fin. The second diffusion fin is structured to project from the surface of the substrate. The second diffusion fin is structured to extend lengthwise in the first direction from a first end of the second diffusion fin to a second end of the second diffusion fin. The second diffusion fin is positioned next to and spaced apart from the first diffusion fin. Also, either the first end or the second end of the second diffusion fin is positioned in the first direction between the first end and the second end of the first diffusion fin.

[00184] The above-mentioned first and second transistors can be located at different positions in the second direction. Also, each of the first and second transistors can be a three-dimensionally gated transistor.

[00185] The above-mentioned first transistor includes a first linear-shaped gate electrode structure that extends lengthwise in a second direction perpendicular to the first direction as viewed from above the substrate. The above-mentioned second transistor includes a second linear-shaped gate electrode structure that extends lengthwise in the second direction perpendicular to the first direction as viewed from above the substrate. At least one of the first and second ends of the first diffusion fin can be positioned in the first direction between the first and second linear-shaped gate electrode structures. And, at least one of the first and second ends of the second diffusion fin can be positioned in the first direction between the first and second linear-shaped gate electrode structures. The first linear-shaped gate electrode structure is positioned next to and spaced apart from the second linear-shaped gate electrode structure.

[00186] The semiconductor device can also include a linear-shaped local interconnect structure that extends in the second direction and that is positioned between the first and second linear-shaped gate electrode structures. The linear-shaped local interconnect structure can be substantially centered in the first direction between the first and second linear-shaped gate electrode structures. The linear-shaped local interconnect structure can connect to one or more of the first and second diffusion fins.

[00187] The semiconductor device can also include a linear-shaped local interconnect structure that extends in the first direction and that is positioned between the first and second diffusion fins. This linear-shaped local interconnect structure can be substantially centered in the second direction between the first and second diffusion fins. Also, this linear-shaped local interconnect structure can connect to one or more of the first and second gate electrode structures.

[00188] The above-mentioned linear-shaped local interconnect structure that extends in the first direction can be referred to as a first linear-shaped local interconnect structure. The semiconductor device can also include a second linear-shaped local interconnect structure that extends in the second direction and that is positioned between the first and second linear-shaped gate electrode structures. The second linear-shaped local interconnect structure can be substantially centered in the first direction between the first and second linear-shaped gate electrode structures. Also, the second linear-shaped local interconnect structure can connect to one or more of the first diffusion fin, the second diffusion fin. Additionally, in some embodiments, the first linear-shaped local interconnect structure can be a first linear segment of a two-dimensionally varying non-linear local interconnect structure, and the second linear-shaped local interconnect structure can be a second linear segment of the two-dimensionally

varying non-linear local interconnect structure. And, in some instances, the first and second linear-shaped local interconnect structures can be connected to each other.

[00189] The semiconductor device can also include a contact structure positioned between the first and second diffusion fins. In some embodiments, the contact structure can be substantially centered between the first and second diffusion fins. In some embodiments, the contact structure can connect to either the first gate electrode structure or the second gate electrode structure.

[00190] The semiconductor device can also include a contact structure positioned between the first and second gate electrode structures. In some embodiments, the contact structure can be substantially centered between the first and second gate electrode structures. Also, in some embodiments, the semiconductor device can include a conductive interconnect structure positioned in the second direction between first and second diffusion fins, where the contact structure connects to the conductive interconnect structure. In some embodiments, the conductive interconnect structure is a lowest level interconnect structure extending in the first direction that is not a diffusion fin.

[00191] The semiconductor device can also include a conductive interconnect structure positioned in the first direction between first and second diffusion fins, where the contact structure connects to a conductive interconnect structure. In some embodiments, the conductive interconnect structure is higher-level interconnect structure.

[00192] The semiconductor device can also include one or more interconnect structures, where some of the one or more interconnect structures include one or more interconnect segments that extend in the first direction. In some embodiments, some of the one or more interconnect segments that extend in the first direction are positioned between the first and second diffusion fins. Also, in some embodiments, some of the one or more interconnect segments that extend in the first direction are positioned over either the first diffusion fin or the second diffusion fin. In some embodiments, the one or more interconnect segments that extend in the first direction are positioned in accordance with a second direction interconnect pitch as measured in the second direction between respective first direction oriented centerlines of the one or more interconnect segments.

[00193] In some embodiments, the first and second diffusion fins can be positioned in accordance with a diffusion fin pitch as measured in the second direction between respective first direction oriented centerlines of the first and second diffusion fins, where the second direction interconnect pitch is a rational multiple of the diffusion fin pitch, with the rational multiple defined as a ratio of integer values.

[00194] In some embodiments, each of the first and second diffusion fins is centerline positioned in accordance with either a first diffusion fin pitch as measured in the second direction or a second diffusion fin pitch as measured in the second direction, where the first and second diffusion pitches successively alternate in the second direction, and where an average diffusion fin pitch is an average of the first and second diffusion fin pitches, and

[00195] where the second direction interconnect pitch is a rational multiple of the average diffusion fin pitch, with the rational multiple defined as a ratio of integer values. In some embodiments, the first diffusion fin pitch is equal to the second diffusion fin pitch. In some embodiments, the first diffusion fin pitch is different than the second diffusion fin pitch.

[00196] The above-mentioned one or more interconnect structures can include either a local interconnect structure, a higher-level interconnect structure, or a combination thereof, where the local interconnect structure is a lowest level interconnect structure that is not a diffusion fin, and where the higher-level interconnect structure is an interconnect structure formed at a level above the local interconnect structure relative to the substrate.

[00197] In some embodiments, each of the first and second diffusion fins is centerline positioned in accordance with either a first diffusion fin pitch as measured in the second direction or a second diffusion fin pitch as measured in the second direction, where the first and second diffusion pitches successively alternate in the second direction, and where an average diffusion fin pitch is an average of the first and second diffusion fin pitches. Also, the one or more interconnect segments that extend in the first direction can be centerline positioned in accordance with either a first interconnect pitch as measured in the second direction or a second interconnect pitch as measured in the second direction, where the first and second interconnect pitches successively alternate in the second direction, and where an average interconnect pitch is an average of the first and second interconnect pitches. Also, the average interconnect pitch is a rational multiple of the average diffusion fin pitch, with the rational multiple defined as a ratio of integer values.

[00198] In some embodiments, the first diffusion fin pitch is equal to the second diffusion fin pitch, and the first interconnect pitch is equal to the second interconnect pitch. In some embodiments, the first diffusion fin pitch is different than the second diffusion fin pitch, and the first interconnect pitch is different than the second interconnect pitch. In some embodiments, the first diffusion fin pitch is equal to the first interconnect pitch, and the second diffusion fin pitch is equal to the second interconnect pitch.

[00199] The semiconductor device can also include one or more interconnect structures, where some of the one or more interconnect structures include one or more interconnect

segments that extend in the second direction. In some embodiments, some of the one or more interconnect segments that extend in the second direction are positioned between the first and second gate electrode structures. In some embodiments, some of the one or more interconnect segments that extend in the second direction are positioned over either the first gate electrode structure or the second gate electrode structure.

[00200] In some embodiments, the one or more interconnect segments that extend in the second direction are positioned in accordance with a first direction interconnect pitch as measured in the first direction between respective second direction oriented centerlines of the one or more interconnect segments. Also, the first and second gate electrode structures can be positioned in accordance with a gate electrode pitch as measured in the first direction between respective second direction oriented centerlines of the first and second gate electrode structures. The first direction interconnect pitch can be a rational multiple of the gate electrode pitch, with the rational multiple defined as a ratio of integer values.

[00201] The above-mentioned one or more interconnect structures can include either a local interconnect structure, a higher-level interconnect structure, or a combination thereof, where the local interconnect structure is a lowest level interconnect structure that is not a diffusion fin, and where the higher-level interconnect structure is an interconnect structure formed at a level above the local interconnect structure relative to the substrate.

[00202] In some embodiments, the semiconductor device can also include a first plurality of transistors each having a respective source region and a respective drain region formed by a respective diffusion fin. Each diffusion fin of the first plurality of transistors is structured to project from the surface of the substrate. Each diffusion fin of the first plurality of transistors is structured to extend lengthwise in the first direction from a first end to a second end of the respective diffusion fin. The first ends of the diffusion fins of the first plurality of transistors are substantially aligned with each other in the first direction.

[00203] Also, the semiconductor device can include a second plurality of transistors each having a respective source region and a respective drain region formed by a respective diffusion fin. Each diffusion fin of the second plurality of transistors is structured to project from the surface of the substrate. Each diffusion fin of the second plurality of transistors is structured to extend lengthwise in the first direction from a first end to a second end of the respective diffusion fin. The first ends of the diffusion fins of the second plurality of transistors are substantially aligned with each other in the first direction. And, one or more of the first ends of the diffusion fins of the second plurality of transistors are positioned in the first

direction between the first and second ends of one or more of the diffusion fins of the first plurality of transistors.

[00204] In some embodiments, each of the first ends of the diffusion fins of the second plurality of transistors is positioned in the first direction between the first and second ends of one or more of the diffusion fins of the first plurality of transistors. In some embodiments, at least one of the diffusion fins of the second plurality of transistors is positioned next to and spaced apart from at least one diffusion fin of the first plurality of transistors. Also, in some embodiments, the first plurality of transistors can include either n-type transistors, p-type transistors, or a combination of n-type and p-type transistors, and the second plurality of transistors can include either n-type transistors, p-type transistors, or a combination of n-type and p-type transistors. In some embodiments, the first plurality of transistors are n-type transistors and the second plurality of transistors are p-type transistors.

[00205] In some embodiments, the first and second pluralities of diffusion fins are positioned to have their respective first direction oriented centerlines substantially aligned to a diffusion fin alignment grating defined by a first diffusion fin pitch as measured in the second direction and a second diffusion fin pitch as measured in the second direction. The first and second diffusion fin pitches occur in an alternating sequence in the second direction. Also, in some embodiments, the diffusion fins of the first and second pluralities of transistors collectively occupy portions at least eight consecutive alignment positions of the diffusion fin alignment grating.

[00206] In an example embodiment, a method of fabricating a semiconductor device is disclosed. The method includes providing a substrate. The method also includes forming a first transistor on the substrate, such that the first transistor has a source region and a drain region within a first diffusion fin, and such that the first diffusion fin is formed to project from a surface of the substrate, and such that the first diffusion fin is formed to extend lengthwise in a first direction from a first end of the first diffusion fin to a second end of the first diffusion fin. The method also includes forming a second transistor on the substrate, such that the second transistor has a source region and a drain region within a second diffusion fin, and such that the second diffusion fin is formed to project from the surface of the substrate, and such that the second diffusion fin is formed to extend lengthwise in the first direction from a first end of the second diffusion fin to a second end of the second diffusion fin, and such that the second diffusion fin is formed at a position next to and spaced apart from the first diffusion fin. Also, the first and second transistors are formed such that either the first end or the second end of the

second diffusion fin is formed at a position in the first direction between the first end and the second end of the first diffusion fin.

[00207] It should be understood that any circuit layout incorporating finfet transistors as disclosed herein can be stored in a tangible form, such as in a digital format on a computer readable medium. For example, a given circuit layout can be stored in a layout data file, and can be selectable from one or more libraries of cells. The layout data file can be formatted as a GDS II (Graphic Data System) database file, an OASIS (Open Artwork System Interchange Standard) database file, or any other type of data file format suitable for storing and communicating semiconductor device layouts. Also, multi-level layouts of a cell incorporating finfet transistors as disclosed herein can be included within a multi-level layout of a larger semiconductor device. The multi-level layout of the larger semiconductor device can also be stored in the form of a layout data file, such as those identified above.

[00208] Also, the invention described herein can be embodied as computer readable code on a computer readable medium. For example, the computer readable code can include a layout data file within which a layout of a cell incorporating finfet transistors as disclosed herein is stored. The computer readable code can also include program instructions for selecting one or more layout libraries and/or cells that include finfet transistors as disclosed herein. The layout libraries and/or cells can also be stored in a digital format on a computer readable medium.

[00209] The computer readable medium mentioned herein is any data storage device that can store data which can thereafter be read by a computer system. Examples of the computer readable medium include hard drives, network attached storage (NAS), read-only memory, random-access memory, CD-ROMs, CD-Rs, CD-RWs, magnetic tapes, and other optical and non-optical data storage devices. Multiple computer readable media distributed within a network of coupled computer systems can also be used to store respective portions of the computer readable code such that the computer readable code is stored and executed in a distributed fashion within the network.

[00210] In an example embodiment, a data storage device has computer executable program instructions stored thereon for rendering a layout of a semiconductor device. The data storage device includes computer program instructions for defining a first transistor to be formed on a substrate, such that the first transistor is defined to have a source region and a drain region within a first diffusion fin, and such that the first diffusion fin is defined to project from a surface of the substrate, and such that the first diffusion fin is defined to extend lengthwise in a first direction from a first end of the first diffusion fin to a second end of the

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first diffusion fin. The data storage device also includes computer program instructions for defining a second transistor to be formed on the substrate, such that the second transistor is defined to have a source region and a drain region within a second diffusion fin, and such that the second diffusion fin is defined to project from the surface of the substrate, and such that the second diffusion fin is defined to extend lengthwise in the first direction from a first end of the second diffusion fin to a second end of the second diffusion fin, and such that the second diffusion fin is defined to be positioned next to and spaced apart from the first diffusion fin, and such that the second diffusion fin is defined to have either its first end or its second end positioned in the first direction between the first end and the second end of the first diffusion fin.

[00211] It should be further understood that any circuit layout incorporating finfet transistors as disclosed herein can be manufactured as part of a semiconductor device or chip. In the fabrication of semiconductor devices such as integrated circuits, memory cells, and the like, a series of manufacturing operations are performed to define features on a semiconductor wafer. The wafer includes integrated circuit devices in the form of multi-level structures defined on a silicon substrate. At a substrate level, transistor devices with diffusion regions and/or diffusion fins are formed. In subsequent levels, interconnect metallization lines are patterned and electrically connected to the transistor devices to define a desired integrated circuit device. Also, patterned conductive layers are insulated from other conductive layers by dielectric materials.

[00212] While this invention has been described in terms of several embodiments, it will be appreciated that those skilled in the art upon reading the preceding specifications and studying the drawings will realize various alterations, additions, permutations and equivalents thereof. Therefore, it is intended that the present invention includes all such alterations, additions, permutations, and equivalents as fall within the true spirit and scope of the invention.

What is claimed is:

What is claimed is:

1. A semiconductor device, comprising:

a substrate;

a first transistor having a source region and a drain region within a first diffusion fin, the first diffusion fin structured to project from a surface of the substrate, the first diffusion fin structured to extend lengthwise in a first direction from a first end of the first diffusion fin to a second end of the first diffusion fin;

a second transistor having a source region and a drain region within a second diffusion fin, the second diffusion fin structured to project from the surface of the substrate, the second diffusion fin structured to extend lengthwise in the first direction from a first end of the second diffusion fin to a second end of the second diffusion fin, the second diffusion fin positioned next to and spaced apart from the first diffusion fin,

wherein either the first end or the second end of the second diffusion fin is positioned in the first direction at a location between the first end and the second end of the first diffusion fin, the location offset in the first direction from the first end and the second end of the first diffusion fin.

2. A semiconductor device as recited in claim 1, wherein the first and second transistors are located at different positions in the second direction perpendicular to the first direction.

3. A semiconductor device as recited in claim 1, wherein each of the first and second transistors is a three-dimensionally gated transistor.

4. A semiconductor device as recited in claim 1, wherein the first transistor includes a first linear-shaped gate electrode structure that extends lengthwise in a second direction perpendicular to the first direction as viewed from above the substrate, and

wherein the second transistor includes a second linear-shaped gate electrode structure that extends lengthwise in the second direction perpendicular to the first direction as viewed from above the substrate,

wherein at least one of the first and second ends of the first diffusion fin is positioned in the first direction between the first and second linear-shaped gate electrode structures, and

wherein at least one of the first and second ends of the second diffusion fin is positioned

in the first direction between the first and second linear-shaped gate electrode structures.

5. A semiconductor device as recited in claim 4, wherein the first linear-shaped gate electrode structure is positioned next to and spaced apart from the second linear-shaped gate electrode structure.

6. A semiconductor device as recited in claim 4, further comprising:
a linear-shaped local interconnect structure that extends in the second direction and that is positioned between the first and second linear-shaped gate electrode structures.

7. A semiconductor device as recited in claim 6, wherein the linear-shaped local interconnect structure is substantially centered in the first direction between the first and second linear-shaped gate electrode structures.

8. A semiconductor device as recited in claim 6, wherein the linear-shaped local interconnect structure connects to one or more of the first and second diffusion fins.

9. A semiconductor device as recited in claim 4, further comprising:
a linear-shaped local interconnect structure that extends in the first direction and that is positioned between the first and second diffusion fins.

10. A semiconductor device as recited in claim 9, wherein the linear-shaped local interconnect structure is substantially centered in the second direction between the first and second diffusion fins.

11. A semiconductor device as recited in claim 9, wherein the linear-shaped local interconnect structure connects to one or more of the first and second gate electrode structures.

12. A semiconductor device as recited in claim 9, wherein the linear-shaped local interconnect structure is a first linear-shaped local interconnect structure, the semiconductor device further including a second linear-shaped local interconnect structure that extends in the second direction and that is positioned between the first and second linear-shaped gate electrode structures.

13. A semiconductor device as recited in claim 12, wherein the second linear-shaped local interconnect structure is substantially centered in the first direction between the first and second linear-shaped gate electrode structures.

14. A semiconductor device as recited in claim 12, wherein the second linear-shaped local interconnect structure connects to one or more of the first diffusion fin, the second diffusion fin.

15. A semiconductor device as recited in claim 12, wherein the first linear-shaped local interconnect structure is a first linear segment of a two-dimensionally varying non-linear local interconnect structure, and wherein the second linear-shaped local interconnect structure is a second linear segment of the two-dimensionally varying non-linear local interconnect structure.

16. A semiconductor device as recited in claim 15, wherein the first and second linear-shaped local interconnect structures are connected to each other.

17. A semiconductor device as recited in claim 4, further comprising:
a contact structure positioned between the first and second diffusion fins.

18. A semiconductor device as recited in claim 17, wherein the contact structure is substantially centered between the first and second diffusion fins.

19. A semiconductor device as recited in claim 18, wherein the contact structure connects to either the first gate electrode structure or the second gate electrode structure.

20. A semiconductor device as recited in claim 4, further comprising:
a contact structure positioned between the first and second gate electrode structures.

21. A semiconductor device as recited in claim 20, wherein the contact structure is substantially centered between the first and second gate electrode structures.

22. A semiconductor device as recited in claim 20, further comprising:
a conductive interconnect structure positioned in the second direction between first and second diffusion fins, wherein the contact structure connects to the conductive interconnect structure.

23. A semiconductor device as recited in claim 22, wherein the conductive interconnect structure is a lowest level interconnect structure extending in the first direction that is not a diffusion fin.

24. A semiconductor device as recited in claim 22, wherein the conductive interconnect structure is higher-level interconnect structure.

25. A semiconductor device as recited in claim 20, further comprising:
a conductive interconnect structure positioned in the first direction between first and second diffusion fins, wherein the contact structure connects to a conductive interconnect structure.

26. A semiconductor device as recited in claim 4, further comprising:
one or more interconnect structures, wherein some of the one or more interconnect

structures include one or more interconnect segments that extend in the first direction.

27. A semiconductor device as recited in claim 26, wherein some of the one or more interconnect segments that extend in the first direction are positioned between the first and second diffusion fins.

28. A semiconductor device as recited in claim 26, wherein some of the one or more interconnect segments that extend in the first direction are positioned over either the first diffusion fin or the second diffusion fin.

29. A semiconductor device as recited in claim 26, wherein the one or more interconnect segments that extend in the first direction are positioned in accordance with a second direction interconnect pitch as measured in the second direction between respective first direction oriented centerlines of the one or more interconnect segments.

30. A semiconductor device as recited in claim 29, wherein the first and second diffusion fins are positioned in accordance with a diffusion fin pitch as measured in the second direction between respective first direction oriented centerlines of the first and second diffusion fins, and

wherein the second direction interconnect pitch is a rational multiple of the diffusion fin pitch, the rational multiple defined as a ratio of integer values.

31. A semiconductor device as recited in claim 29, wherein each of the first and second diffusion fins is centerline positioned in accordance with either a first diffusion fin pitch as measured in the second direction or a second diffusion fin pitch as measured in the second direction, wherein the first and second diffusion pitches successively alternate in the second direction, and wherein an average diffusion fin pitch is an average of the first and second diffusion fin pitches, and

wherein the second direction interconnect pitch is a rational multiple of the average diffusion fin pitch, the rational multiple defined as a ratio of integer values.

32. A semiconductor device as recited in claim 31, wherein the first diffusion fin pitch is equal to the second diffusion fin pitch.

33. A semiconductor device as recited in claim 31, wherein the first diffusion fin pitch is different than the second diffusion fin pitch.

34. A semiconductor device as recited in claim 26, wherein the one or more interconnect structures include either a local interconnect structure, a higher-level interconnect

structure formed at a level above a local interconnect structure relative to the substrate, or both a local interconnect structure and a higher-level interconnect structure formed at a level above the local interconnect structure relative to the substrate, wherein the local interconnect structure is a lowest level interconnect structure that is not a diffusion fin.

35. A semiconductor device as recited in claim 26, wherein each of the first and second diffusion fins is centerline positioned in accordance with either a first diffusion fin pitch as measured in the second direction or a second diffusion fin pitch as measured in the second direction, wherein the first and second diffusion pitches successively alternate in the second direction, and wherein an average diffusion fin pitch is an average of the first and second diffusion fin pitches, and

wherein the one or more interconnect segments that extend in the first direction are centerline positioned in accordance with either a first interconnect pitch as measured in the second direction or a second interconnect pitch as measured in the second direction, wherein the first and second interconnect pitches successively alternate in the second direction, and wherein an average interconnect pitch is an average of the first and second interconnect pitches,

wherein the average interconnect pitch is a rational multiple of the average diffusion fin pitch, the rational multiple defined as a ratio of integer values.

36. A semiconductor device as recited in claim 35, wherein the first diffusion fin pitch is equal to the second diffusion fin pitch, and the first interconnect pitch is equal to the second interconnect pitch.

37. A semiconductor device as recited in claim 35, wherein the first diffusion fin pitch is different than the second diffusion fin pitch, and the first interconnect pitch is different than the second interconnect pitch.

38. A semiconductor device as recited in claim 35, wherein the first diffusion fin pitch is equal to the first interconnect pitch, and the second diffusion fin pitch is equal to the second interconnect pitch.

39. A semiconductor device as recited in claim 4, further comprising:
one or more interconnect structures, wherein some of the one or more interconnect structures include one or more interconnect segments that extend in the second direction.

40. A semiconductor device as recited in claim 39, wherein some of the one or more interconnect segments that extend in the second direction are positioned between the first and

second gate electrode structures.

41. A semiconductor device as recited in claim 39, wherein some of the one or more interconnect segments that extend in the second direction are positioned over either the first gate electrode structure or the second gate electrode structure.

42. A semiconductor device as recited in claim 39, wherein the one or more interconnect segments that extend in the second direction are positioned in accordance with a first direction interconnect pitch as measured in the first direction between respective second direction oriented centerlines of the one or more interconnect segments.

43. A semiconductor device as recited in claim 42, wherein the first and second gate electrode structures are positioned in accordance with a gate electrode pitch as measured in the first direction between respective second direction oriented centerlines of the first and second gate electrode structures, and

wherein the first direction interconnect pitch is a rational multiple of the gate electrode pitch, the rational multiple defined as a ratio of integer values.

44. A semiconductor device as recited in claim 39, wherein the one or more interconnect structures include either a local interconnect structure, a higher-level interconnect structure, or a combination thereof, wherein the local interconnect structure is a lowest level interconnect structure that is not a diffusion fin, and wherein the higher-level interconnect structure is an interconnect structure formed at a level above the local interconnect structure relative to the substrate.

45. A semiconductor device as recited in claim 1, further comprising:

a first plurality of transistors each having a respective source region and a respective drain region formed by a respective diffusion fin, each diffusion fin of the first plurality of transistors structured to project from the surface of the substrate, each diffusion fin of the first plurality of transistors structured to extend lengthwise in the first direction from a first end to a second end of the respective diffusion fin, wherein the first ends of the diffusion fins of the first plurality of transistors are substantially aligned with each other in the first direction,

a second plurality of transistors each having a respective source region and a respective drain region formed by a respective diffusion fin, each diffusion fin of the second plurality of transistors structured to project from the surface of the substrate, each diffusion fin of the second plurality of transistors structured to extend lengthwise in the first direction from a first end to a

second end of the respective diffusion fin, wherein the first ends of the diffusion fins of the second plurality of transistors are substantially aligned with each other in the first direction, and

wherein one or more of the first ends of the diffusion fins of the second plurality of transistors are positioned in the first direction between the first and second ends of one or more of the diffusion fins of the first plurality of transistors.

46. A semiconductor device as recited in claim 45, wherein each of the first ends of the diffusion fins of the second plurality of transistors is positioned in the first direction between the first and second ends of one or more of the diffusion fins of the first plurality of transistors.

47. A semiconductor device as recited in claim 46, wherein at least one of the diffusion fins of the second plurality of transistors is positioned next to and spaced apart from at least one diffusion fin of the first plurality of transistors.

48. A semiconductor device as recited in claim 45, wherein the first plurality of transistors includes either n-type transistors, p-type transistors, or a combination of n-type and p-type transistors, and

wherein the second plurality of transistors includes either n-type transistors, p-type transistors, or a combination of n-type and p-type transistors.

49. A semiconductor device as recited in claim 45, wherein the first plurality of transistors are n-type transistors and the second plurality of transistors are p-type transistors.

50. A semiconductor device as recited in claim 45, wherein the first and second pluralities of diffusion fins are positioned to have their respective first direction oriented centerlines substantially aligned to a diffusion fin alignment grating defined by a first diffusion fin pitch as measured in the second direction perpendicular to the first direction and a second diffusion fin pitch as measured in the second direction, where the first and second diffusion fin pitches occur in an alternating sequence in the second direction.

51. A semiconductor device as recited in claim 50, wherein the diffusion fins of the first and second pluralities of transistors collectively occupy portions at least eight consecutive alignment positions of the diffusion fin alignment grating.

52. A method of fabricating a semiconductor device, comprising:

providing a substrate;

forming a first transistor on the substrate, the first transistor having a source region and a drain region within a first diffusion fin, the first diffusion fin formed to project from a surface of

the substrate, the first diffusion fin formed to extend lengthwise in a first direction from a first end of the first diffusion fin to a second end of the first diffusion fin;

forming a second transistor on the substrate, the second transistor having a source region and a drain region within a second diffusion fin, the second diffusion fin formed to project from the surface of the substrate, the second diffusion fin formed to extend lengthwise in the first direction from a first end of the second diffusion fin to a second end of the second diffusion fin, the second diffusion fin formed at a position next to and spaced apart from the first diffusion fin,

wherein either the first end or the second end of the second diffusion fin is formed at a location in the first direction between the first end and the second end of the first diffusion fin, the location offset in the first direction from the first end and the second end of the first diffusion fin.