CLAIMS

1. A multilayered structure comprising:

one or more nanocrystalline layers each comprising a transition metal dichalcogenide;

one or more substantially amorphous electrically insulating layers each comprising a transition metal oxide, wherein the transition metal oxide comprises a transition metal which is identical to the transition metal of the transition metal dichalcogenide;

wherein the one or more nanocrystalline layers and the one or more substantially amorphous electrically insulating layers are formed in an alternating manner, and

wherein each of the one or more nanocrystalline layers is formed adjacent to the substantially amorphous insulating layer, and wherein one substantially amorphous electrically insulating layer is positioned between two nanocrystalline layers.

~~2. The multilayered structure of claim 1, wherein one substantially amorphous electrically insulating layer is positioned between two nanocrystalline layers.~~

~~3~~2. The multilayered structure of claim 1 ~~or 2~~, wherein each of the one or more nanocrystalline layers has a grain size of less than 1 µm.

~~4~~3. The multilayered structure of ~~any one of~~ claim~~s~~ 1 ~~to~~or ~~3~~2, wherein the transition metal dichalcogenide comprises MoS_2, WS_2, $MoSe_2$, WSe_2, WTe_2, or $MoTe_2$.

~~5~~4. The multilayered structure of any one of claims 1 to ~~4~~3, wherein the substantially amorphous electrically insulating layer further comprises a polymer, wherein the polymer comprises poly methyl methacrylate, polystyrene, or polycarbonate.

~~6~~5. The multilayered structure of any one of claims 1 to ~~5~~4, wherein the transition metal of the transition metal oxide comprises Mo or W.

~~7~~6. The multilayered structure of any one of claims 1 to ~~6~~5, wherein each of the one or more nanocrystalline layers has a minimum thickness of 0.6 nm.

~~8~~7. A resistive memory device comprising the multilayered structure of any one of claims 1 to ~~7~~6.

~~9~~8. The resistive memory device of claim ~~8~~7, further comprising a first electrode and a second electrode, wherein (i) the first electrode is electrically conductive and comprises a reactive metal and (ii) the second electrode is electrically conductive and comprises a non-reactive metal.

~~10~~9. The resistive memory device of claim 7 or 8 ~~or 9~~,

wherein the reactive metal comprises silver, copper, or aluminum; and

wherein the non-reactive metal comprises gold, tungsten, or platinum.

~~11~~10. A process of fabricating the multilayered structure of any one of claims 1 to ~~7~~6, the process comprising:

providing a substrate comprising a nanocrystalline layer and a polymer layer deposited thereon, wherein the polymer layer is deposited on the nanocrystalline layer, wherein the nanocrystalline layer comprises a transition metal dichalcogenide;

separating the nanocrystalline layer with the polymer layer thereon from the substrate in an aqueous medium;

arranging the nanocrystalline layer with the polymer layer thereon on a target substrate which is heated prior to having the nanocrystalline layer and the polymer layer arranged thereon, wherein the target substrate is heated to a temperature which renders formation of a substantially amorphous electrically insulating layer on the nanocrystalline layer, wherein the substantially amorphous electrically insulating layer comprises a transition metal oxide, wherein the transition metal oxide comprises a transition metal which is identical to the transition metal of the transition metal dichalcogenide; and

removing the polymer layer from the nanocrystalline layer.

~~12~~11. The process of claim ~~11~~10, further comprises depositing a supporting layer on the polymer layer prior to separating the nanocrystalline layer with the polymer layer thereon from the substrate in the aqueous medium.

~~13~~12. The process of claim 10 or 11 ~~or 12~~, further comprises:

annealing the target substrate comprising the nanocrystalline layer but having the polymer layer already removed therefrom; and

heating the annealed target substrate prior to arranging another set of the nanocrystalline layer and the polymer layer on the target substrate.

~~14~~13. The process of any one of claims ~~11~~10 to ~~13~~12, wherein providing the substrate comprises:

depositing the transition metal dichalcogenide by physical vapor deposition on the substrate to form the nanocrystalline layer; and

spin coating a polymer solution on the nanocrystalline layer to form the polymer layer.

~~15~~14. The process of claim ~~14~~13, wherein the polymer solution comprises a polymer dissolved in an organic solvent, wherein the organic solvent comprises anisole.

~~16~~15. The process of any one of claims ~~12~~11 to ~~15~~14, wherein depositing the supporting layer comprises:

drying the polymer layer; and

arranging the supporting layer on the polymer layer.

~~17~~16. The process of any one of claims ~~12~~11 to ~~16~~15, further comprises detaching the supporting layer from the polymer layer after arranging the nanocrystalline layer with the polymer layer thereon on the target substrate.

~~18~~17. The process of any one of claims ~~12~~11 to ~~17~~16, wherein the supporting layer comprises polydimethylsiloxane or a thermal release tape.

~~19~~18. The process of any one of claims ~~11~~10 to ~~18~~17, wherein the temperature ranges from 120°C to 170°C.

~~20~~19. The process of any one of claims ~~11~~10 to ~~19~~18, wherein the aqueous medium is deionized water.