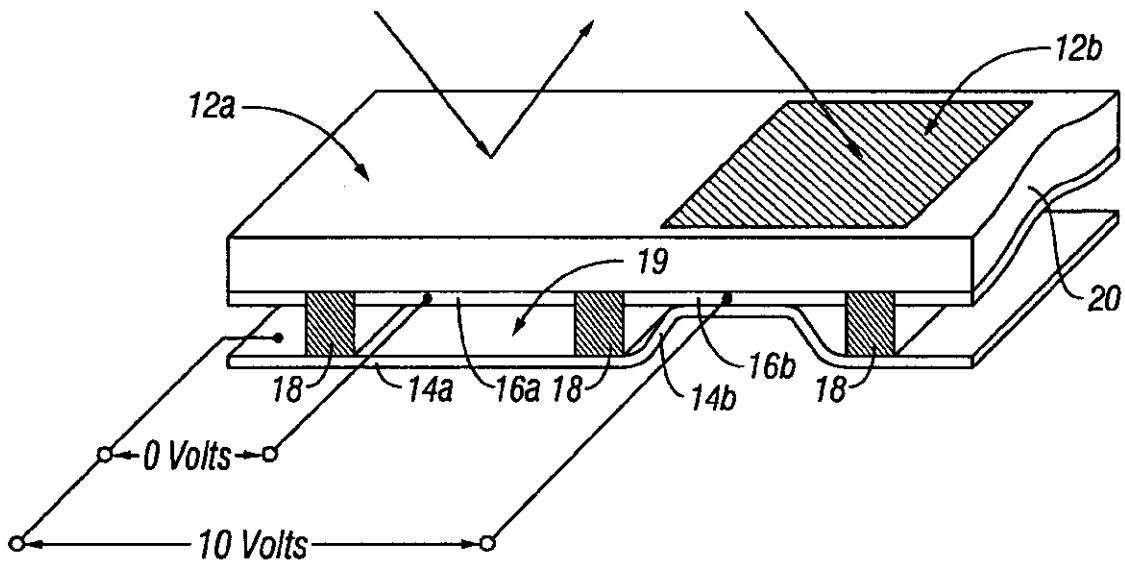


FIG. 1

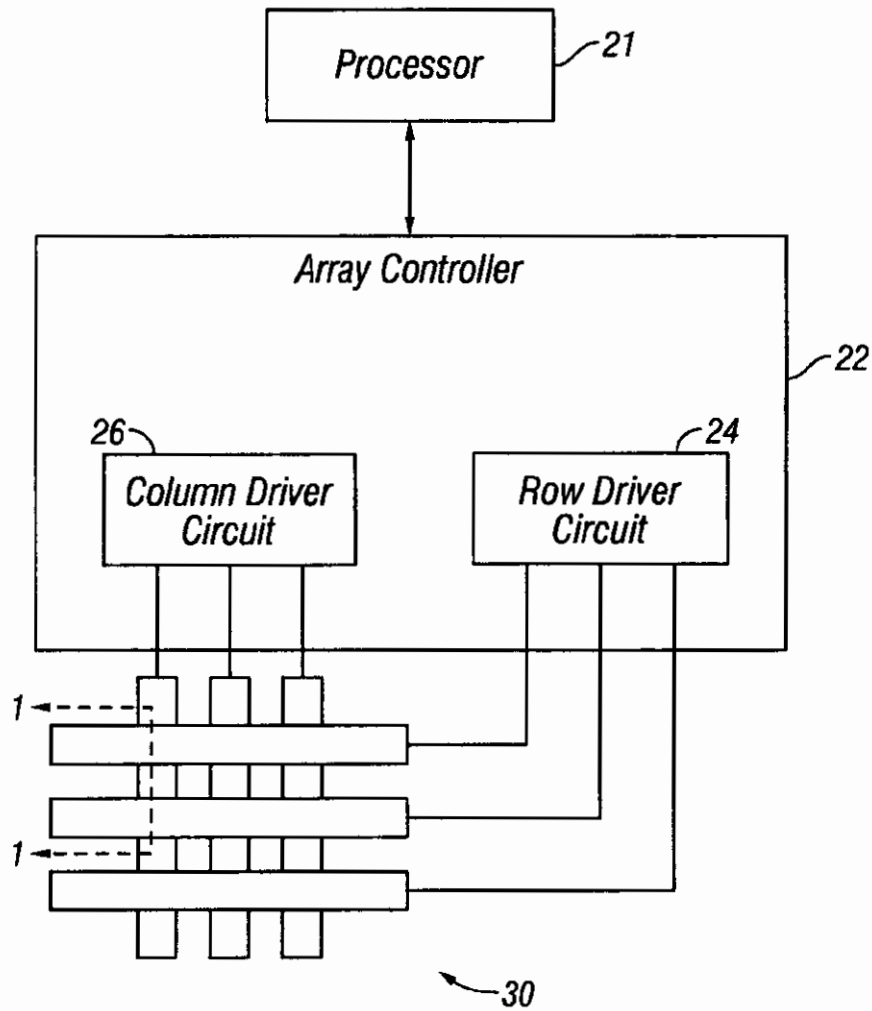

Processor
21
Array Controller
22
26
Column Driver Circuit
24
Row Driver Circuit
1
1
30

FIG. 2

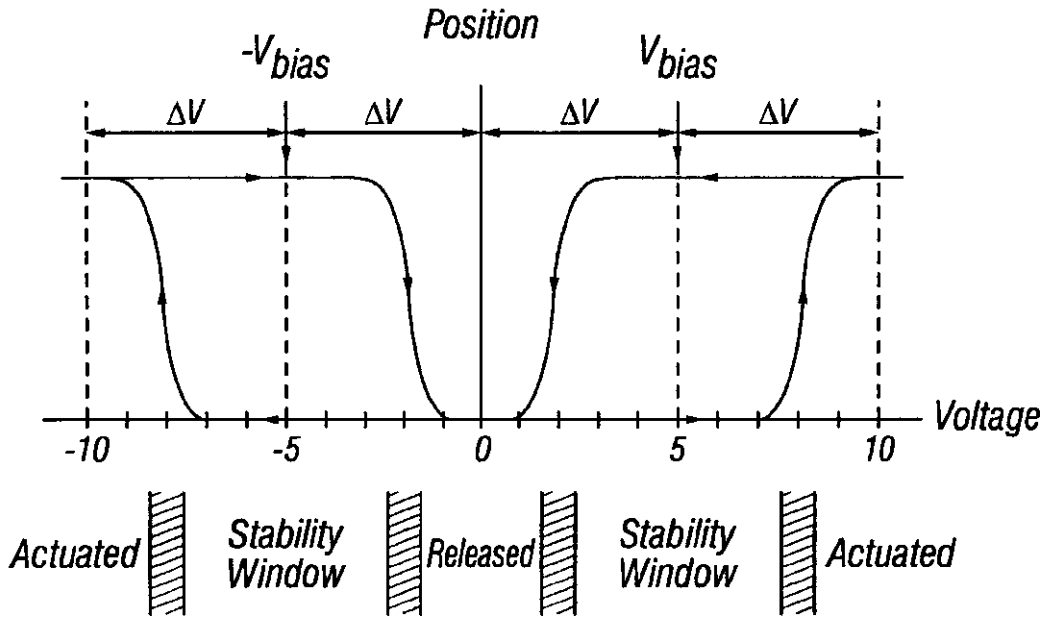


FIG. 3

Row Output Signals	Column Output Signals: $+V_{bias}$	Column Output Signals: $-V_{bias}$
0	Stable	Stable
$+\Delta V$	Release	Actuate
$-\Delta V$	Actuate	Release

FIG. 4

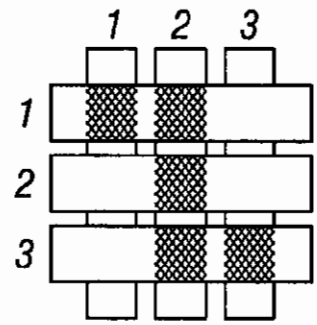

1
2
3
1
2
3

FIG. 5A

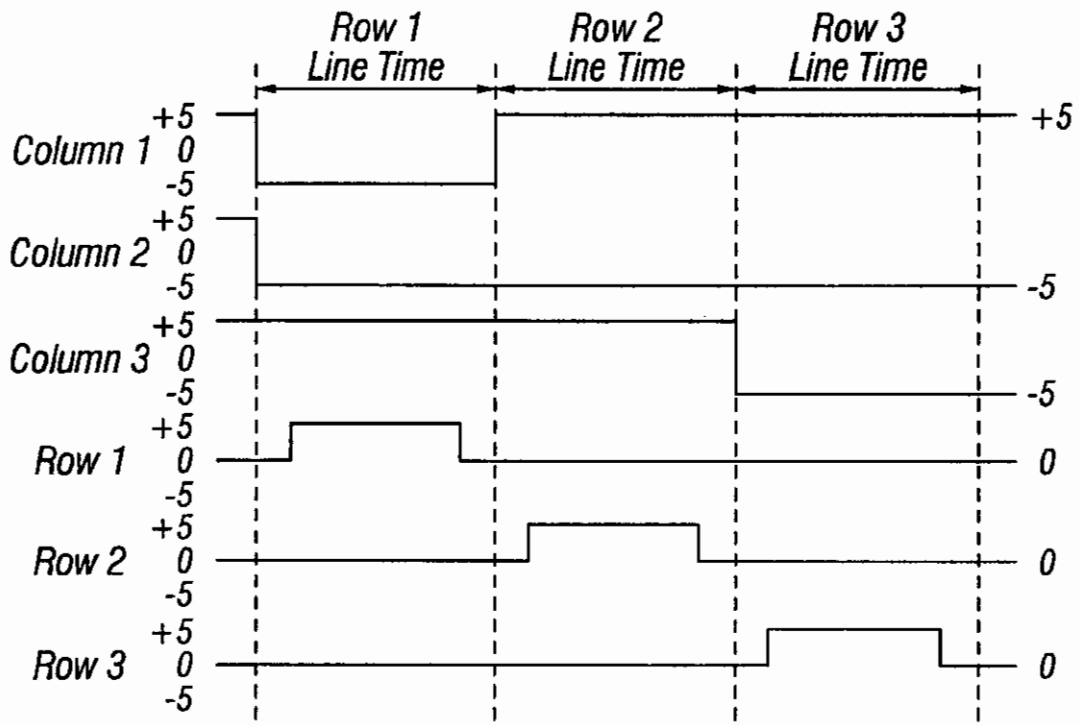

Row 1
Line Time
Row 2
Line Time
Row 3
Line Time
Column 1
Column 2
Column 3
Row 1
Row 2
Row 3
+5
0
-5
+5
-5
-5
0
0
0

FIG. 5B

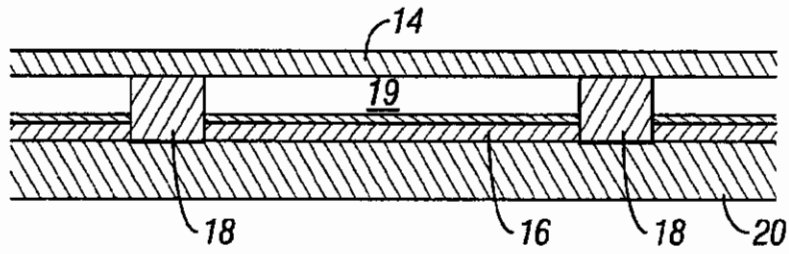


FIG. 6A

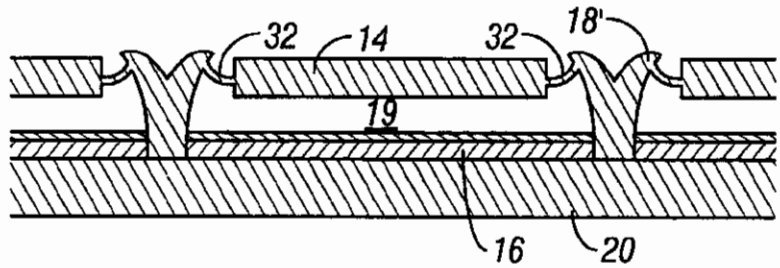


FIG. 6B

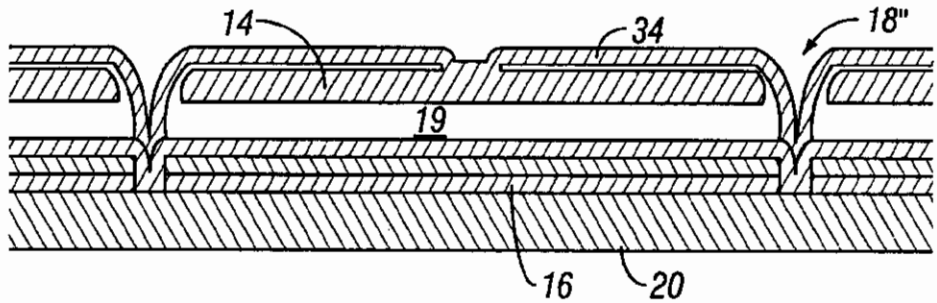


FIG. 6C

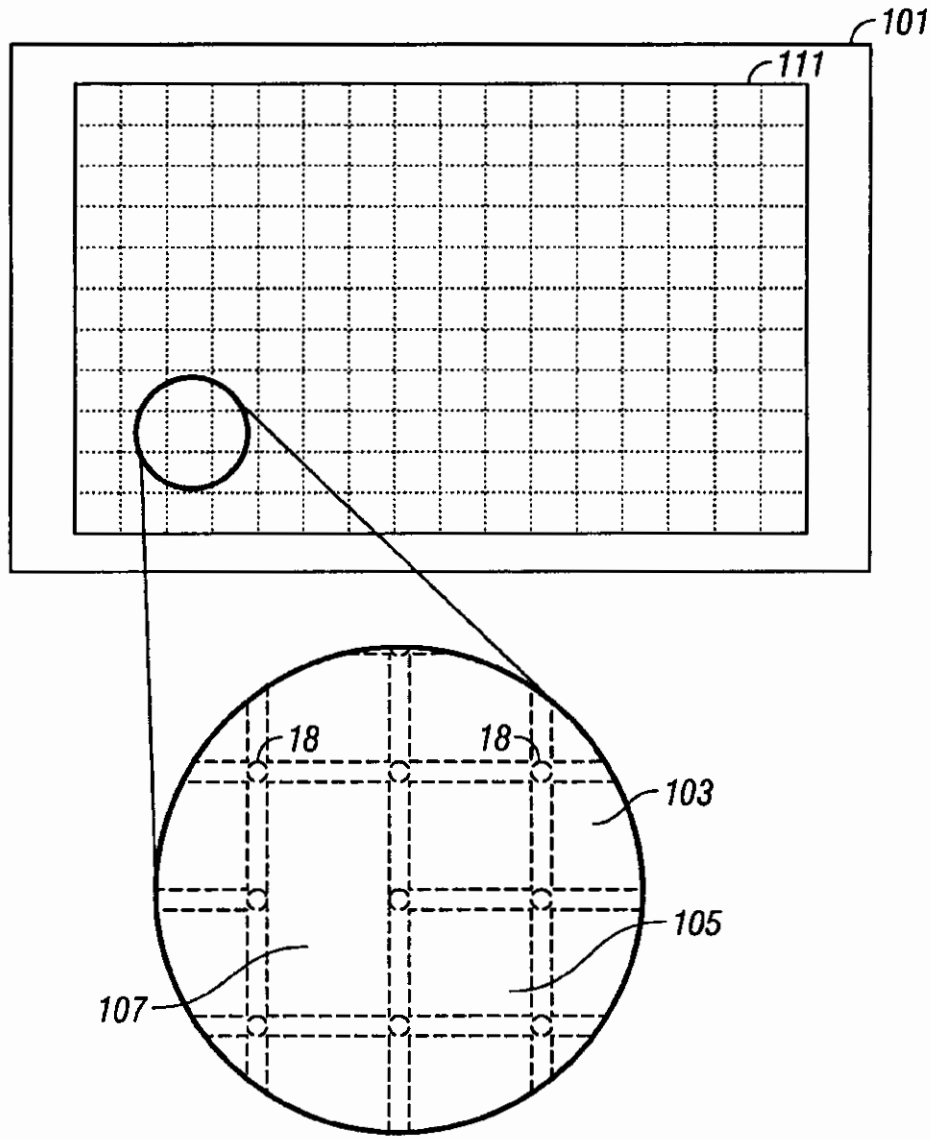


FIG. 7

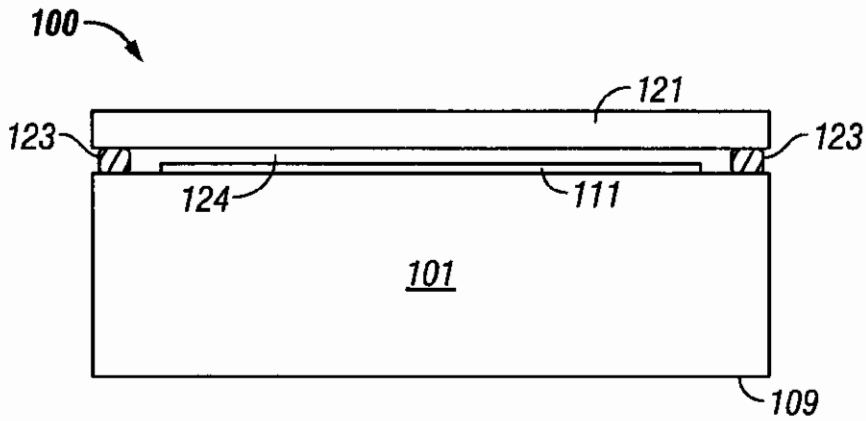

100
121
123
123
124
111
101
109

FIG. 8

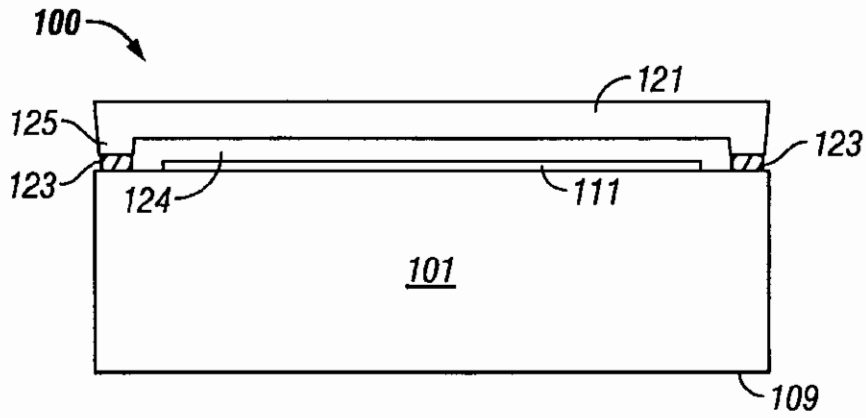

100
121
125
123
123
124
111
101
109

FIG. 9

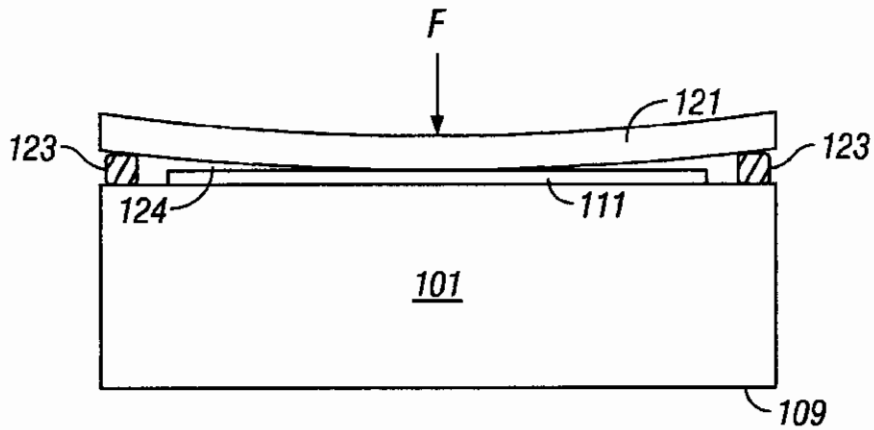


FIG. 10

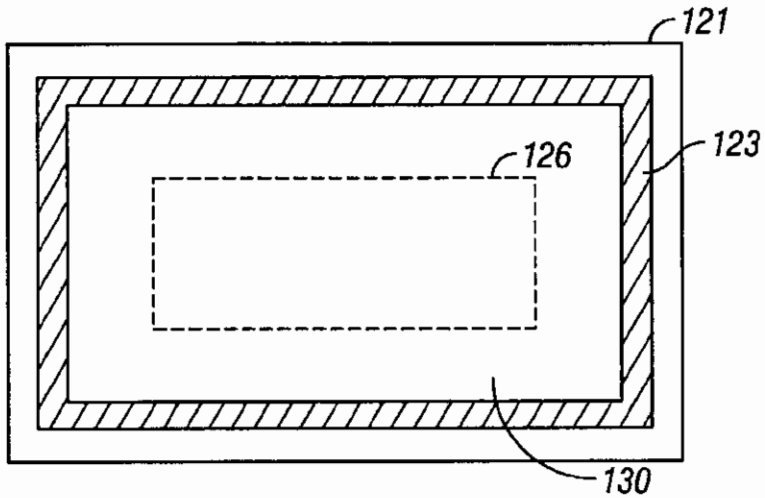


FIG. 11

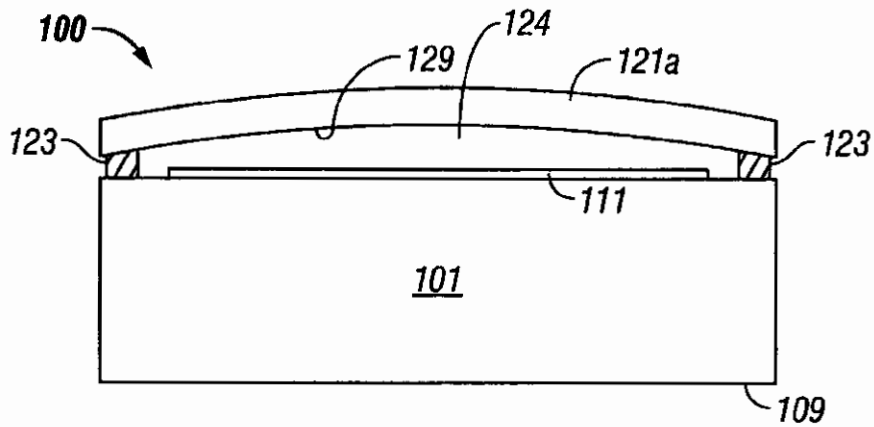


FIG. 12

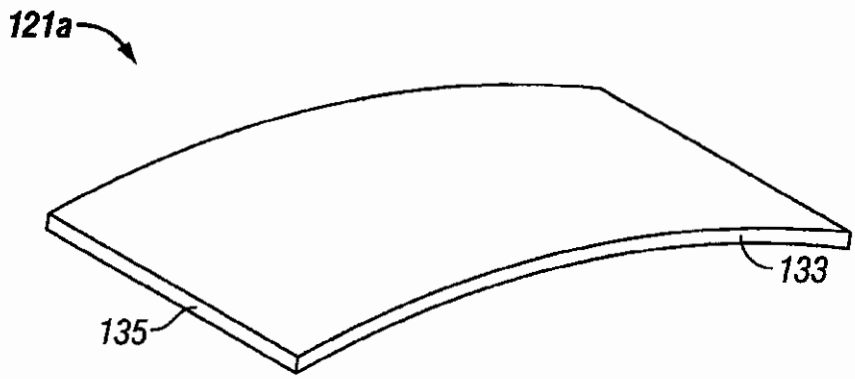


FIG. 13A

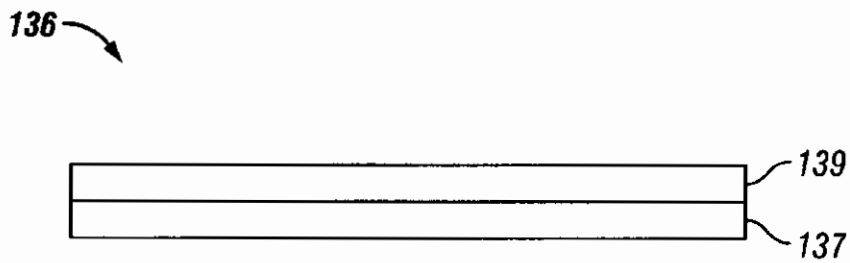


FIG. 13B

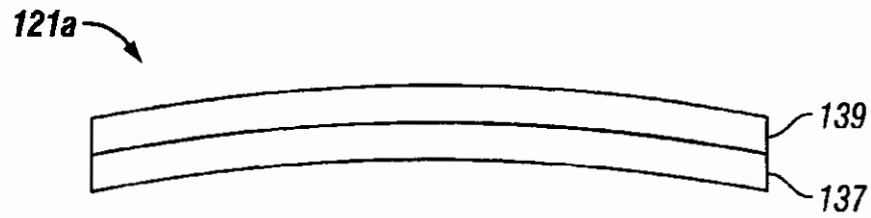


FIG. 13C

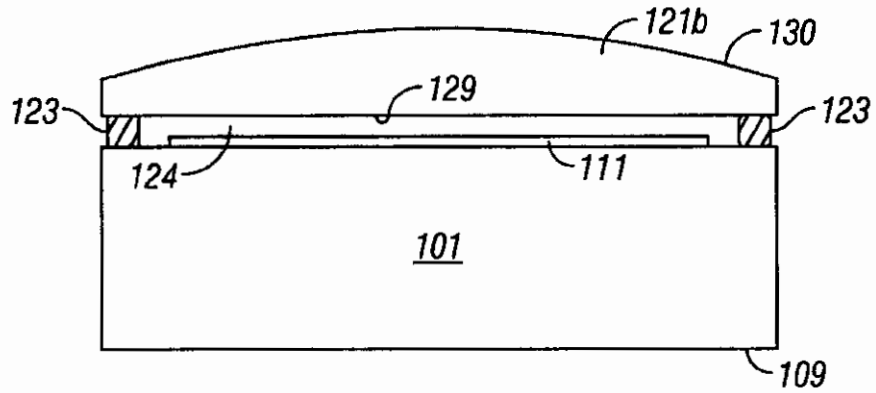


FIG. 14

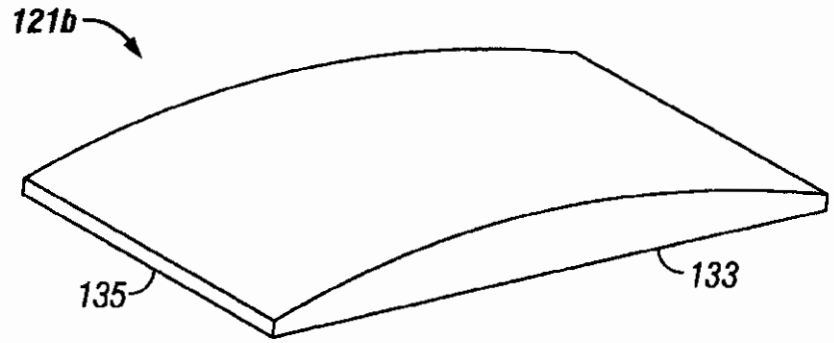


FIG. 15

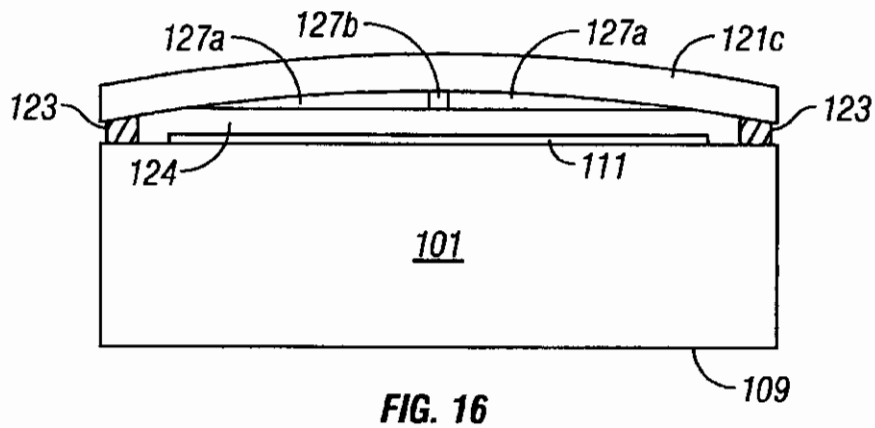


FIG. 16

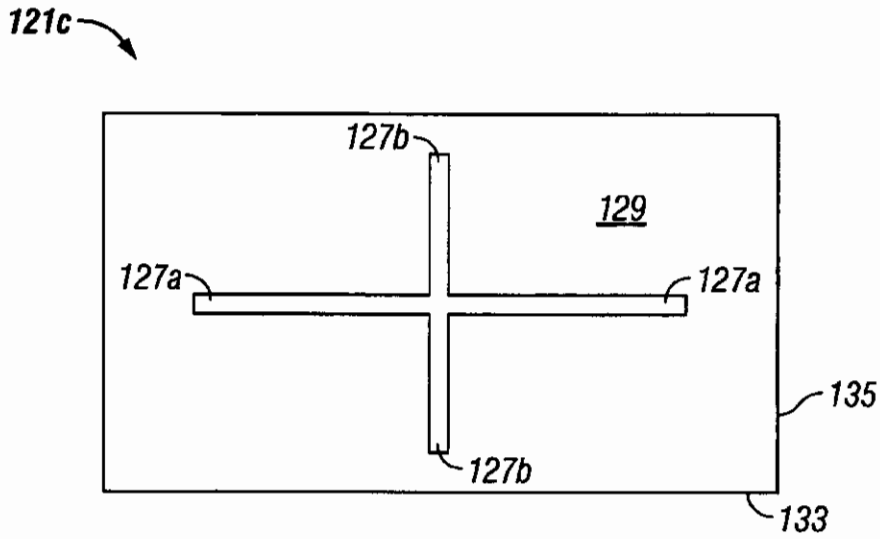


FIG. 17A

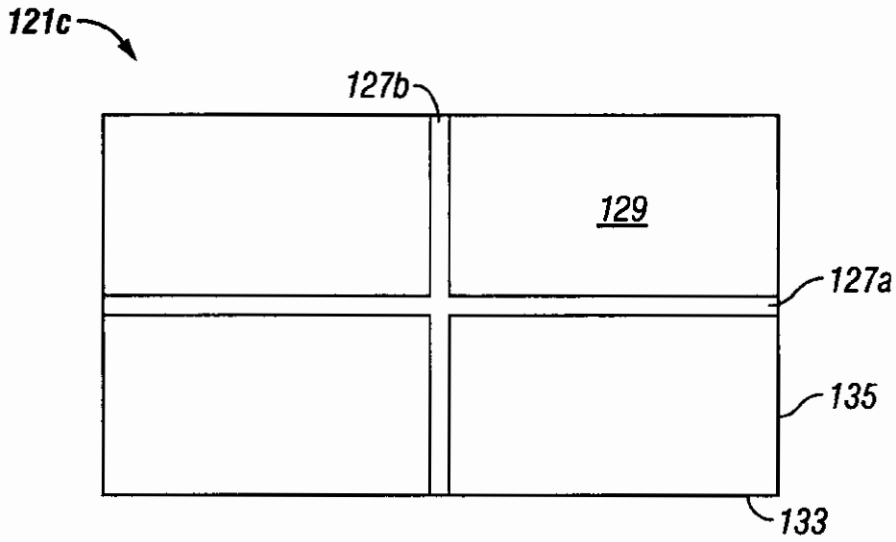


FIG. 17B

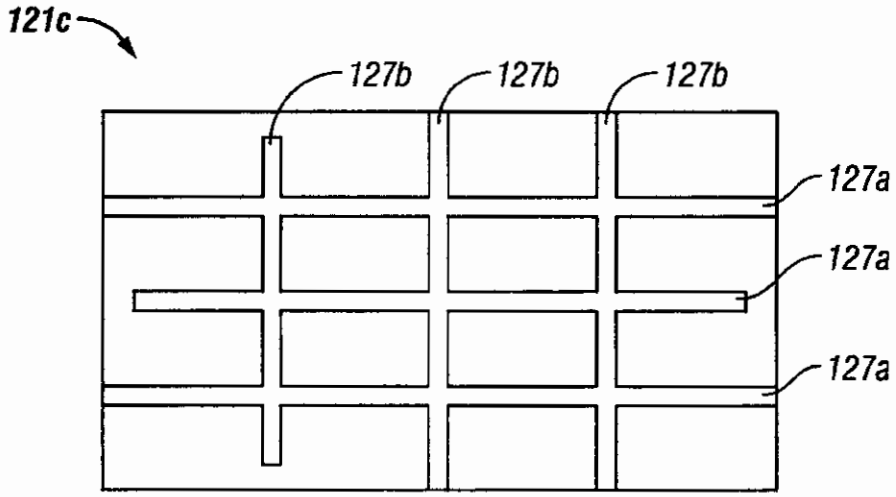


FIG. 17C

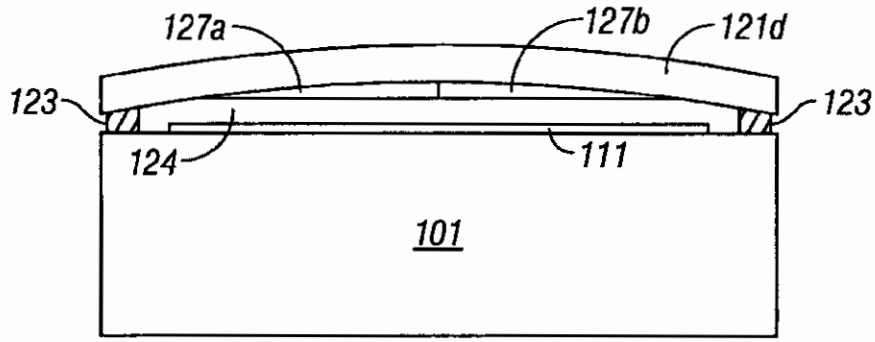

127a
127b
121d
123
123
124
111
101

FIG. 18

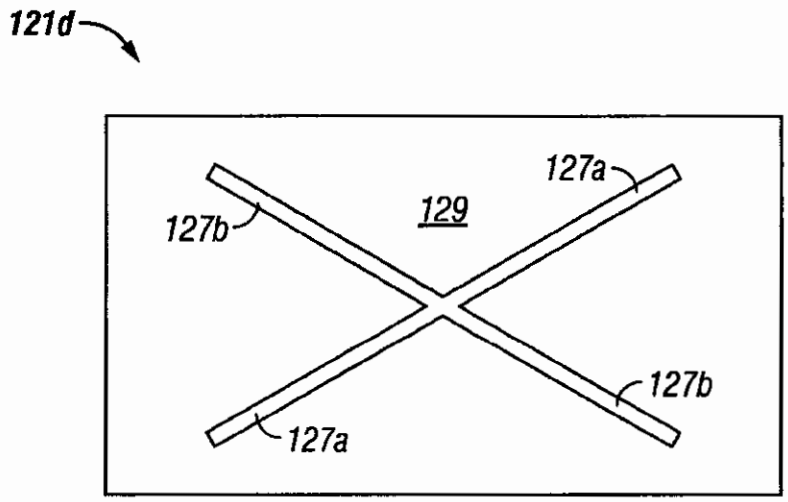

121d
127a
129
127b
127b
127a

FIG. 19

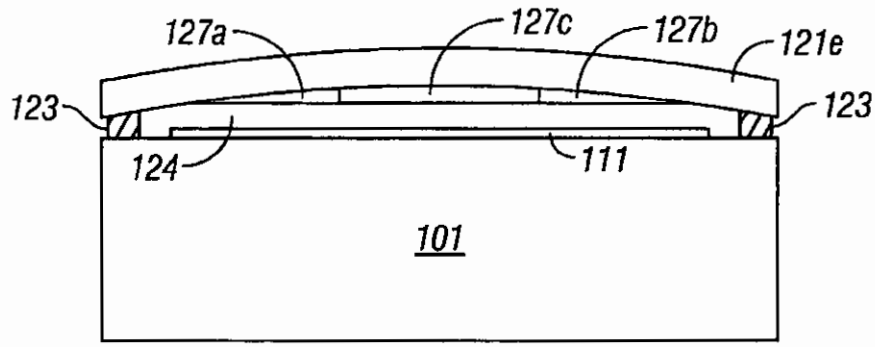

127a
127c
127b
121e
123
123
124
111
101

FIG. 20

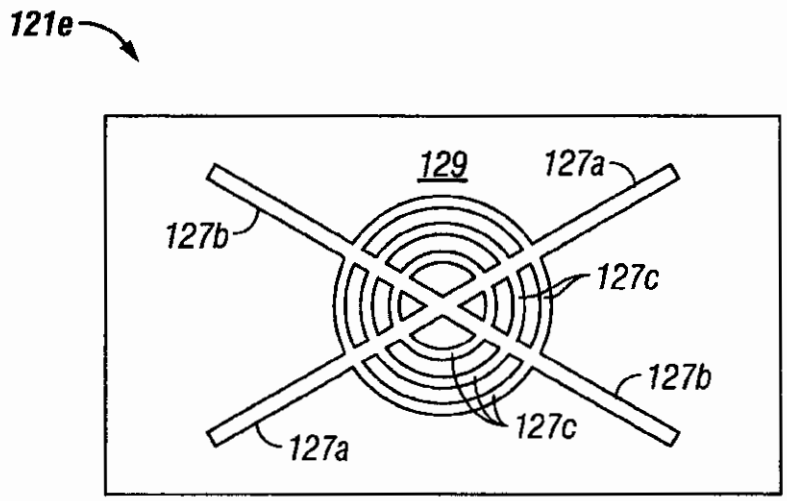

121e
129
127a
127b
127c
127b
127c
127a

FIG. 21

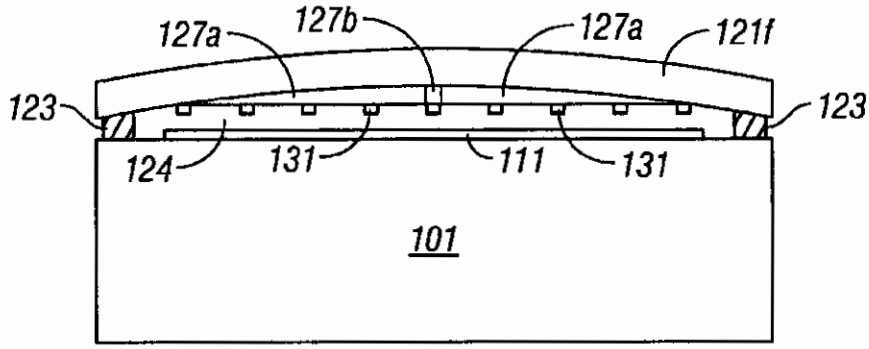

127a
127b
127a
121f
123
123
124
131
111
131
101

FIG. 22

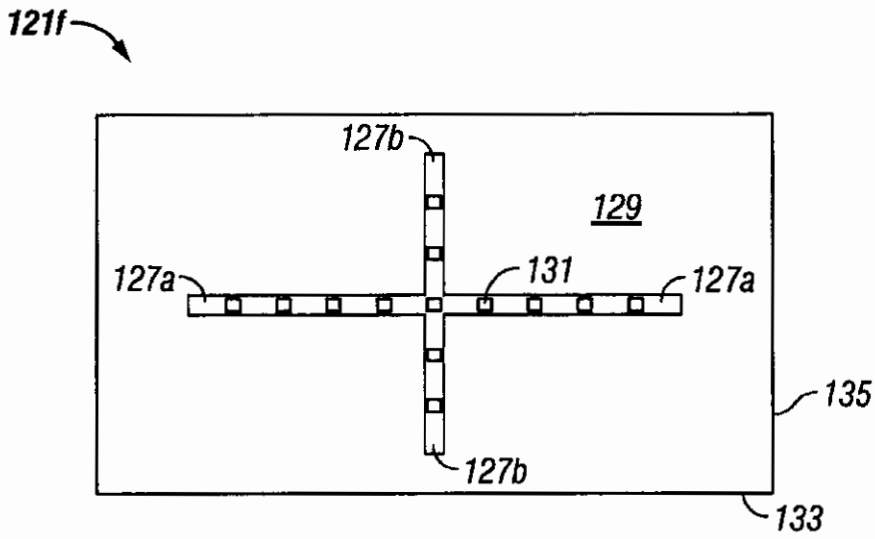

121f
127b
129
127a
131
127a
135
127b
133

FIG. 23

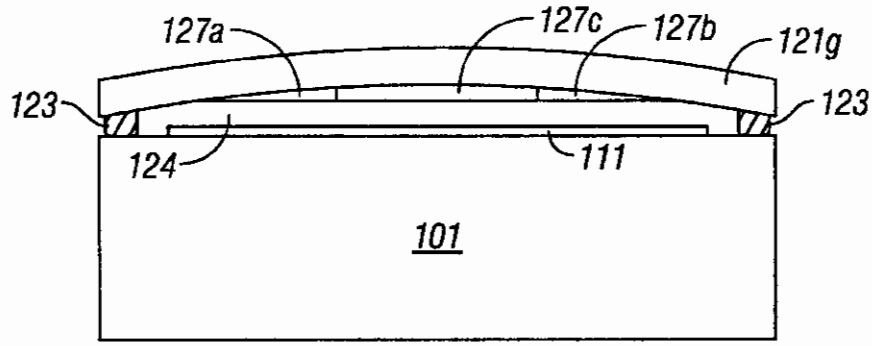

127a
127c
127b
121g
123
123
124
111
101

FIG. 24

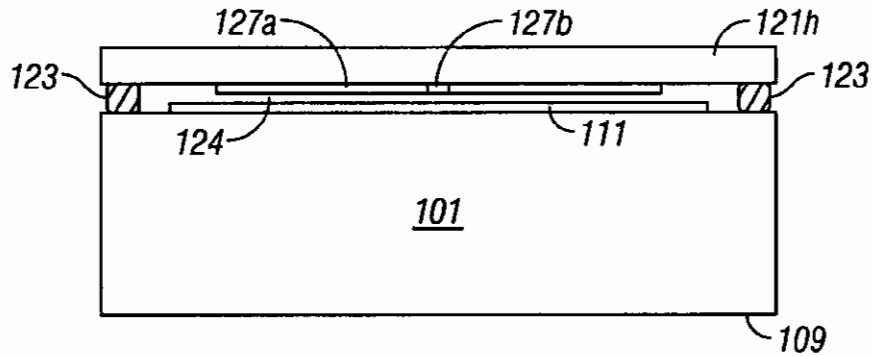

127a
127b
121h
123
123
124
111
101
109

FIG. 25

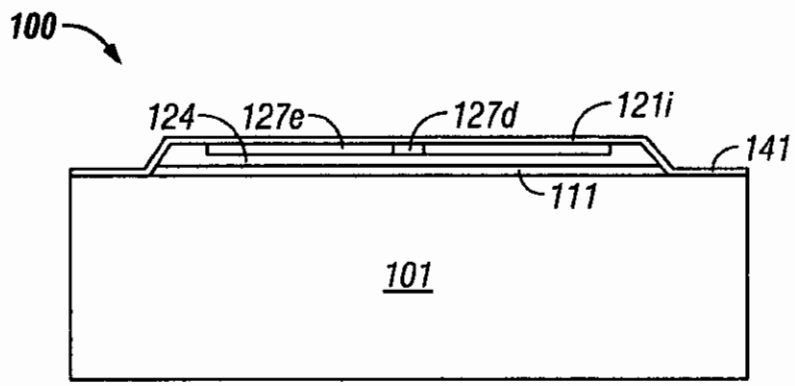

100
124
127e
127d
121i
141
111
101

FIG. 26

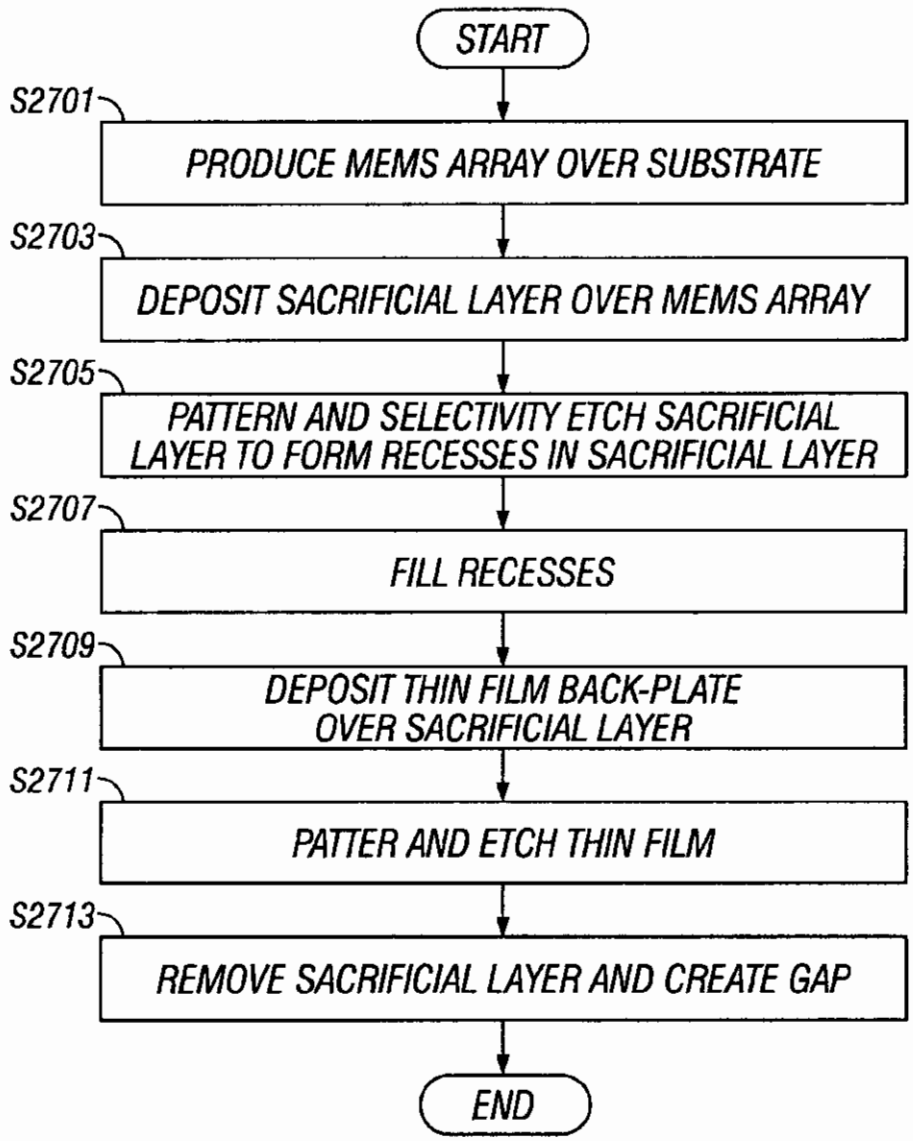

START
S2701
PRODUCE MEMS ARRAY OVER SUBSTRATE
S2703
DEPOSIT SACRIFICIAL LAYER OVER MEMS ARRAY
S2705
PATTERN AND SELECTIVITY ETCH SACRIFICIAL LAYER TO FORM RECESSES IN SACRIFICIAL LAYER
S2707
FILL RECESSES
S2709
DEPOSIT THIN FILM BACK-PLATE OVER SACRIFICIAL LAYER
S2711
PATTER AND ETCH THIN FILM
S2713
REMOVE SACRIFICIAL LAYER AND CREATE GAP
END

FIG. 27

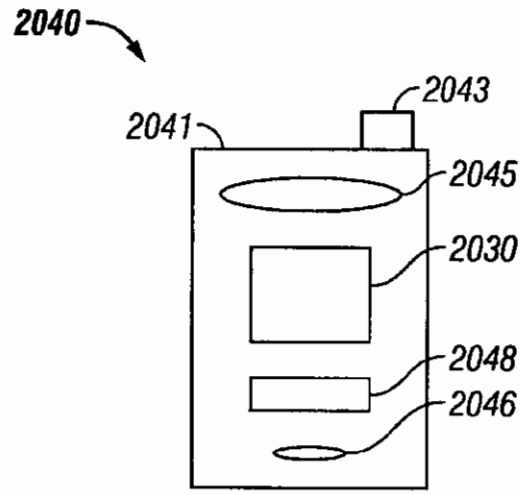


FIG. 28A

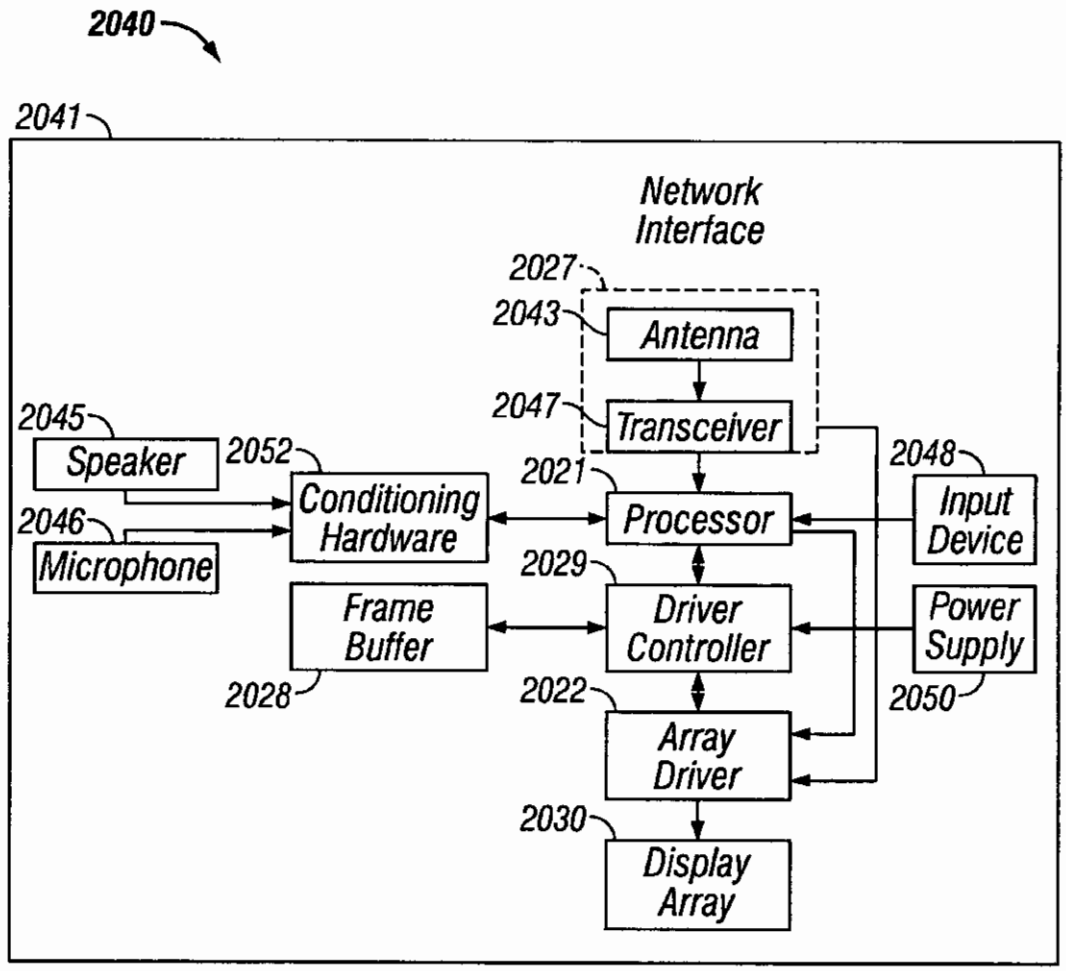


FIG. 28B