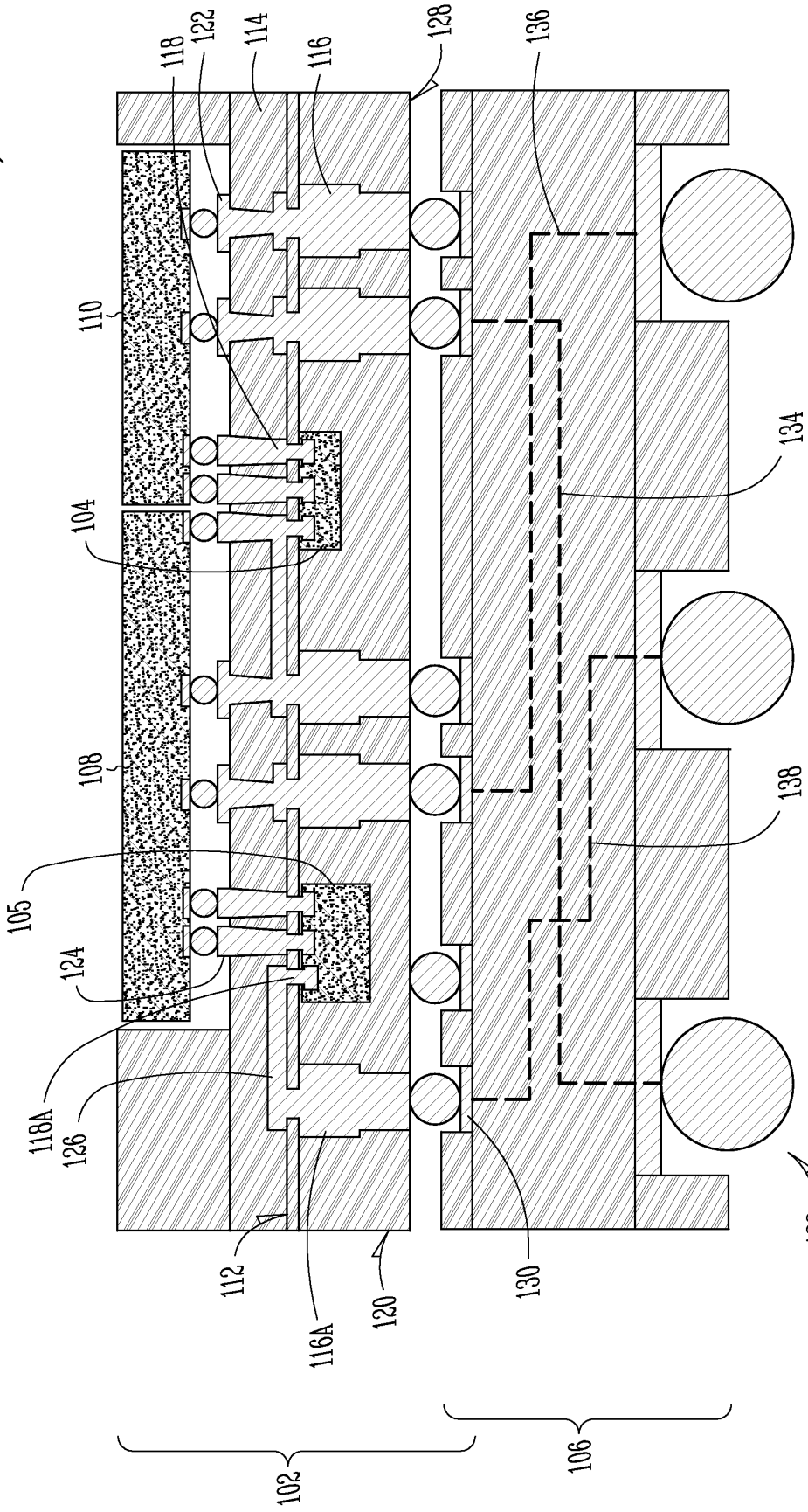

100
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122
114
116
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118A
126
112
116A
120
130
132
102
106

Fig. 1A

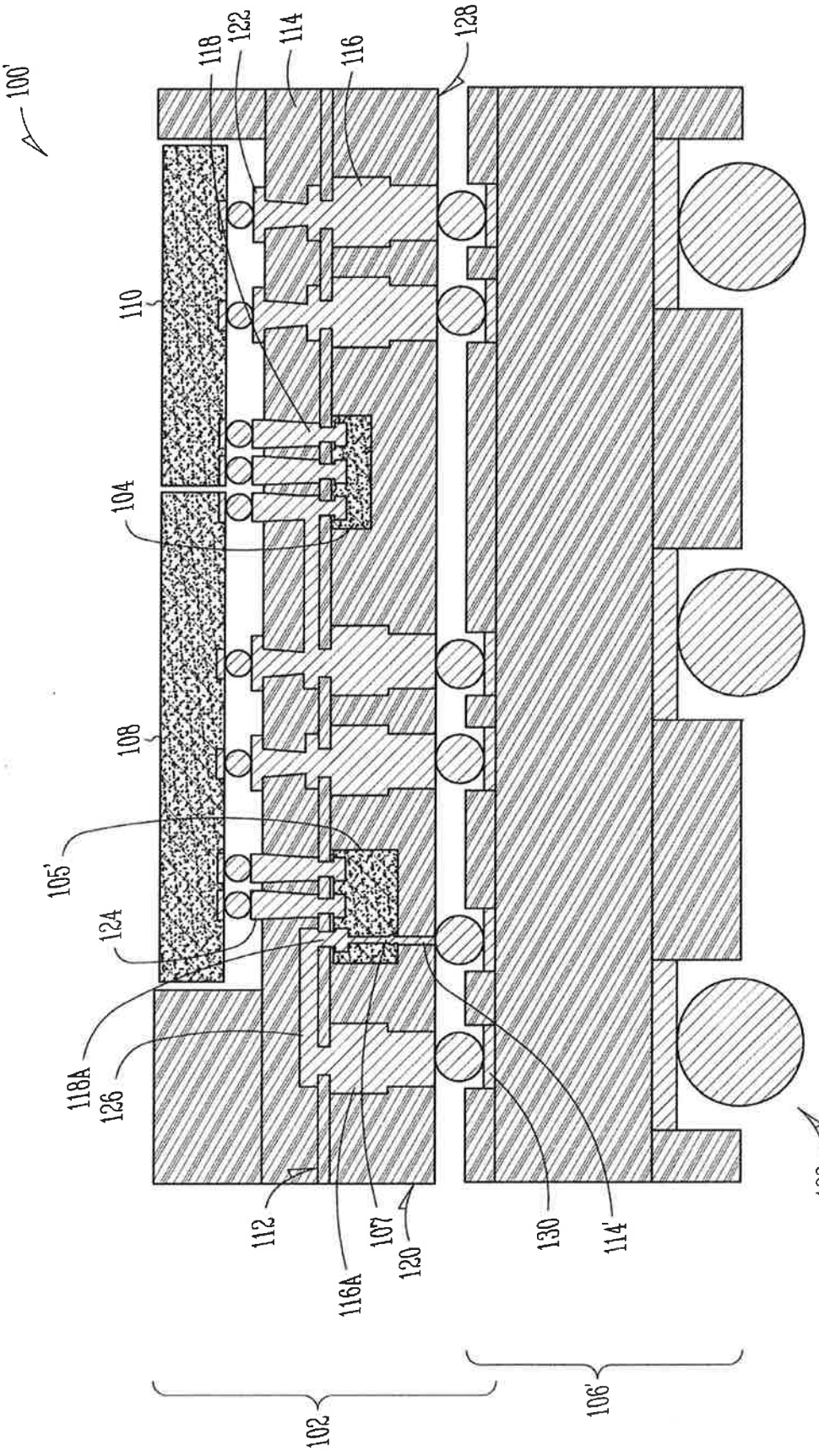

100'
118
122
114
116
128
110
104
108
105'
124
118A
126
112
116A
107
120
130
114'
132
102
106'

Fig. 1B

Fig.2A

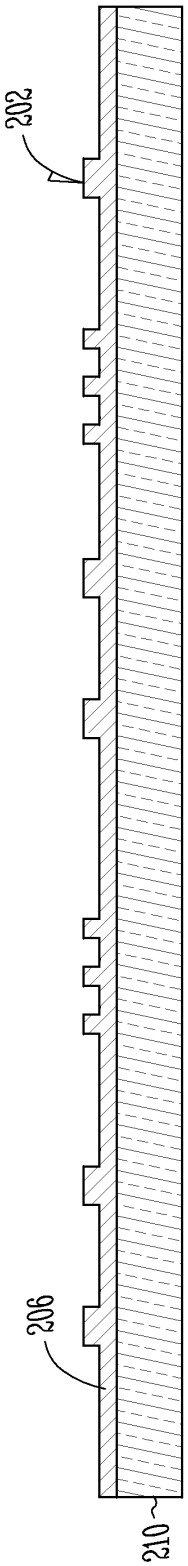


Fig.2B

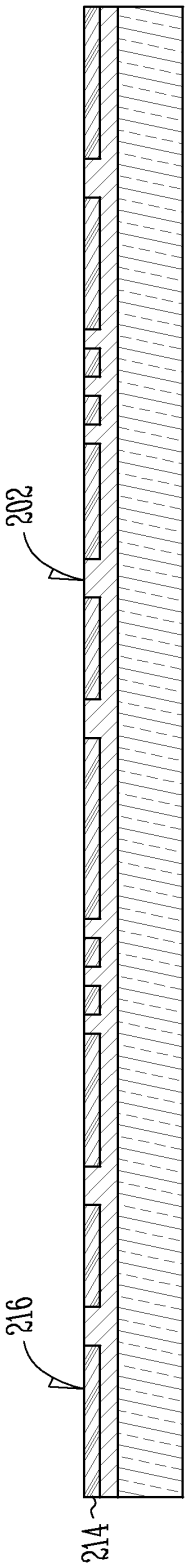


Fig.2C

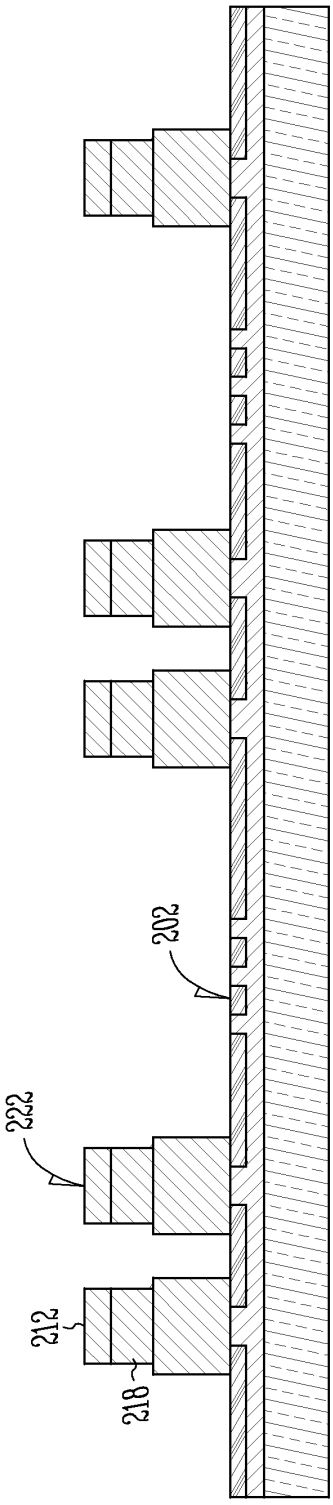


Fig.2D

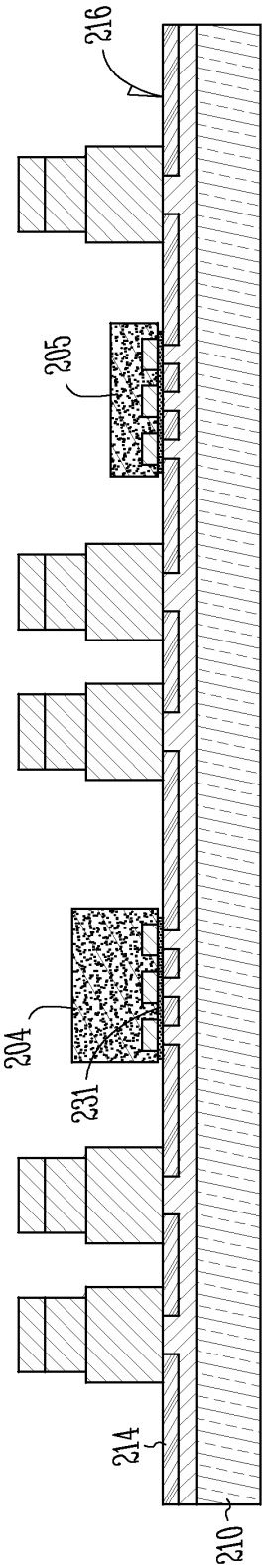


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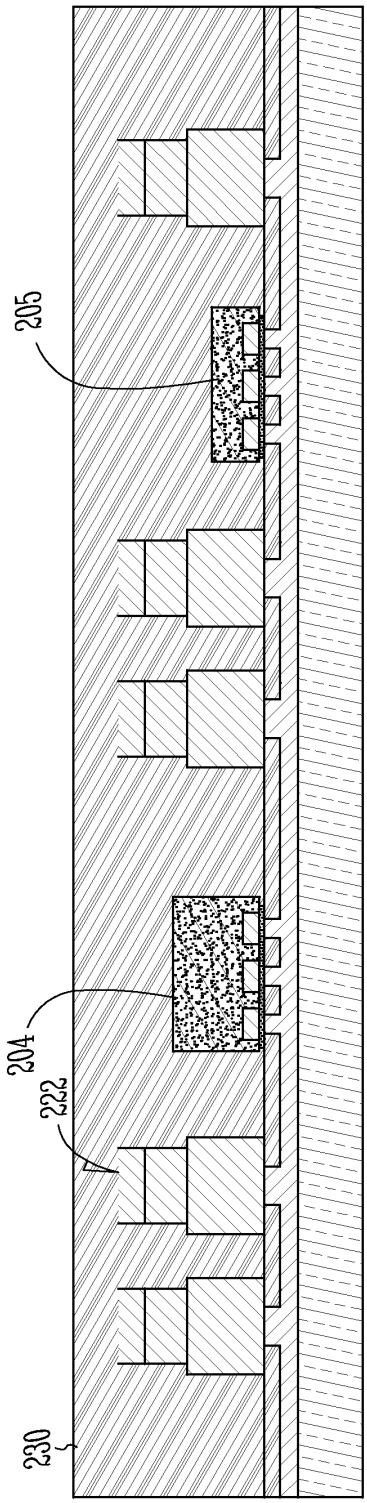


Fig.2F

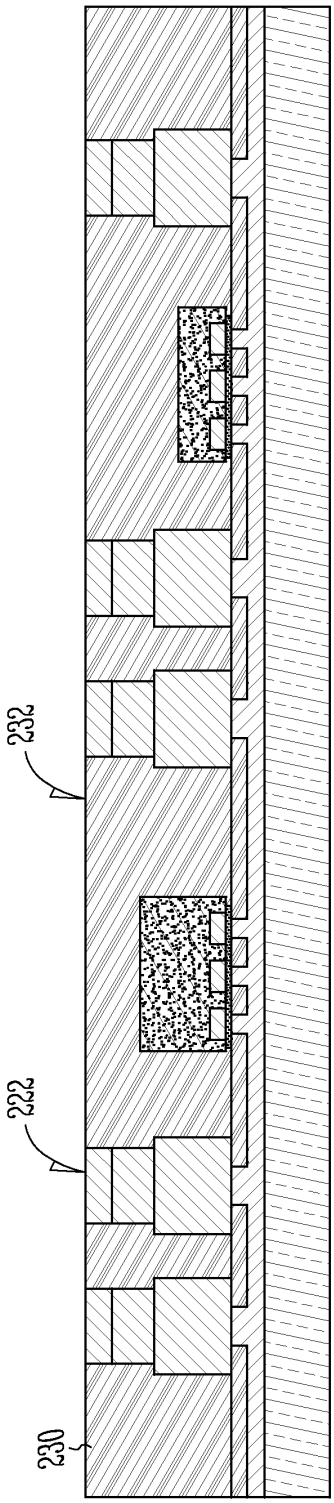


Fig.2G

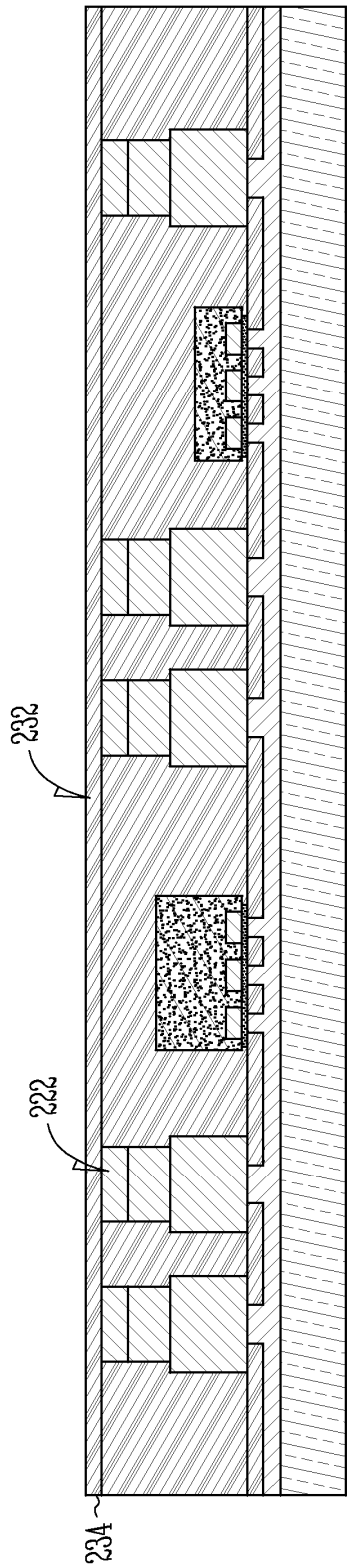


Fig.2H

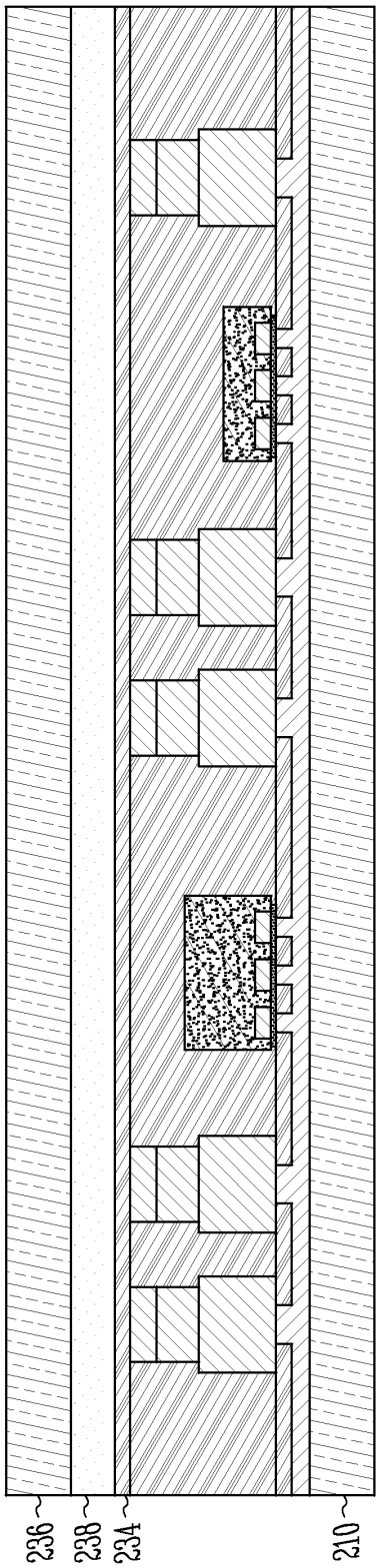


Fig.2I

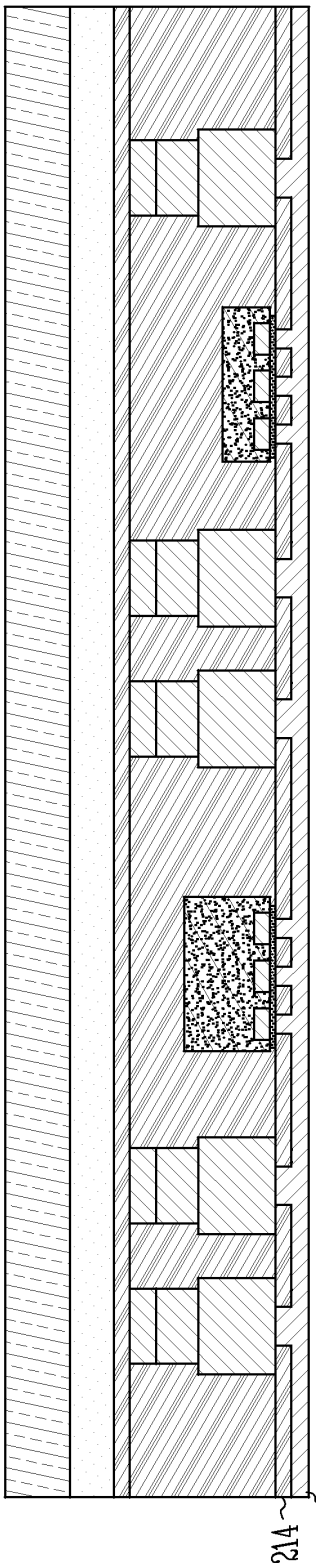


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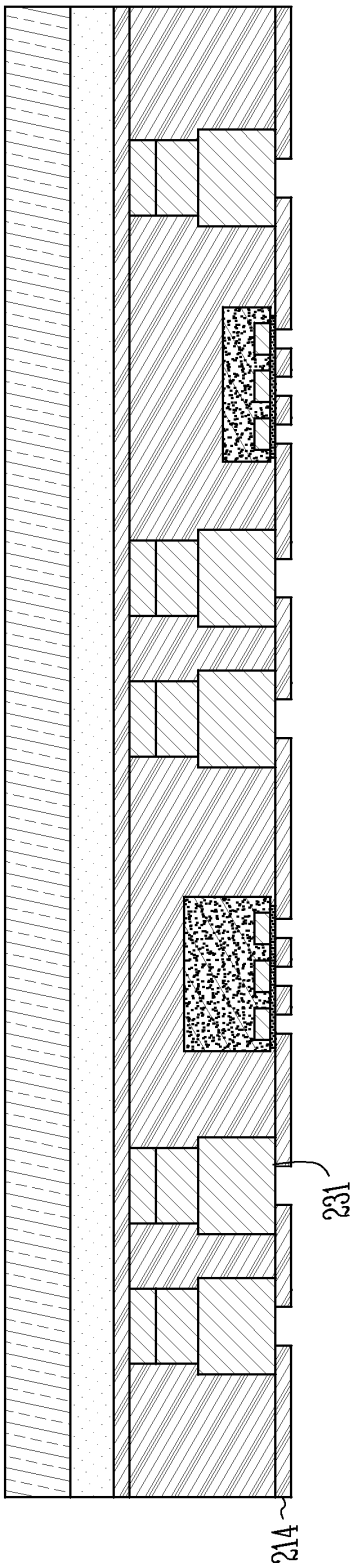


Fig.2K

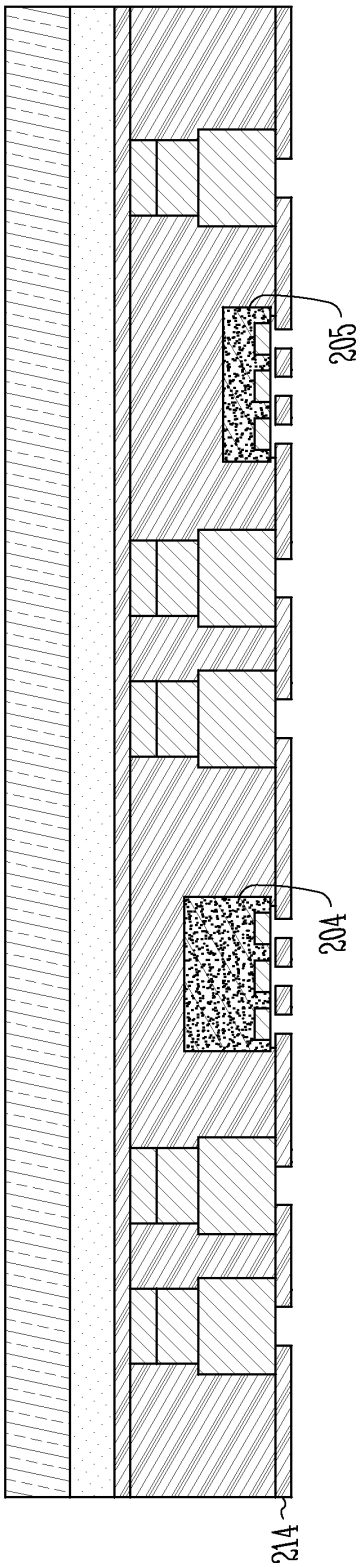


Fig.2L

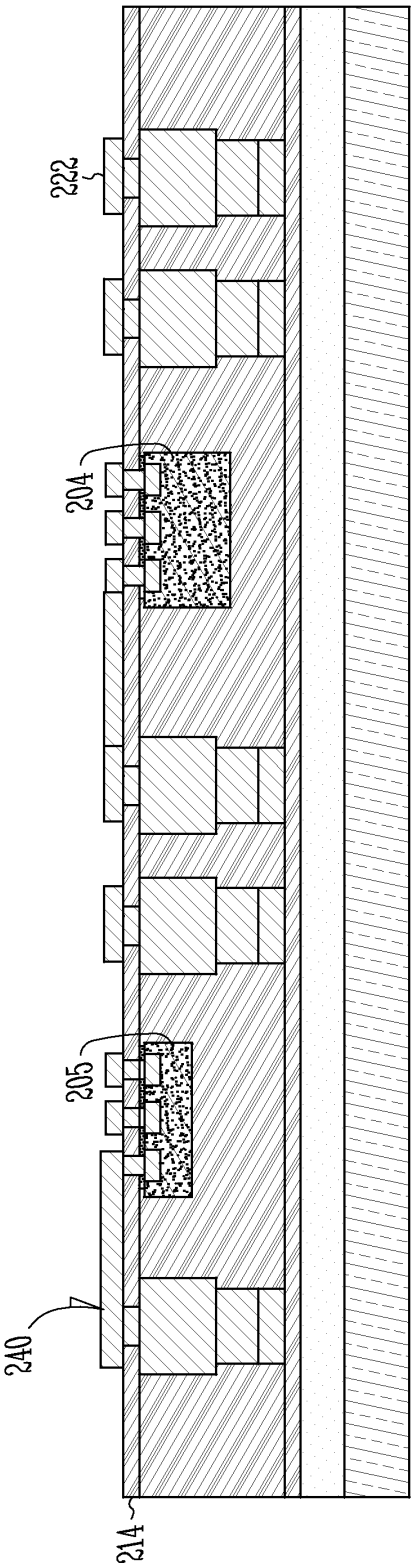


Fig.2M

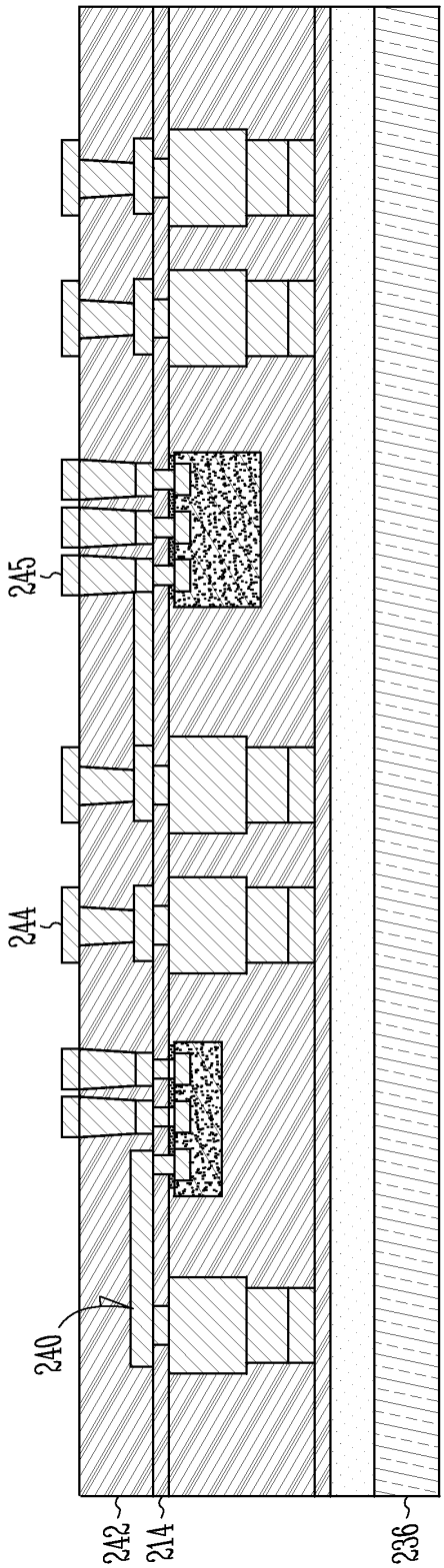


Fig.2N

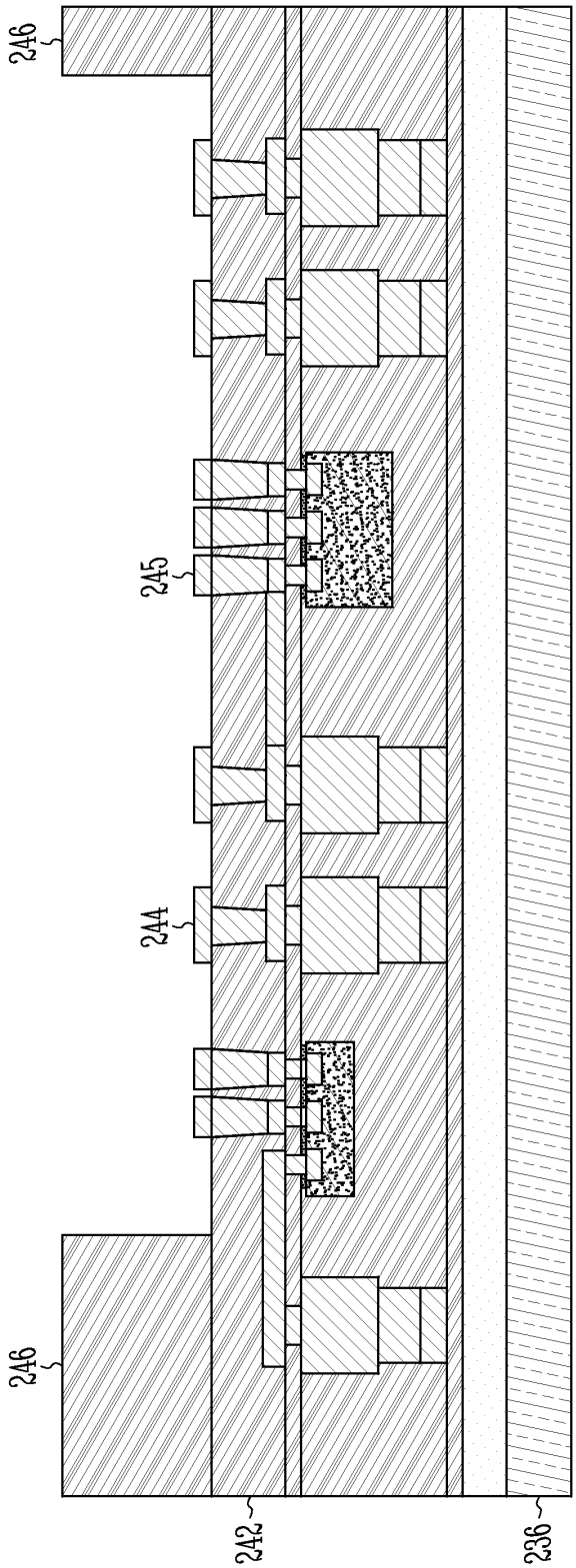


Fig.2O

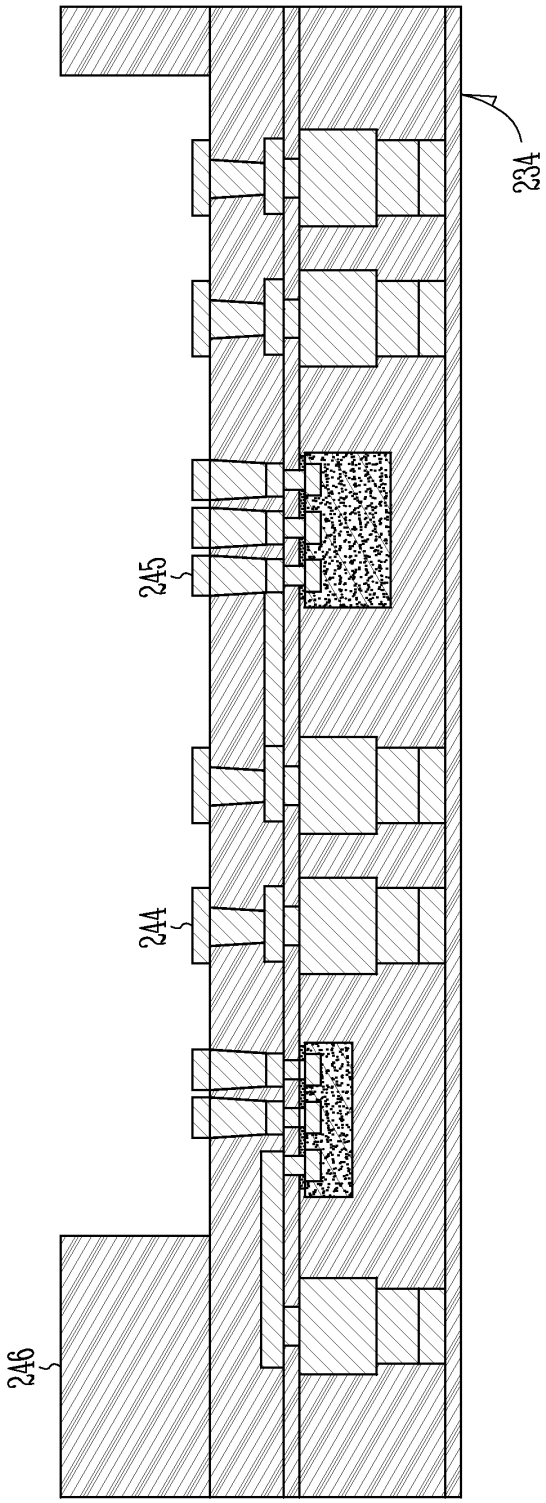


Fig.2P

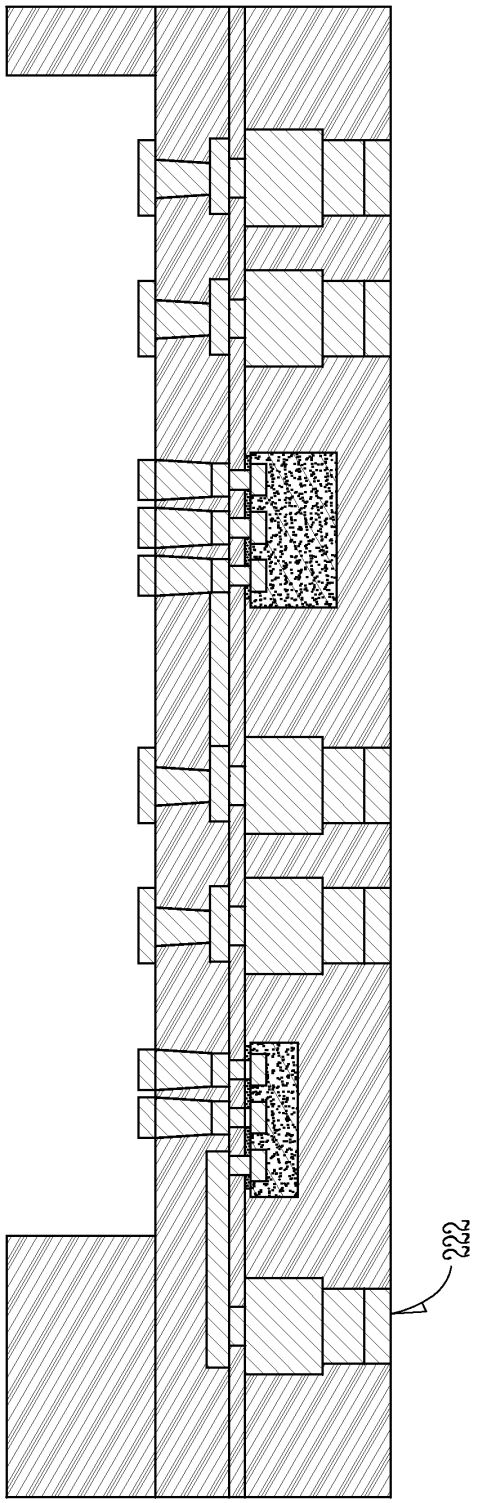


Fig.2Q

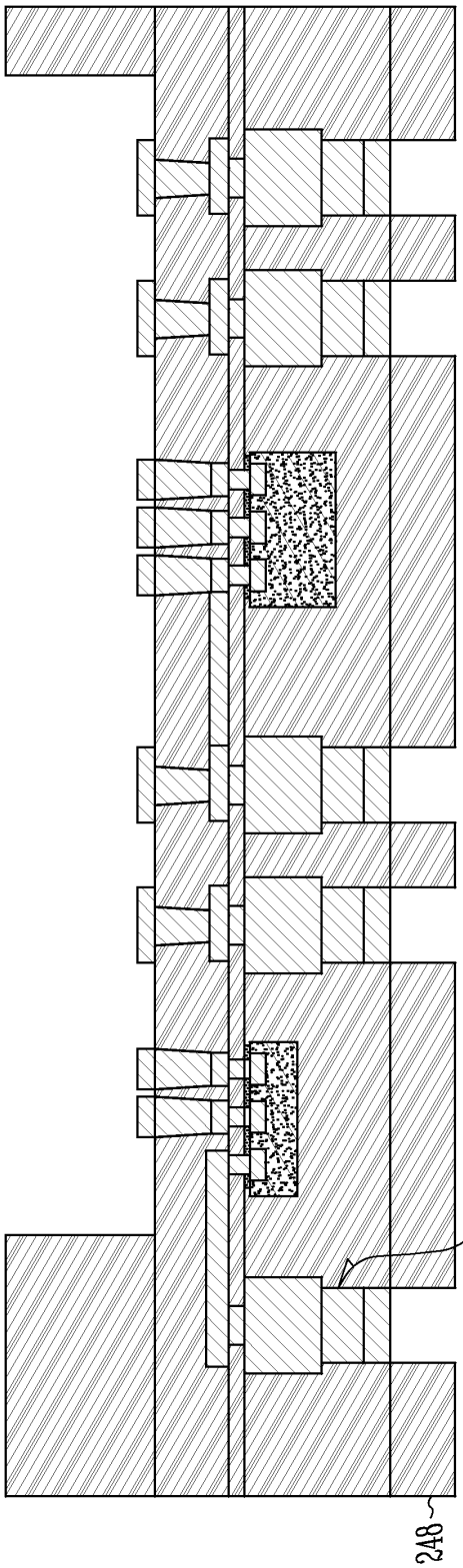


Fig.2R

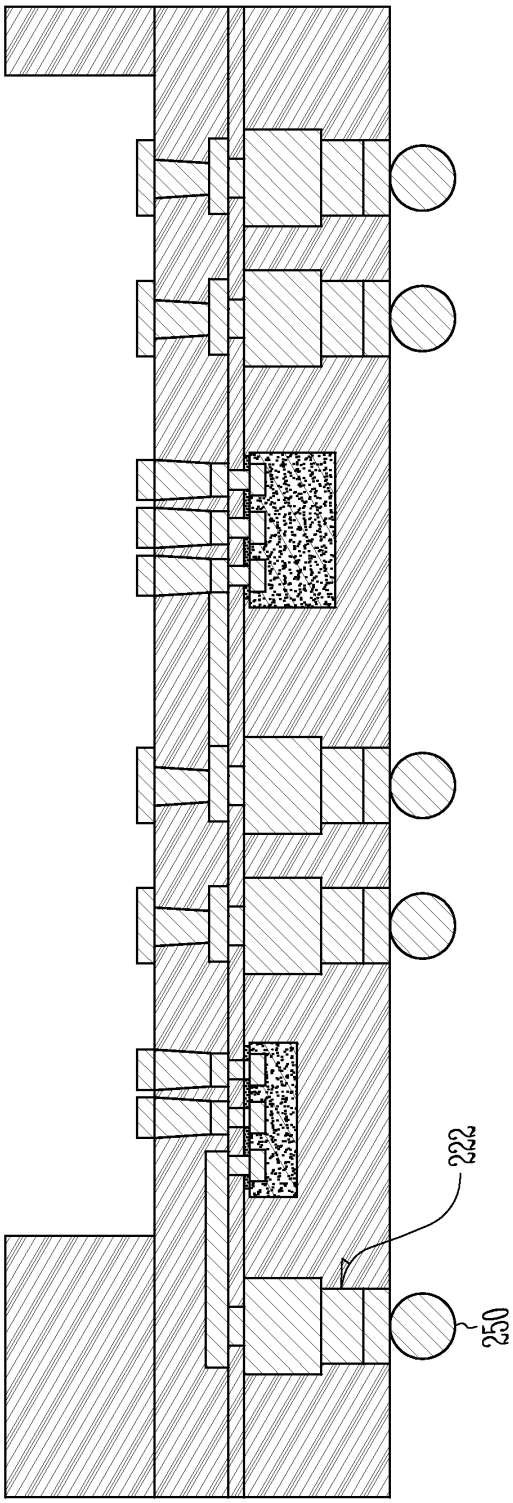


Fig. 3A

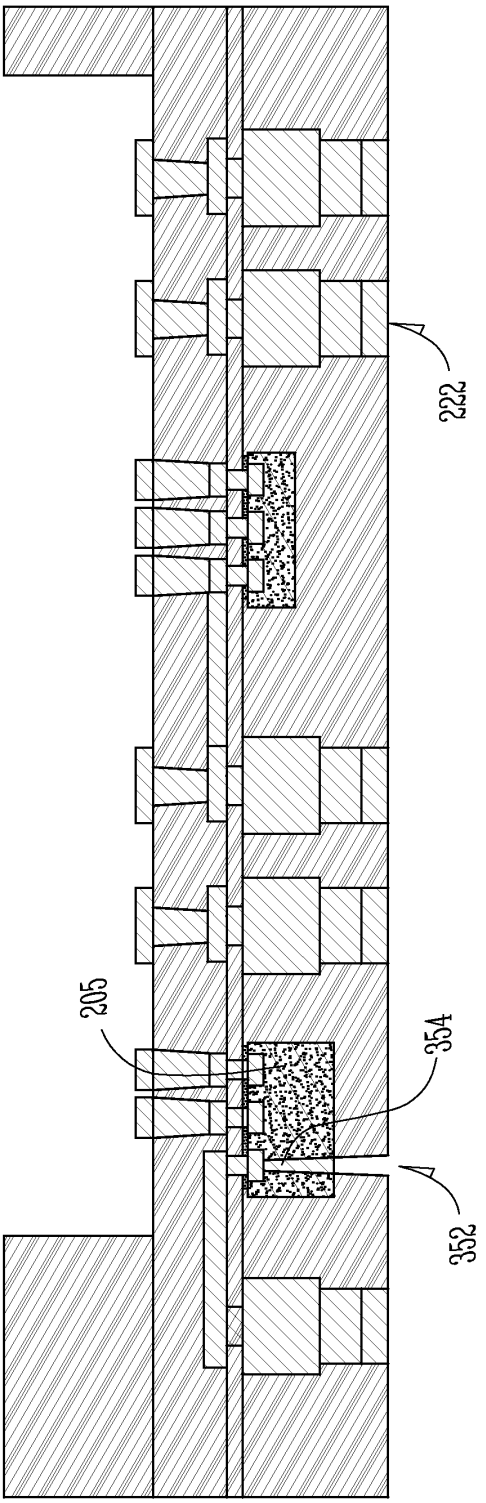


Fig. 3B

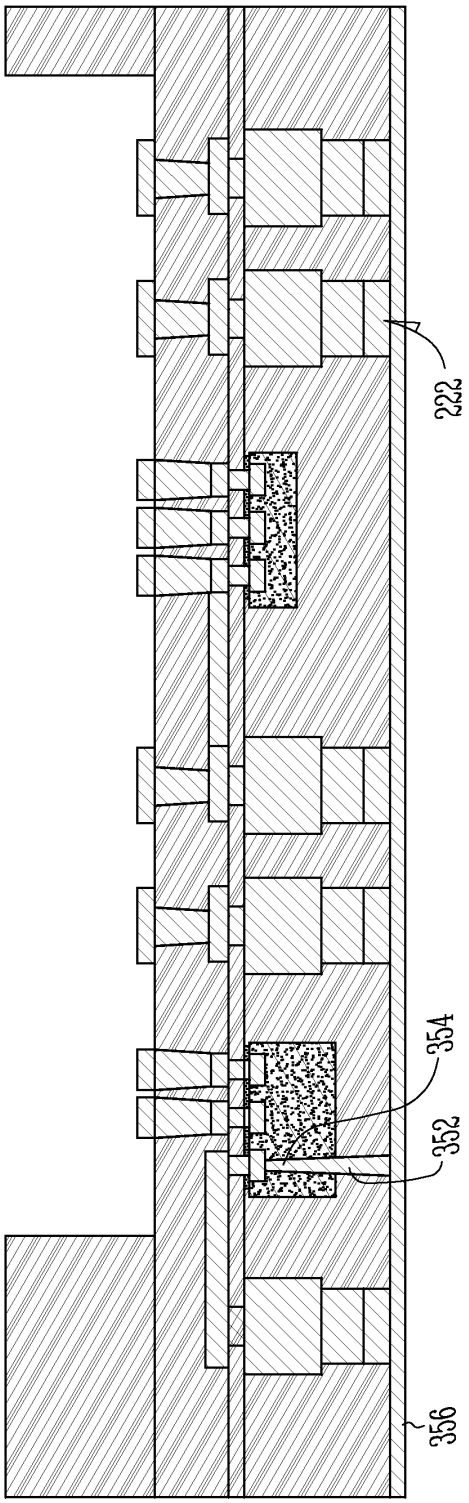


Fig. 3C

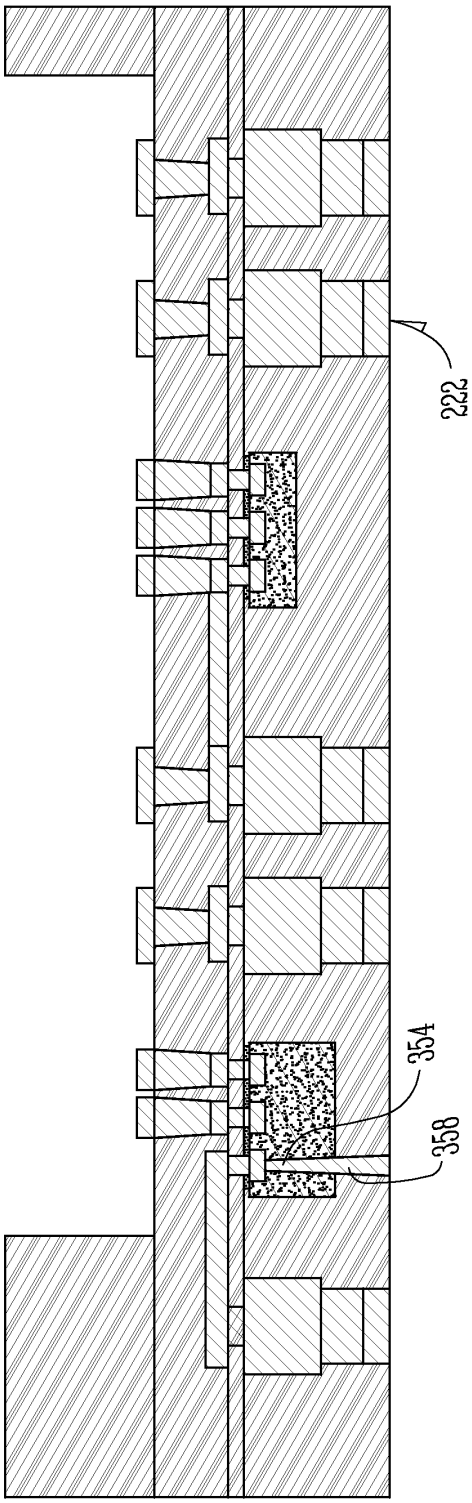
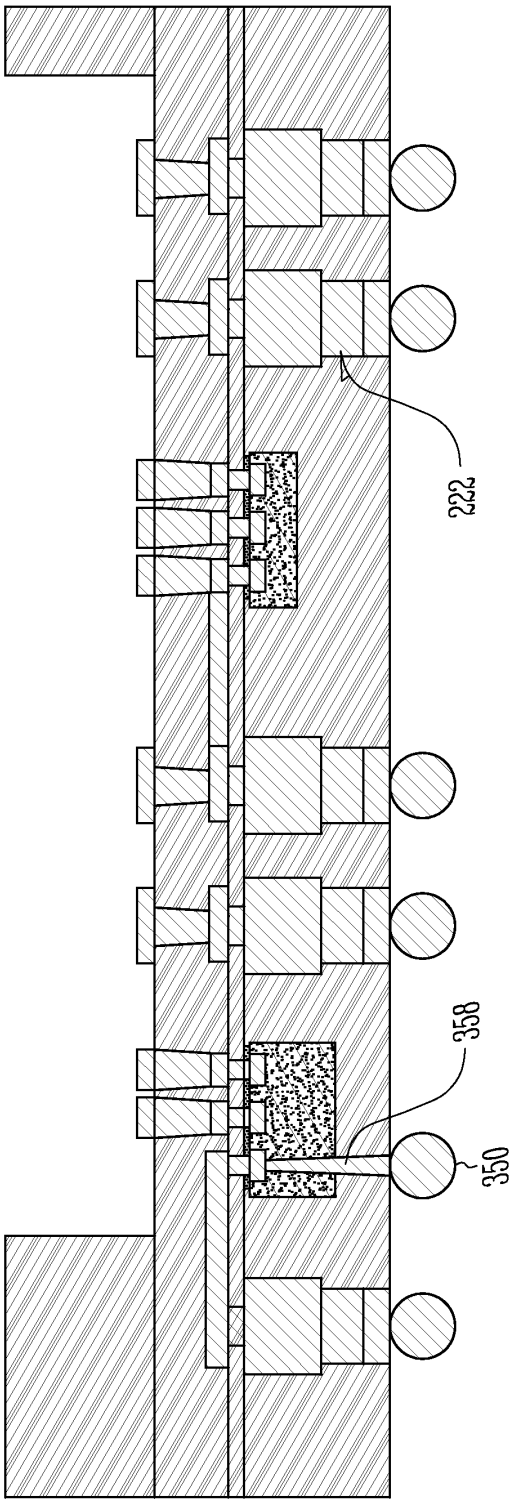


Fig. 3D



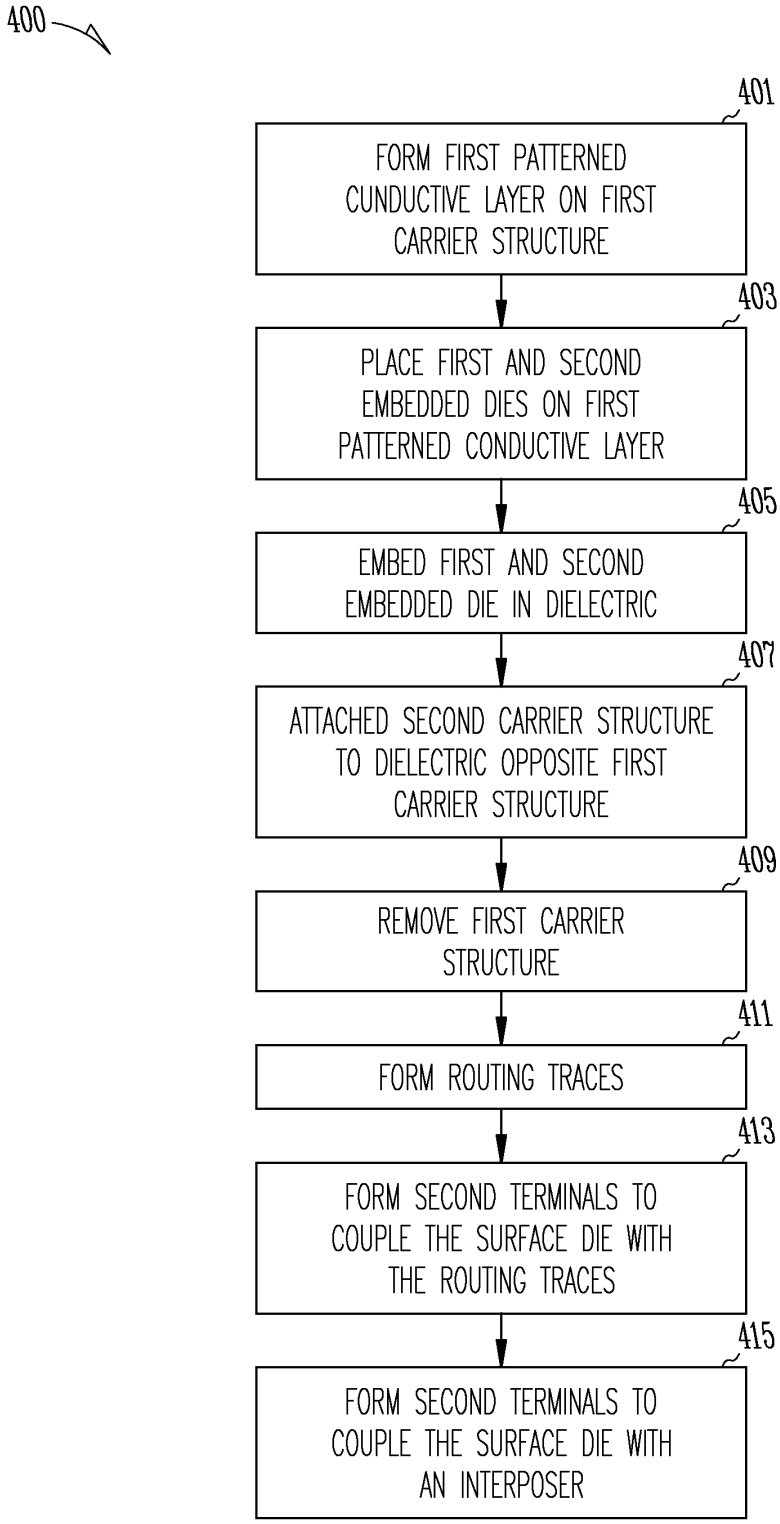

400
401
FORM FIRST PATTERNED CUNDUCTIVE LAYER ON FIRST CARRIER STRUCTURE
403
PLACE FIRST AND SECOND EMBEDDED DIES ON FIRST PATTERNED CONDUCTIVE LAYER
405
EMBED FIRST AND SECOND EMBEDDED DIE IN DIELECTRIC
407
ATTACHED SECOND CARRIER STRUCTURE TO DIELECTRIC OPPOSITE FIRST CARRIER STRUCTURE
409
REMOVE FIRST CARRIER STRUCTURE
411
FORM ROUTING TRACES
413
FORM SECOND TERMINALS TO COUPLE THE SURFACE DIE WITH THE ROUTING TRACES
415
FORM SECOND TERMINALS TO COUPLE THE SURFACE DIE WITH AN INTERPOSER

Fig. 4

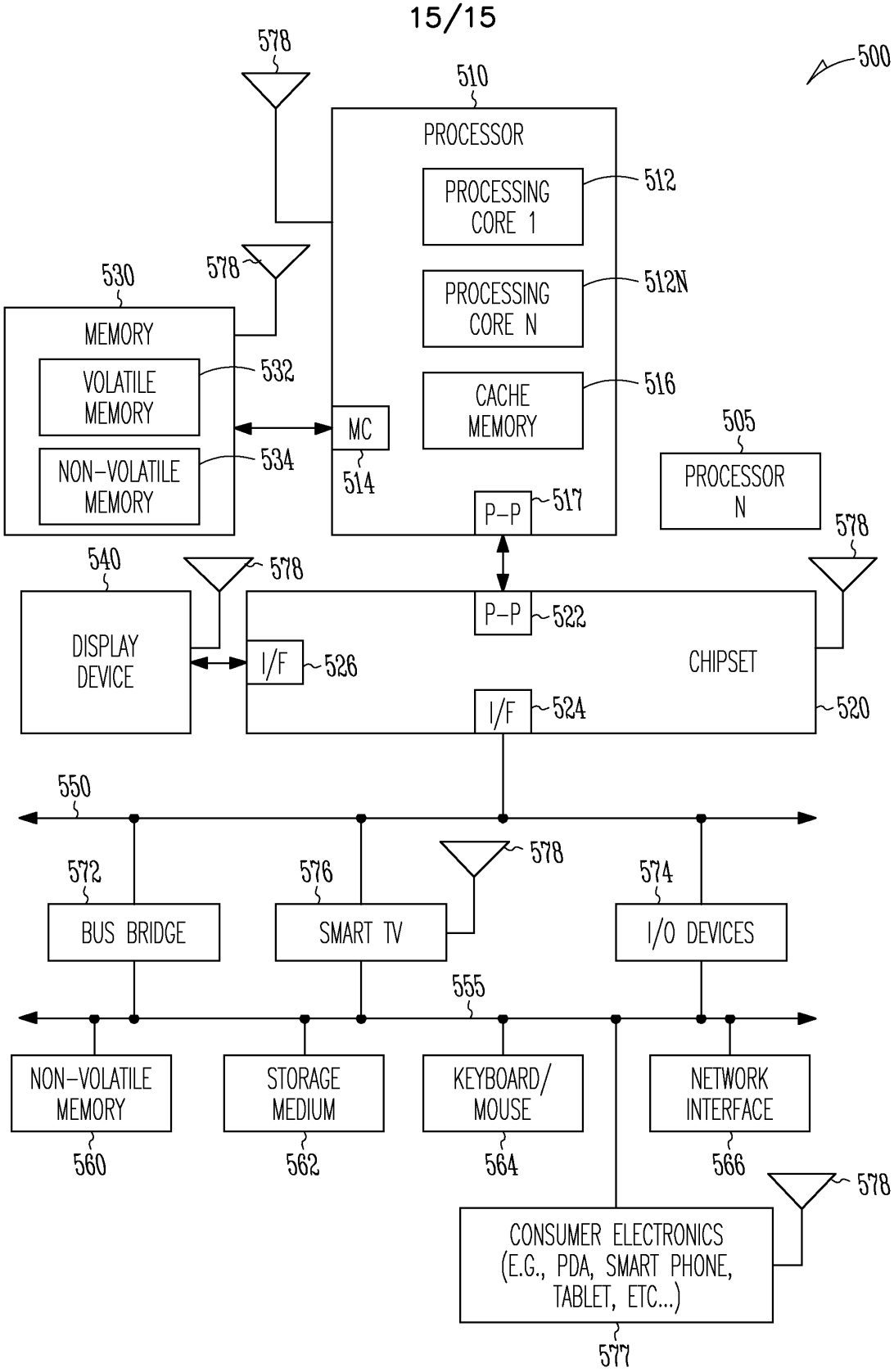

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PROCESSOR
PROCESSING CORE 1
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PROCESSING CORE N
512N
CACHE MEMORY
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MC
514
P-P
517
530
MEMORY
VOLATILE MEMORY
532
NON-VOLATILE MEMORY
534
505
PROCESSOR N
540
DISPLAY DEVICE
I/F
526
P-P
522
I/F
524
CHIPSET
520
550
572
BUS BRIDGE
576
SMART TV
574
I/O DEVICES
555
NON-VOLATILE MEMORY
560
STORAGE MEDIUM
562
KEYBOARD/ MOUSE
564
NETWORK INTERFACE
566
CONSUMER ELECTRONICS (E.G., PDA, SMART PHONE, TABLET, ETC...)
577

Fig. 5