



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G01R	A2	(11) International Publication Number: WO 99/06845 (43) International Publication Date: 11 February 1999 (11.02.99)
(21) International Application Number: PCT/US98/14846 (22) International Filing Date: 17 July 1998 (17.07.98) (30) Priority Data: 08/902,345 29 July 1997 (29.07.97) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): MOONEY, Stephen, R. [US/US]; 17265 N.W. Madras Court, Beaverton, OR 97006 (US). HAYCOCK, Matthew, B. [US/US]; 16206 N.W. Barkton Court, Beaverton, OR 97006 (US). KENNEDY, Joseph, T. [US/US]; 16006 N.W. Lyndel Lane, Beaverton, OR 97006 (US). (74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).		(81) Designated States: AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published Without international search report and to be republished upon receipt of that report.

(54) Title: IMPEDANCE CONTROL CIRCUIT

(57) Abstract

Briefly, in accordance with one embodiment of the invention an integrated circuit includes: a digital feedback control circuit to adjust the impedance of an interface circuit output buffer based, at least in part, on having adjusted the impedance of a non-data signal output buffer coupled to an external impedance. Briefly, in accordance with another embodiment of the invention, a method of digitally adjusting the impedance of an interface circuit output buffer comprises: digitally adjusting the impedance of a non-data signal output buffer coupled to an external impedance, and digitally adjusting the impedance of the interface circuit output buffer based, at least in part, on the digitally adjusted impedance of the non-data signal output buffer.

