MULTI-STEP PLANARIZING AND POLISHING METHOD

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention relates to a method for fabricating a semiconductor device. More particularly, the present invention relates to a method for planarizing and polishing a semiconductor wafer.

Description of Related Art

[0001] In the fabrication of advanced integrated circuits (ICs), it is often necessary to polish a surface of a layer or a structure, such as a semiconductor wafer, to remove topographic irregularities and surface defects including scratches or embedded debris and particles. For example, a dielectric layer may form over a previously patterned layer. The dielectric layer may be used to form an interlevel dielectric or shallow trench isolation. The surface fluctuations and the excessive amount of the deposited dielectric layer may be removed by a planarization process known as chemical mechanical polishing (CMP). It is well aware in the art that providing planar surfaces facilitates the formation of the subsequent layers. And as the level of integration increases and the feature sizes of semiconductor devices continuously reduce, providing planar surfaces become increasingly important since a non-planar topography may result with photo-printing difficulties and problems in etching and step coverage of openings.

[0002] As mentioned above, CMP is a technique commonly used to planarize and

polish semiconductor topography. Typically, CMP is effected through placing a semiconductor wafer on a wafer carrier, pressing the semiconductor wafer against a polishing pad, and introducing an abrasive, chemical slurry into the space between the polishing pad and the wafer surface while the wafer and the polishing pad rotate relative to each other. The slurry is an aqueous suspension of abrasive particles, for example, silica. The chemical in the slurry reacts with the surface material being polished, while the abrasive particles, due to the movement of the polishing pad and the wafer, physically strip the surface material from the wafer.

[0003] However, many problems are associated with the CMP technique. For example, during the fabrication of shallow trench isolation (STI), a CVD (chemical vapor deposition) oxide is deposited on the substrate and is subsequently planarized by CMP. The substrate, which is already formed with trenches therein, is also covered by a silicon nitride etch-stop layer on the surface before forming the CVD oxide. To ensure a complete removal of the CVD oxide in the low pattern density region, it is necessary to over polish the high pattern density region. The over polishing, however, may result in "dishing" of the trench oxide and "erosion" of the adjacent silicon nitride. Dishing is the formation of a concave depression in the trench oxide, while "erosion" is an uneven removal of the adjacent nitride layer. Another problem that may be encountered in the CMP process is the "loading effect" in which an irregular surface is formed on the polished structure due to a deformed polishing pad.

[0004] One conventional solution to these problems in the CMP process is the application of a reverse-tone mask. The reverse-tone mask having openings that expose the active regions is formed over the trench-filled oxide layer, and a portion of the exposed oxide layer within the openings is etched back. CMP is subsequently used

to planarize the oxide layer remaining on the active regions and the trench regions. The reverse masking, however, adds an additional lithography and etching process. Therefore, the cost is increased and the cycle time is prolonged. Moreover, reverse masking still suffers from poor uniformity problems.

[0005] Other approach to resolve the abovementioned problems is by employing fixed abrasive pads (FA) in a CMP process, in which abrasive material is embedded into the polishing pad. Polishing by FA pads is achieved by a frictional contact between the wafer and the polishing pad when the wafer on the carrier is pushed against the polishing pad. Accordingly, FA-CMP is effective in planarizing typography and in providing global uniformity. However, there are also issues associated with this approach, such as drop of the removal rate. The removal rate of a FA-CMP process is a function of the local step height; for example, the removal rate of the up area is fast, while the removal rate of the down area approaches zero. Frequently, the FA-CMP process may come to a halt before the topography of the entire wafer is completely planarized. Ultimately, the drop of the removal rate leads to a low throughput. Moreover, since a polishing process using FA pads operates in a time mode basis, overpolishing due to a thickness variation of the incoming wafers is often resulted. Alternatively, high selectivity slurry (HSS) has been employed to maximize the oxide-to-nitride selectivity and to mitigate the effects of erosion and dishing. However, HSS also suffers from removal rate drop and removal rate deviation, which ultimately impacts on the throughput. A two-step polishing process has also been proposed to address the above-mentioned problems. The two-step polishing process may include a first polishing step to remove the topography on a substrate surface by polishing with an abrasive-containing polishing composition, for example, containing silica abrasives, and

an abrasive-free polishing pad, and then polishing the substrate with a fixed abrasive (FA) polishing pad. However, even combining a "regular" polishing step using silica abrasives with a polishing step using a FA pad, it has been observed that the within-die uniformity remains undesirable. Further, the thickness deviation of the incoming wafers entering the FA polishing step is high; therefore, overpolishing as commonly occurred in polishing with a FA pad is still resulted.

[0006] Other two-step polishing process may include a high selectivity slurry (HSS) based polishing step and a FA based polishing step. Since polishing with HSS typically results with high removal rate deviation, the wafer-to-wafer uniformity is undesirable. Moreover, the thickness deviation of the incoming wafers entering the FA based polishing step is high, the problem of overpolishing remains a great concern. Further, both the HSS based and the FA based polishing processes exhibit removal rate drop; low throughput is ultimately resulted.

[0007] Yet another two-step polishing process may include a "typical" polishing step using silica abrasives, for example, and a high selectivity slurry (HSS) based polishing step. However, completing a polishing process with a HSS based polishing step remains undesirable since the HSS based polishing process exhibits high removal rate deviation and removal rate drop. Further, global uniformity can not be attained.

[0008] In summary, the conventional one step or two-step polishing methods are unable to concurrently achieve global uniformity, local planarity and high throughput.

SUMMARY OF THE INVENTION

[0009] In view of the deficiencies of the conventional approaches for forming a planarized and polished surface, the present invention provides a multi-step planarizing

and polishing method, wherein the throughput is optimized.

[0010] The present invention also provides a multi-step planarizing and polishing method, wherein local planarity and within-die uniformity are improved.

[0011] The present invention also provides a multi-step planarizing and polishing method, wherein global uniformity is improved.

[0012] The present invention further provides a multi-step planarizing and polishing method, wherein the problem of overpolishing and underpolishing that is often occurred in a polishing process using a fixed abrasive (FA) pad can be precluded.

[0013] According to one aspect of the multi-step planarizing and polishing method for removing topography from a semiconductor wafer of the present invention, a first polishing step is performed with a first polishing pad and a first slurry composition. Thereafter, a second polishing step is performed with a second polishing pad and a second slurry composition. In this aspect of the invention, the first slurry composition may include at least silica abrasives, and the second slurry composition may include at least CeO_2 abrasives. Further, in accordance to the present invention, the thickness deviation of wafers at the end of the second polishing step is controlled. Thereafter, a third polishing step is performed using a fixed-abrasive pad.

[0014] In accordance to this aspect of the invention, the second polishing step is controlled by an endpoint detection mechanism, for example.

[0015] In accordance to this aspect of the invention, the first and second polishing pads are "standard" pad without embedded abrasive particles.

[0016] In accordance to this aspect of the invention, the bulk of a material layer is removed in the first polishing step using silica abrasives based slurry. Accordingly, the polishing rate of the first polishing step is high and the throughput of the overall process

is improved.

[0017] Further, the second polishing step of this aspect of the invention employs CeO_2 abrasives. Therefore, the within-die uniformity can be achieved. Additionally, the thickness deviation of wafers is well controlled by the end of the second polishing step. Accordingly, not only the issue of overpolishing that is often occurred in a FA polishing step can be obviated, global uniformity is achieved.

[0018] According to another aspect of the multi-step planarizing and polishing method for removing topography from a semiconductor wafer of the present invention, a first polishing step and a second polishing step are respectively performed with a first slurry composition and a second slurry composition. In accordance to this aspect of the invention, the first slurry composition may include at least CeO_2 abrasives, and the second slurry composition may include at least silica abrasives. Further, the remaining thickness the polished material at the end of the second polishing step is well controlled. Thereafter, a third polishing step is performed using a fixed-abrasive pad.

[0019] In accordance to this aspect of the invention, the second polishing step is controlled by an endpoint detection mechanism, for example.

[0020] In accordance to this aspect of the invention, the first and second polishing steps employ, for example, "standard" pads without embedded abrasive particles.

[0021] In accordance to this aspect of the invention, the first and second polishing steps include polishing with CeO_2 abrasives which can provide excellent within-die uniformity, and polishing with silica abrasives which can provide high removal rate. Thus, subsequent to the first two polishing steps, not only the throughput of the overall process is high, the within-die uniformity is also improved. Further, since the second polishing step is controlled by means of an end point detection mechanism, the

thickness deviation of the polished material before entering the third polishing step using a fixed-abrasive pad is minimized. Therefore, the problem of overpolishing that is often confronted in a FA polishing process can be obviated, while global uniformity is achieved.

[0022] According to the multi-step planarizing and polishing method of the present invention, improved throughput, good local planarizity and global uniformity can be achieved.

[0023] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0025] Figures 1A to 1D are schematic, cross-sectional views showing selected steps for fabrication of a semiconductor structure having patterned features according to a first embodiment of the multi-step planarizing and polishing method of the present invention.

[0026] Fig. 2 is a flow chart of exemplary process steps of the multi-step planarizing and polishing method according to the first embodiment of the present invention.

[0027] Fig. 3 is a flow chart of exemplary process steps of the multi-step planarizing and polishing method according to the second embodiment of the present

invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

[0028] Figures 1A to 1C are schematic, cross-sectional views showing selected steps for fabricating a semiconductor structure having patterned features according to a first embodiment of the multi-step planarizing and polishing method of the present invention. In one aspect of the invention, the patterned features may include a trench structure, a contact structure or a via structure. For illustration purposes, the present invention is described herein with respect to a trench structure, for example, a trench isolation structure. However, it is appreciated that the application of the planarizing and polishing method introduced herein is not restricted in the fabrication of a trench structure or a trench isolation structure.

[0029] Referring to Figure 1A, a substrate 100 is defined into active regions by first forming a pad layer 102 and a barrier/polishing stop layer 104 thereon, followed by performing a photolithograph and etching process to form a plurality of trenches 106 in the substrate 100. The pad layer 102 is, for example, a silicon oxide layer, while the barrier/polishing stop layer 104 is a silicon nitride layer, for example. Alternatively, other suitable pad layers or stop layers can be used in accordance with the invention. A material layer 108 is then blanket deposited over the substrate 100 to a thickness of about 6000 Å to 7000 Å, for example, filling the trenches 106. The material layer 108, typically a thick oxide layer, may form by performing a high density plasma chemical vapor deposition (HDPCVD), followed by an annealing process at about 1100°C for densification purposes. The deposited material layer 108 generally has an excessive

overburden with a non-uniform surface topography.

[0030] Accordingly, a planarizing and polishing process is to be performed on the deposited material layer 108. In this embodiment of the invention, the multi-step planarizing and polishing method includes at least three polishing steps, which may be conducted in a three-platen polishing apparatus, for example. As shown in Figure 1B, the first step of a three-step polishing process is performed to remove the excessive overburden of the material layer 108. According to one embodiment of the invention, the first step of the multi-step polishing process employs a slurry composition and a polishing pad. The polishing pad used in the first planarizing and polishing step includes but not limited to a "standard" polishing pad. A "standard" polishing pad typically has a durable surface, without embedded abrasive particles. The slurry composition used in the first planarizing and polishing step may comprise, for example silica abrasives, such as Cabot SS-25, which is a commercial slurry from Cabot Corporation. The first planarizing and polishing step is performed to remove substantially the bulk of the material layer 108 with a relatively high polishing rate. Ultimately, the first step of the multi-step planarizing and polishing method ensures a high throughput for the overall process.

[0031] Continuing to Figure 1C, the second step of the three-step polishing process is performed. According to the one embodiment of the invention, the second step of the three-step polishing process is performed using a polishing pad and a slurry composition. The polishing pad used in the second polishing step includes but not limited to a "standard" polishing pad. In the second polishing step, the slurry composition comprises at least CeO_2 (Cerium Oxide) abrasives, for example. In one aspect of the invention, high selectivity slurry comprising CeO_2, such as Cabot HSS or

Asahi HSS, may be used. According to the first embodiment of the invention, the second polishing step is controlled to terminate near the interface between the material layer 108 and the stop layer 104, for example, by an end point detection apparatus. The thickness of the material layer 108 remaining over the substrate 100 surface is controlled to about 0 to 100Å, for example. The polishing pad used in the second polishing step may be the same or a different polishing pad used in the first polishing step.

[0032] Thereafter, the third step of the three-step polishing process is performed to polish the remaining material layer 108 to form a planarized surface of the isolated structures as shown in Figure 1D. In the third polishing step, a fixed abrasive (FA) polishing pad is employed. Further, a third slurry composition may or may not be included in this polishing step.

[0033] Fig. 2 summarizes the exemplary process steps of the multi-step planarizing and polishing method according to the first embodiment of the present invention. As shown in Figure 2, the multi-step polishing method of the invention is commenced by polishing with a "standard" polishing pad and silica abrasives containing slurry as in step 201. In step 202, a "standard" polishing pad and CeO_2 abrasives containing slurry are used to perform the second polishing step. Thereafter, in step 203, a fixed abrasive polishing pad is used perform the third polishing step. In step 203, a slurry composition is optional.

[0034] In accordance to the first exemplary embodiment of the multi-step planarizing and polishing method of the present invention, the bulk of the material layer is first removed in the silica abrasives based polishing step, in which the removal rate is high, followed by a CeO_2 abrasives based polishing step. Therefore, the overall polishing

can be accomplished in effective polishing times. Further, it has been determined by the present invention that polishing with CeO_2 abrasives provides excellent within die uniformity. Hence, after the completion of the first two polishing steps, not only the throughput of the overall process is high, the within-die uniformity is also improved. Further, since the second polishing step is controlled by means of an end point detection mechanism, the thickness deviation of the wafers entering the third polishing step using a fixed-abrasive pad can be minimized. Therefore, the problem of overpolishing that is often confronted in a FA polishing process can be obviated, while global uniformity is achieved. According to the multi-step planarizing and polishing method of the present invention, improved throughput, good local planarity and global uniformity are achieved.

[0035] It is worthy to note that the benefits provided by this invention can not be achieved by any conventional two-step polishing method. As mentioned above, a two-step polishing method may include a "typical" polishing step using silica abrasives, for example, with a polishing step using a FA pad. Although the overall polishing rate may be improved by the "typical" polishing step, the thickness deviation of the incoming wafers entering the polishing step using a FA pad is high. Therefore, the problem of overpolishing or underpolishing may still occur. Further, the within-in die uniformity has not improved. Other two-step polishing method may include a high selectivity slurry (HSS) based polishing step and a FA pad based polishing step. Since polishing with HSS typically results with high removal rate deviation, the wafer-to-wafer uniformity is thus undesirable. Further, the thickness deviation of the incoming wafers entering the FA based polishing step is high, and overpolishing or underpolishing is still a serious problem. Additionally, both HSS based polishing and

FA based polishing have removal rate drop problems, the throughput of the overall process is thus undesirable. Another two-step polishing method may include a "typical" polishing step using silica abrasives, for example, and a HSS based polishing step. However, completing a polishing process with a HSS based polishing step remains undesirable since the HSS based polishing process has high removal rate deviation. Further, global uniformity is not achieved and localized dishing problem occurs.

[0036] It is also worthy to note that the benefits provided by the multi-step planarizing and polishing method of this invention can not be achieved by any combination or sequence of the polishing steps. For example, since a polishing step using a FA pad gradually decelerates and results in a drop of the removal rate, FA polishing is not preferred as a first polishing step. Instead, since FA polishing can provide excellent global uniformity, completing the multi-step polishing process is preferable as long as the thickness variation of the wafer is well controlled before entering the FA polishing step. Further, although a "typical" polishing step using, for example, silica abrasives may provide a high throughput, completing the multi-step polishing process with a "typical" polishing step will result in poor local and global uniformities. Even a HSS polishing step using CeO_2 abrasives may also provide a desirable oxide-to-nitride selectivity, a high removal rate deviation and a high removal rate drop suffered in a HSS polishing step render the HSS polishing step unsuitable for completing the multi-step polishing process. However, it has been demonstrated that CeO_2 abrasives can provide with-die uniformity, a high selectivity slurry comprising CeO_2 abrasives is adopted for the multi-step planarizing and polishing method. Accordingly, in the above embodiment of the multi-step planarizing and polishing

method of the present invention, a "typical" polishing step using, for example, silica abrasives is first provided to enhance the overall throughput of the process, followed by a HSS polishing step to furnish a with-in die uniformity and completing the multi-step polishing process with a FA polishing step to achieve the desired global uniformity. Further, the wafer-to-wafer uniformity before entering the FA polishing step is well controlled by means of an end point detection mechanism incorporated in the polishing step before the FA polishing step, the problem of overpolishing that is often occurred in FA polishing can be obviated, while global uniformity is achieved.

Second Embodiment

[0037] The multi-step planarizing and polishing method of the present invention may also be conducted alternatively according to a second embodiment of the invention. Referring to Figure 3, Figure 3 is a flow chart of exemplary steps of the multi-step planarizing and polishing method according to the second embodiment of the present invention. As shown in step 301, the multi-step planarizing and polishing method of the second embodiment of the invention is initiated by performing the first polishing step using a polishing pad and a slurry composition to remove and polish a portion of the overburden of the material layer 108. The polishing pad used in the first polishing step 310 in this embodiment includes but not limited to a "standard" polishing pad. Further, the slurry composition used in the first polishing step comprises at least CeO_2 abrasives, for example. In one aspect of the invention, high selectivity slurry comprising CeO_2 abrasives, such as Cabot HSS or Asahi HSS, may be used. In this first polishing step using CeO_2 abrasives, only a portion of the excessive overburden of the material layer is removed. Therefore, the polishing can be accomplished with

effective polishing rates, while the within-die uniformity is achieved.

[0038] Thereafter, the second polishing step of the multi-step polishing and planarizing method is conducted using, for example, a "standard" polishing pad, for example, and a slurry composition as in step 302. The slurry composition used in the second polishing step comprises, for example silica abrasives, such as Cabot SS-25. This second polishing step, which has a high polishing rate, removes the bulk of the material layer 108. According to the second embodiment of the invention, the second polishing step is controlled to terminate near the interface between the oxide layer 102 and the stop layer 104, for example, by an end point detection apparatus. The material layer 108 remaining over the substrate 100 surface is controlled to about 0 to 100Å thick, for example. Since polishing with a "standard" polishing pad and a silica abrasives containing slurry composition can be accomplished at a relatively high polishing rate, the second polishing step of this embodiment of the multi-step planarizing and polishing method warrants a high throughput of the overall process.

[0039] Thereafter, the third step of the multi-step planarizing and polishing method is performed in step 303 to polish the remaining material layer 108 to form a planarized surface of the isolated structures. In the third polishing step, a fixed abrasive (FA) polishing pad is employed. Further, a slurry composition may or may not be included in this polishing step. The third polishing step employing a FA polishing pad is performed for a fixed period of time to provide a polished surface of the material layer 108 and global uniformity.

[0040] In accordance to the second exemplary embodiment of the planarizing and polishing method of the present invention, polishing with CeO_2 abrasives can provide excellent within-die uniformity, while polishing silica abrasives can provide high

removal rate. Therefore, after the completion of the second polishing step, not only the throughput of the overall process is high, the within-die uniformity is also improved. Further, the second polishing step is controlled by means of an end point detection mechanism. The thickness deviation of the wafers entering the third polishing step using a fixed-abrasive pad can be minimized. Hence, the problem of overpolishing or underpolishing that is often confronted in a FA polishing process can be obviated, while global uniformity is achieved. According to the multi-step planarizing and polishing method of the present invention, improved throughput, good local planarity and global uniformity are achieved.

[0041] As previously discussed, the benefits provided by the multi-step planarizing and polishing method of the present invention can not be achieved by any combination or sequence of the polishing steps. For example, although a "typical" polishing step using, for example, silica abrasives may provide a high throughput, completing the multi-step polishing process with a "typical" polishing step will result in poor local and global uniformities. Further, even a HSS polishing step using CeO_2 abrasives may also provide a desirable oxide-to-nitride selectivity, a high removal rate deviation and a high removal rate drop suffered in a HSS polishing step render the HSS polishing step unsuitable for completing the multi-step polishing process. However, it has been demonstrated that CeO_2 abrasives can provide good with-in die uniformity, a high selectivity slurry comprising CeO_2 abrasives is adopted for the multi-step planarizing and polishing method. Further, because a polishing step using a FA pad gradually decelerates and results in a drop of the removal rate, FA polishing is not preferred as a first polishing step. Instead, since FA polishing can provide excellent global uniformity, completing the multi-step polishing process is preferable as long as the

wafer-to-wafer uniformity is well controlled before entering the FA polishing step. Accordingly, the present invention provides a multi-step planarizing and polishing method, wherein at least one of the last polishing steps of the multi-step polishing process is a FA polishing step to achieve the desired global uniformity. The FA polishing step is preceded by either a HSS polishing step to provide the within-die uniformity, followed by a "typical" polishing step using, for example, silica abrasives to enhance the overall throughput of the process or vice versa.

[0042] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing descriptions, it is intended that the present invention covers modifications and variations of this invention if they fall within the scope of the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A planarizing and polishing method comprising:

providing a substrate having a plurality of patterned features;

forming a material layer over the substrate and the patterned features;

planarizing the material layer with a first polishing slurry comprising at least silica abrasives;

planarizing the material layer with a second polishing slurry comprising at least CeO_2 (cerium oxide) abrasives;

continuing to a final planarization of the material layer with a fixed abrasive pad, wherein a remaining thickness of the material layer entering the final planarization of the material layer is controlled.

2. The method of claim 1, wherein the step of planarizing the material layer with the second polishing slurry is controlled by an end-point detection system.

3. The method of claim 1, wherein the step of planarizing the material layer with the first polishing slurry removes a bulk of the material layer.

4. The method of claim 1, wherein after the steps of planarizing the material layer with the first polishing slurry and the second polishing slurry, the remaining thickness of material layer is about 0 to 100Å.

5. The method of claim 1, wherein the step of planarizing the material layer with the second polishing slurry is performed before the step of planarizing the material

layer with the first polishing slurry.

6. The method of claim 5, wherein the step of planarizing the material layer with the first polishing slurry is controlled by an endpoint detection mechanism.

7. The method of claim 1, wherein the patterned features comprise trench isolation structures.

8. The method of claim 1, wherein the final planarization of the material layer with the fixed abrasive pad comprises a control of polishing time to avoid overpolishing.

9. A planarizing and polishing method comprising:

performing a first polishing step with a first slurry composition comprising at least silica abrasives;

performing a second polishing step with a second slurry composition comprising at least CeO_2 (Cerium Oxide) abrasives, wherein the second polishing step is controlled by an end-point detection mechanism; and

performing a third polishing step with a fixed abrasive pad.

10. The method of claim 9, wherein the first polishing step is performed using a "standard" pad without embedded abrasive particles.

11. The method of claim 9, wherein the second polishing step is performed

using a "standard" pad without embedded abrasive particles.

12. The method of claim 9, wherein the third polishing step is performed without slurry.

13. A planarizing and polishing method comprising:

performing a first polishing step with a first slurry composition comprising at least CeO_2 abrasives;

performing a second polishing step with a second slurry composition comprising at least silica abrasives, wherein the second polishing step is terminated by an end-point detection mechanism; and

performing a third polishing step with a fixed abrasive pad.

14. The method of claim 13, wherein the first polishing step is performed using a "standard" pad with without embedded abrasive particles.

15. The method of claim 13, wherein the second polishing step is performed using a "standard" pad without embedded abrasive particles.

16. The method of claim 13, wherein the third polishing step is performed without slurry.

17. A multi-step planarizing and polishing method comprising:

providing a structure having a nonplanar surface topography;

performing at least two polishing steps with two different slurry compositions, wherein a removal rate of one of the two polishing steps is higher than that of the other polishing step;

controlling a remaining thickness of the structure at an end of the two polishing steps; and

performing a final polishing step with a fixed abrasive pad.

18. The method of claim 17, wherein one of the two slurry compositions comprises at least CeO_2 abrasives.

19. The method of claim 17, wherein one of the two slurry compositions comprises at least silica abrasives.

20. The method of claim 17, wherein the two polishing steps use different polishing pads.

21. The method of claim 17, wherein the two polishing steps use a same polishing pad.

22. The method of claim 17, wherein the two polishing steps use a "standard" pad without embedded abrasive particles.

23. The method of claim 17, wherein at least one of the two polishing steps is controlled by an end-point detection method to control the remaining thickness of the

structure.