



(51) International Patent Classification:

G06F 11/22 (2006.01) G06F 9/44 (2006.01)
G06F 19/00 (2011.01)

(21) International Application Number:

PCT/US2011/035212

(22) International Filing Date:

4 May 2011 (04.05.2011)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

61/331,418 5 May 2010 (05.05.2010) US

(71) Applicant (for all designated States except US): **TERADYNE, INC.** [US/US]; 600 Riverpark Drive, North Reading, MA 01864 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **VAN WAGENEN, Bethany** [US/US]; 21 Oak Street, #2, Somerville, MA 02143 (US). **EDWARD, Seng, J.** [US/US]; 5 Apple Blossom Road, Andover, MA 01810 (US).

(74) Agent: **WALSH, Edmund, J.**; Wolf, Greenfield & Sacks, P.C., 600 Atlantic Avenue, Boston, MA 02210-2206 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

[Continued on next page]

(54) Title: SYSTEM FOR CONCURRENT TEST OF SEMICONDUCTOR DEVICES

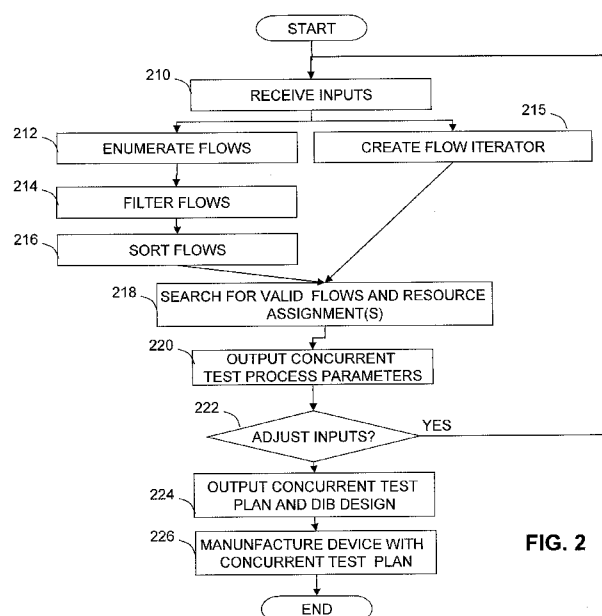


FIG. 2

(57) Abstract: A tool to aid a test engineer in creating a concurrent test plan. The tool may quickly map test system resources to specific pins to satisfy the requirements of a concurrent test. The tool may project test time when such a mapping is possible. When a mapping is not possible, the tool may inform its user, including making suggestions of additional resources that could allow the test system to perform the test or suggestions for other variations in input parameters that would allow a mapping. The tool employs an assignment process in which groups of associated pins are identified, along with associated resource requirements for each group. Groups of test system resources that collectively fulfill a higher level requirement are identified and the assignment is made by mapping resource sets to resource groups, using ordering and matching heuristics to reduce processing time.



(88) Date of publication of the international search report:
29 December 2011