

COLOUR ENCODER

The present invention relates to a colour encoder which is particularly suitable for use in a T.V. game system in which a motion picture pattern, which may be varied under the control of the operator, is combined with a still picture pattern which defines the background of the picture frame to be displayed.

The present application is divided out from copending U.K. patent application No. 83.33979 (2133257A) which describes and claims an image processing system for combining a motion picture pattern and a still picture pattern.

The present invention provides a color encoder comprising a color generator for generating a color code signal, said color generator having a predetermined number of color code signals and generating as an output one of said predetermined number of color code signals in response to a color selection signal supplied thereto, each color code signal containing a phase selection code comprising a first predetermined number of bits and a level selection code comprising a second predetermined number of bits, means for producing a predetermined

number of phase difference signals, each having a different relative, and each being phase associated with one of said phase selection codes, in response to a reference signal, first selecting means for selecting one of said predetermined number of phase difference signals in response to the phase selection code of said color code signal generated by said color generator, second selecting means for selecting a level of said phase difference signal selected by said first selecting means in response to the level selection code of said color code signal generated by said color generator, and output means associated with said first and second selecting means for outputting a color signal corresponding to the phase difference signal selected by said first selecting means, and oscillating with a predetermined amplitude with said level selected by said second selecting means as a reference.

A colour encoder in accordance with the invention will now be described with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram showing a T.V. game system;

Figs. 2a and 2b are schematic illustrations showing examples of displaying the background on the T.V. screen;

Fig. 3 is a block diagram showing the



detailed structure of the system shown in Fig. 1;

Fig. 4 is a schematic illustration showing the memory map of the motion picture attribute table memory 12-2 shown in Fig. 3;

Fig. 5 is a circuit diagram partly in logic symbols showing the detailed structure of the multiplexer 30 shown in Fig. 3;

Fig. 6 is a block diagram showing the detailed structure of the colour generator 35 shown in Fig. 3;

Fig. 7 is a schematic illustration showing colour signals at different levels which may be produced as outputs from the colour encoder of Fig. 6; and

Fig. 8 is a block diagram showing another embodiment in which two picture processing units (PPU) are provided as connected to each other.

Fig. 1 is a block diagram showing an image processing system as applied to a T.V. game system. As shown, the image processing system or T.V. game system includes a picture processing unit ("PPU") 11 provided with a motion picture attribute table memory 12-2 which is typically comprised of a RAM and which is rewritten for each frame with the information supplied from the video memory. PPU 11 also includes a temporary memory 15 which is also typically comprised of a RAM. The temporary memory 15 stores the motion picture character data for a single scanning line by accessing the motion picture attribute table memory 12-2 and it is rewritten for each scanning line. Also provided in PPU 11 is a motion picture buffer memory 16 which is typically comprised of a RAM whose contents are rewritten for each scanning line and which stores the

attributes and pattern data of the motion picture character stored in the temporary memory 15. PPU 11 further includes a synthesizer 17 which is connected to receive an output signal from the motion picture buffer memory 16 and an output signal from a still picture character pattern generator 12-3 or an output signal supplied from an external circuit, as the case may be, to supply a particular signal, which is a combination of two or more input signals, as its output in accordance with predetermined conditions.

A video memory 12 is provided external to PPU 11 and it includes a motion picture character pattern generator 12-1, a still picture character pattern generator 12-3 typically comprised of a ROM or RAM, four still picture character pattern name tables 12-41 through 12-44 typically comprised of RAMs and four still picture color tables 12-51 through 12-54 typically comprised of RAMs. As shown in Fig. 1, PPU 11 is also connected to CPU 3 which controls the overall operation of the present system and which is connected to a main memory 4.

In operation, when a main switch (not shown) is turned on or programs containing different games are changed, the contents of the still picture character pattern name tables 12-41 through 12-44 and still picture color tables 12-51 through 12-54 are rewritten in accordance with the main memory 4 under the control of

CPU 3. Then, at the first vertical blanking period of a single frame, the contents of the motion picture attribute table memory 12-2 are also rewritten in accordance with the main memory 4 under the control of CPU 3.

In PPU 11, during line scanning, the motion picture character pattern to be displayed in the next scanning line is retrieved from the motion picture attribute table memory 12-2 and stored into the temporary memory 15, and, then, during the horizontal blanking period, the motion picture character pattern generator 12-1 is retrieved on the basis of the data then stored in the temporary memory 15 via address and data buses, thereby causing the data necessary to display a motion picture character for the next line to be stored into the motion picture buffer memory 16. After initiation of line scanning, when the corresponding horizontal position has been reached, the motion picture character pattern data is supplied to the synthesizer 17 from the motion picture buffer memory 16, and at the same time the still picture character pattern name tables 12-41 through 12-44 and the color tables 12-51 through 12-54 are retrieved in real time via address and data buses so that the still picture character pattern data thus retrieved and defining the background of a displayed picture is

supplied from the still picture character pattern generator 12-3 to the synthesizer 17.

5 In the system illustrated in Fig. 1, the still picture character pattern name tables 12-41 through 12-44 and the still picture color tables 12-51 through 12-54 are larger in area by four times than the display area or screen. Accordingly, a desired still picture may be displayed on the display screen by using only one of the four still picture character pattern name tables, or, 10 alternatively, the display area may be set at any location within the scope of four frames to define a desired background to be displayed on the screen as shown in Figs. 2a and 2b. The display area may be shifted horizontally as well as vertically independently from each other in a scrolling fashion with a dot as a unit. 15 Such a scrolling technique is disclosed, for example, in the Japanese Patent Laid-open Pub. No. 55-96186.

It is to be noted that in the video memory 12 the motion picture character pattern generator 12-1 and 20 the still picture character pattern generator 12-3 may not only be used separately from each other as described above but also be used in common. That is, the same character pattern generator may be accessed by an address for motion picture and another address for still picture 25 thereby producing both of motion picture and still picture characters from the same character pattern

generator. Such a structure is advantageous because an increased number of characters may be generated using a character pattern generator of the same capacity as compared with the case in which a character pattern generator is not used in common.

An assumption is made here that the display area or screen has the width of 256 dots in the horizontal direction and the height of 240 dots in the vertical direction and a character constituting a motion picture or still picture is defined by a matrix of 8 dots by 8 dots. It is also assumed that the max. number of motion pictures to be displayed on a single horizontal line is eight and thus 64 motion pictures may be displayed on the screen at maximum at the same time. Furthermore, in the motion picture character pattern generator 12-1 and the still picture character pattern generator 12-3, a single dot or picture element to be displayed on the screen is represented by two bits and thus a single character formed by 8 dots by 8 dots is represented by 16 bytes.

Fig. 3 shows the detailed structure of PPU 11 shown in Fig. 1. Now, it will first be described as to the structure for displaying a motion picture character pattern. The motion picture attribute table memory 12-2 for storing the attributes of motion picture characters for a single frame has a capacity to store sixty-four

motion picture characters as shown in Fig. 4 and it has areas for storing a vertical position (8 bits), a character number (8 bits), an attribute (5 bits) and a horizontal position (8 bits) for each character to be displayed. The attribute data includes 1 bit for each of horizontal and vertical inversions, 1 bit for determining the priority between motion and still picture characters and 2 bits for color display.

Storage of data from CPU 3 into the motion picture attribute table 12-2 is carried out via input terminals D_{0-7} and its storage position is determined by a motion picture attribute memory address register 18. While the previous line is being scanned, the retrieval of the motion picture character to be displayed on the next following line is carried out by a comparator 20 using a vertical position data. At the comparator 20, the signal indicating the vertical position of the next line to be displayed is compared with the vertical position data of each character stored in the motion picture attribute table memory 12-2 to determine whether they agree (in-range) or not. The motion picture character which has been found to be in-range is then stored into the temporary memory 15 by means of a temporary memory register 19. The temporary memory 15 is provided with an area capable of storing eight motion picture characters at the same time. Accordingly, if

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nine or more motion picture characters have been found to be in-range, only eight of them are stored into the temporary memory 15 with a flag indicating the presence of nine or more being posted.

5 The motion picture buffer memory 16 whose contents are rewritten during the horizontal blanking period also has the memory area capable of storing eight motion picture characters to be displayed on the next line, and, in the buffer memory 16, for each motion
10 picture character, a horizontal position area (8 bits) 16-1, an attribute area (3 bits) 16-2 and a pair of shift registers (8 bits) 16-3 are allocated. The horizontal position area 16-1 stores a horizontal position data supplied from the temporary memory 15, and
15 this area is structured in the form of a down-counter which down-counts in accordance with the scanning along a horizontal scanning line, and when the count has reached "0", the motion picture character is supplied as its output. The attribute area 16-2 stores a bit for
20 determining the priority and two bits of color data and thus three bits in total among the attribute data stored in the temporary memory 15. Each of the shift registers 16-3 stores 8-bit data supplied as an output from the motion picture character pattern generator 12-1 in
25 accordance with the character number of motion picture character in the temporary memory 15. The reason why a



pair of shift registers 16-3 are provided in parallel is that a picture element is represented by two bits.

In Fig. 3 there is also provided a picture address register 21 which retrieves the character pattern generator 12-1 or 12-3 from terminals AD_{0-7} through buses by means of motion picture character data, which has been found to be in-range, during the horizontal blanking period and of still picture character data during the line scanning period and calls or obtains corresponding character pattern data. In the case where a vertical inversion data is contained in the motion picture character data, the retrieving operation is carried out with the vertical address inverted within the motion picture character pattern in accordance with a signal supplied from an inverter 22. There is also provided a horizontal inverter 23 which functions to supply the retrieved motion picture character pattern data with the order of transmission reversed to the shift register 16-3 of motion picture buffer memory 16 if a horizontal inversion signal is contained in the motion picture character data.

Next, a description will be made as to the structure for displaying a still picture (background) character pattern. As line scanning proceeds, still picture character pattern data of the corresponding position is supplied through the terminals AD_{0-7} in

accordance with a signal from the picture address register 21. This character pattern data is comprised of a two bit data for character pattern and another two bit data for color display for a single dot on the display screen, so that the character pattern data and color display data are inputted to the shift registers 24-1, 24-2 and a selector 25, respectively, which are then inputted to selectors 28-1, 28-2 and 29 in the form of 8, 8 and 16 bits through shift registers 26-1, 26-2 and 27, respectively. In the case where no scrolling operation is to take place, these data are then outputted to a multiplexer 30 in the order mentioned without change.

The structure of Fig. 3 also includes a register 31 which has a dual function as a horizontal scroll register (SCCH) and as a video memory address register (VRAM.ARL) for counting the lower address of video memory and another register 32 having a dual function as a vertical scroll register (SCCV) and as a video memory address register (VRAM.ARH) for counting the upper address of video memory. In the scroll registers 31 and 32 are set offset values (scrolling initiation position) at the time of scrolling in the order of that in the horizontal direction and that in the vertical direction, and the selection of selectors 28-1, 28-2 and 29 is carried out in accordance with these offset values. On the other hand, when used as video

memory address registers 31 and 32, upon completion of read out/write in operation of video memory 12, values of 1 and 32 are respectively added automatically. Also provided as connected to the registers 31 and 32 are horizontal and vertical counters 33 and 34, respectively.

The multiplexer 30 constitutes part of the synthesizer 17 shown in Fig. 1 and it receives motion picture character pattern data and still picture character pattern data and moreover another motion picture character pattern data and still picture character pattern data from terminals EXT_{0-3} , as the case may be. The multiplexer 30 then supplies its output signal to a color generator 35 in accordance with the priority order determined by the attribute data within the motion picture character pattern data. If desired, the multiplexer 30 may so function to supply its output signal to the exterior through the terminals EXT_{0-3} . In the case where a collision occurs between a particular motion picture character pattern data and a still picture character pattern data in the multiplexer 30, a flag (STK.F) for that effect is raised.

The color generator 35 is typically comprised of a RAM and it is accessed by a 6-bit code comprised of a 2-bit code designating one of four levels and a 4-bit code designating one of 12 kinds of phases (hue), so that selection is made by a 4-bit data representing a

character pattern data supplied as an output from the multiplexer 30. A decoder 36 is provided as connected to receive an output signal from the color generator 35 as its input thereby converting it into a level selection
5 signal and a phase selection signal. Also provided as connected to receive an output signal from the decoder as its input is a digital-to-analog converter (DAC) 37 which serves to have its input converted into and supplies as its output an analog video signal. A phase
10 shifter 38 is provided as connected to the decoder 36.

It is to be understood that the synthesizer 17 of Fig. 1 is constructed by those elements of multiplexer 30, color generator 35, decoder 36, DAC 37 and phase shifter 38. Also provided are control registers 39 and
15 40 for determining the operating mode of PPU 11 and they receive data from CPU 3 via a counter 41.

Fig. 5 shows in detail the structure of multiplexer 30. As shown, the multiplexer 30 includes a transmission gate 50 for transmitting a 4-bit still
20 picture character pattern data (BG0-BG3) and it includes four MOS transistors 50-1 through 50-4 each corresponding to each bit. Also provided is another transmission gate 51 for transmitting a 4-bit portion (OBJ0-OBJ3) among a 5-bit motion picture character
25 pattern and it is provided with four MOS transistors 51-1 through 51-4 one for each bit. Provided in the

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5 multiplexer 30 is a priority determining circuit 52 for
determining to transmit either one of the still picture
character pattern data BG0-BG3 forming a background of
displayed picture and the motion picture character
pattern data OBJ0-OBJ3 and it is so structured that a NOR
circuit 53 receives OBJ0 and OBJ1 as its two inputs and
an OR circuit 54 receives BG0 and BG1 as its two inputs.
Data OBJ4 which determines the priority order and an
output from the OR circuit 54 are supplied as two inputs
10 to an AND circuit 55 whose output is supplied as one
input to another OR circuit 56 which also receives as its
the other input an output from the NOR circuit 53. The
OR circuit 56 is connected to supply its output to the
gate of each of the MOS transistors 50-1 through 50-4 and
15 to supply its inverted output to the gates of MOS
transistors 51-1 through 51-4 via an inverter 57.

As a result, depending upon a combination of
BG0, BG1, OBJ0, OBJ1 and OBJ4, either one of the
transmission gates 50 and 51 is turned on, so that
20 BG0-BG3 or OBJ0-OBJ3 and the output signal from the
inverter 57 indicating the result of the priority order
determination are transferred through inverters 61-1
through 61-4 and 62-1 through 62-5 via transmission gate
transistors 59-1 through 59-5, which are turned on and
25 off in accordance with a clock signal ϕ .

Turn-over circuits 64-1 through 64-4 are also provided and they are appropriately activated by a slave signal $\overline{SLAVE}$ to thereby cause the terminals EXT0-EXT3 to function either as input or output terminals when two PPU's are connected to each other. The turn-over circuit 64-1 includes a driver circuit 65 which receives as its input either of data BG0 or OBJ0 and which also receives the $\overline{SLAVE}$ signal for controlling the passage of data therethrough. Moreover, in order to control data input via the terminal EXT0, the turn-over circuit 64-1 includes a NAND circuit 66 which has one input connected to receive the data supplied via the terminal EXT0 through an inverter 67 and the remaining input connected to receive the $\overline{SLAVE}$ signal via another inverter 68. The other turn-over circuits 64-2 through 64-4 are similarly structured.

Also provided is a master/slave priority order determining circuit 80 which causes a transmission gate 81 or 82 to be turned on in accordance with the $\overline{SLAVE}$ signal and input signals from BG0, BG1 (or OBJ0, OBJ1) and EXT0, EXT1 terminals, thereby determining to transfer the data from either one of the master and slave PPU's. BG0 and BG1 (or OBJ0 and OBJ1) are supplied as inputs to an OR circuit 85 and the data supplied through the EXT0 and EXT1 terminals are inputted to a NOR circuit 86. The circuit 80 includes another OR circuit 87 which

has its one input connected to receive an output signal from the OR circuit 85 and the remaining input connected to receive an output signal from the NOR circuit 86 and the OR circuit 87 is connected to supply its output signal to the gate of each of MOS transistors provided in a transmission gate 81 and to supply its inverted output signal to the gate of each of MOS transistors in another transmission gate 82 via an inverter 88.

The data transferred through the transmission gate 81 or 82 then passes through inverters 96-1 through 96-4 and transmission gate MOS transistors 94-1 through 94-4 which are controlled by a clock signal $\bar{\phi}$ and inverters 97-1 through 97-4 to be supplied as address signals CGA0-CGA3 for addressing the color generator 35 shown in Fig. 3. As a signal CGA4 which indicates whether CGA0-CGA3 are either BG0-BG3 or OBJ0-OBJ3, an output signal supplied from the priority determining circuit 52 is used after having been inverted by an inverter 94-5.

There is also provided an AND circuit 100 which functions to raise a collision flag (STK.F) when a collision has occurred between BG0-BG3 and OBJ0-OBJ3.

The operation of priority order determining circuit 52 of the multiplexer 30 shown in Fig. 5 may be summarized in the following table.

	OBJ0+OBJ1	BG0+BG1	OBJ4	Data transferred thru gate 50 or 51
	0	0	0	BG
	0	1	0	BG
	1	0	0	OBJ
	1	1	0	OBJ
5	0	0	1	BG
	0	1	1	BG
	1	0	1	OBJ
	1	1	1	BG

Next, in the case where two PPUs are provided as connected to each other and the present PPU serves as a master, the $\overline{SLAVE}$ signal is "1". In the turn-over circuits 64-1 through 64-4, the NAND circuit 66 receives at its one input "0" through the inverter 68, so that the NAND circuit 66 is enabled thereby allowing data to be inputted through the terminals EXT0-EXT3. On the other hand, the driver circuit 65 is disabled since the $\overline{SLAVE}$ signal is "1", thereby inhibiting data to be outputted. Conversely, in the case where the present PPU serves as a slave, the $\overline{SLAVE}$ signal is "0" so that the NAND circuit 66 becomes disabled and the driver circuit 65 becomes enabled, thereby setting up the condition in which data may be outputted through terminals EXT0-EXT3.

Now, the operation of the master/slave priority order determining circuit 80 may be summarized as in the following table.

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BG0+BG1 (OBJ0+OBJ1)	EXT0+EXT1	SLAVE	Data transferred thru gate 81 or 82
0		0	internal data
0		0	internal data
1		0	internal data
1		0	internal data
5			
0	0	1	internal data
0	1	1	EXT data
1	0	1	internal data
1	1	1	internal data

Now, the color generator 35, decoder 36, DAC 37 and phase shifter 38 will be described in detail with particular reference to Fig. 6.

The color generator 35 is comprised of a RAM and capable of storing thirty-two 6-bit color codes, one of which is supplied as its output after having been selected by a 5-bit address signal CGA0-CGA4 supplied from the multiplexer 30. The color code signals stored in the color generator 35 may be rewritten under the control of a CPU 112.

Provided in the structure of Fig. 6 is a phase shifter 38 which divides six times ($3.58 \text{ MHz} \times 6$) of the frequency of chrominance subcarrier (Sc) and produces twelve kinds of phase difference pulses different in phase from each other. Provided as connected to receive an output signal from the phase shifter 38 is a phase selector 114 which receives a 4-bit data among a 6-bit color code signal supplied from the color code generator 35 thereby selectively outputting

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one of the twelve kinds of phase difference pulses
different in phase supplied from the phase shifter 38.
There is also provided a level decoder 115 which receives
a 2-bit data among a 6-bit color code signal supplied
5 from the color generator 35 and converts it into a level
selection signal having four different levels. It is to
be noted that the decoder 36 of Fig. 3 includes the phase
shifter 114 and the level decoder 115.

Also provided as shown in Fig. 6 is a resistor
10 ladder 116 which includes nine resistors 117-1 through
117-9 connected in series between a supply voltage V_{CC}
and ground (GND). From each of the nodes between the
adjacent resistors, an output signal having a voltage
level divided proportionately may be obtained through the
15 corresponding one of MOS transistors 118-1 through 118-8
which together form a transmission gate. Gate circuits
119-1 and 119-4 are provided as appropriately connected
to control two of the transistors 118-1 through 118-8 at
the same time. Each of the gate circuits 119-1 through
20 119-4 includes two NAND circuits 120 and 121, each of
which has its one input connected to receive the same
level selection signal supplied from the level decoder
115. Furthermore, in each of the gate circuits 119-1
through 119-4, one 120 of the pair of NAND circuits has
25 the other input commonly connected to receive the same
phase difference pulses having a desired phase

supplied from the phase selector 114; whereas, the other NAND circuit 121 has its the other input connected to receive an output signal of the one NAND circuit 120. Each of the NAND circuits 120 and 121 has its output
5 connected to the gate of corresponding one of MOS transistors 118-1 through 118-8. It is to be noted that the DAC 37 of Fig. 3 includes the resistor ladder 116, transistors 118-1 through 118-8 and gate circuits 119-1 through 119-4.

10 The operation of the structure shown in Fig. 6 will now be described with particular reference to Fig. 7. When a single data is outputted from the multiplexer 30, there is outputted a single color code signal (6 bits) from the color generator 35. The phase selector
15 114 then receives only four bits among the thus supplied color code signal thereby selecting one out of twelve kinds of phase difference pulses different in phase one from another to be supplied to all of the gate circuits 119-1 through 119-4. On the other hand, the level
20 decoder 115 receives a 2-bit data from the same color code signal to supply a level selection signal to one of the gate circuits 119-1 through 119-4.

Now, suppose that, for example, the gate circuit 119-1 is selected by the level decoder 115, then
25 a low level signal is applied to one input of each of the NAND circuits 120 and 121 in the gate circuit 119-1 and a

high level signal is applied to one input of each of the NAND circuits 120 and 121 in each of the remaining gate circuits 119-2 through 119-4. Under the condition, if the phase difference pulse from the phase selector 114 is a low level signal, in the gate circuit 119-1, the NAND circuit 120 supplies a high level output signal and the NAND circuit 121 supplies a low level output signal, so that the transistor 118-1 connected to the node of the resistor ladder at voltage V_1 is turned on and the transistor 118-2 connected to the node at voltage V_2 is turned off. On the other hand, if the phase difference pulse is a high level signal, then the NAND circuits 120 and 121 of gate circuit 119-1 supply low and high level signals, respectively, and, thus, the transistor 118-1, connected to the node at voltage V_1 is turned off and the transistor 118-2 connected to the node at voltage V_2 is turned on. Under the circumstances, the outputs from all of the other gate circuits 119-2 through 119-4 are at low level, and, thus, the transistors 118-3 and 118-8 are all maintained off.

As a result, an output signal obtained from the output terminal 22 under the condition is a color signal which is defined by a phase difference pulse having an intended phase and an amplitude which varies between two voltage levels V_1 and V_2 in an oscillatory manner, as indicated by a signal A in Fig. 7, whereby the center of

amplitude indicates luminance or degree of brightness. In this color signal, the amplitude indicates chroma and the phase indicates hue.

When another level is selected by the decoder 115 in accordance with another output signal from the multiplexer 30, for example when the gate 119-2 is selected, there is outputted a color signal having an amplitude which varies between two voltage levels V_3 and V_4 as shown by a signal B in Fig. 7. Similarly, color signals for other color code levels are shown by signals C and D in Fig. 7.

If another phase difference pulse having a different phase had been selected in accordance with a 4-bit code for phase selection in the color code signal supplied from the color generator 35, another color signal having a different phase (hue) with one of the signals A through D in Fig. 7 having particular amplitudes (chroma) and voltage levels (luminance) is outputted. A color signal thus supplied as an output is then added with a burst signal and a sync signal to be formed into a color video signal which may be supplied to any of conventional T.V. sets (not shown) for display on the screen.

Since each of the twelve different kinds of phase difference pulses can take four different levels (amplitudes and voltage levels) in the present

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embodiment, color may be produced in 48 different representations. However, since the output signal from the multiplexer 30 has a 5-bit structure, color may be produced in 32 different representations at a time. In
5 view of this, provision is made of the color generator 11 capable of storing thirty-two 6-bit color codes in the present embodiment so that although only thirty-two kinds may be selected by the color data generator 10, color may be represented in forty-eight different ways at maximum
10 with a 6-bit color code signal by rewriting the contents of the color generator 35 by CPU 112. Thus, the maximum number of different color representations in the present embodiment is 48, and four of the remaining codes may be allocated to white, gray (2) and black.

15 Fig. 8 shows another embodiment of the present invention in which two PPUs 11-1 and 11-2 are coupled together to synthesize the character patterns in these PPUs 11-1 and 11-2. Let us assume that use is made of the $\overline{SLAVE}$ signal and PPUs 11-1 and 11-2 function as a
20 master and a slave, respectively. With PPUs 11-1 and 11-2 interconnected as shown in Fig. 8, a square wave having sharp rising and falling edges is applied to a clock terminal CLK and a reset signal is employed for initial synchronization between the two PPUs 11-1 and
25 11-2. Under the condition, the character pattern data of slave PPU 11-2 is outputted from terminals EXT0-3 to be



inputted to the terminals EXT0-3 of master PPU 11-1, whereby synthesization of character pattern data takes place within the master PPU 11-1 with the determination of priority order as described with reference to Fig. 5.

With the structure shown in Fig. 8, as a video output signal, any of possible combinations between still or motion picture character pattern in master PPU 11-1 and still or motion picture character pattern in slave PPU 11-2 may be obtained and displayed on the screen.

CLAIMS

1. A color encoder comprising a color generator for generating a color code signal, said color generator having a predetermined number of color code signals and generating as an output one of said predetermined number of color code signals in response to a color selection signal supplied thereto, each color code signal containing a phase selection code comprising a first predetermined number of bits and a level selection code comprising a second predetermined number of bits, means for producing a predetermined number of phase difference signals, each having a different ^{relative} phase ^{and each being} associated with one of said phase selection codes, in response to a reference signal, first selecting means for selecting one of said predetermined number of phase difference signals in response to the phase selection code of said color code signal generated by said color generator, second selecting means for selecting a level of said phase difference signal selected by said first selecting means in response to the level selection code of said color code signal generated by said color generator, and output means associated with said first and second selecting means for outputting a color signal corresponding to the phase difference signal selected

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by said first selecting means, and oscillating with a predetermined amplitude with said level selected by said second selecting means as a reference.

2. An encoder as claimed in claim 1, wherein said color generator comprises a random access memory.

3. An encoder as claimed in claim 2, further comprising a central processing unit connected to said color generator, whereby the contents of said predetermined number of color code signals may be altered by said central processing unit.

4. An encoder as claimed in claim 1, wherein said color selection signal comprises a third predetermined number of bits which is smaller in number than a sum of said first and second predetermined number of bits.

5. An encoder as claimed in claim 1, wherein said output means comprises a predetermined number of gate circuits each of which has a first input terminal connected to receive an output from said first selecting means, a second input terminal connected to receive an output from said second selecting means, and a pair of first and second output terminals, a



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voltage divider including a predetermined number of resistors connected in series between a pair of predetermined high and low voltages, and a plurality of MOS transistor switches each of which is connected between a corresponding one of junctions between said plurality of resistors and an output terminal of said encoder and has a gate connected to a corresponding one of said output terminals of said gate circuits.

6. An encoder as claimed in claim 5, wherein said first and second output terminals of one of said plurality of gate circuits are connected to the gates of two MOS transistor switches which are connected to two adjacent ones of said junctions.

7. An encoder as claimed in claim 6, wherein each of said gate circuits includes a pair of first and second NAND gates, said first NAND gate having a first input terminal connected to said first selecting means, a second input terminal connected to said second selecting means and an output terminal defining said first output terminal of said gate circuit, and said second NAND gate having a first input terminal connected to said output terminal of said first NAND gate, a second input terminal connected to said second selecting means and an

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output terminal defining said second output terminal of said gate circuit.

8. An encoder as claimed in any one of the preceding claims, further comprising means for adding a burst signal and a sync signal to said chrominance subcarrier signal output from said output means, thereby providing a composite color video signal.

9. An encoder as claimed in any one of the preceding claims, wherein said reference signal is a chrominance subcarrier contained in a television signal.

10. A color encoder substantially as herein described with reference to Figures 6 and 7 of the accompanying drawings.
