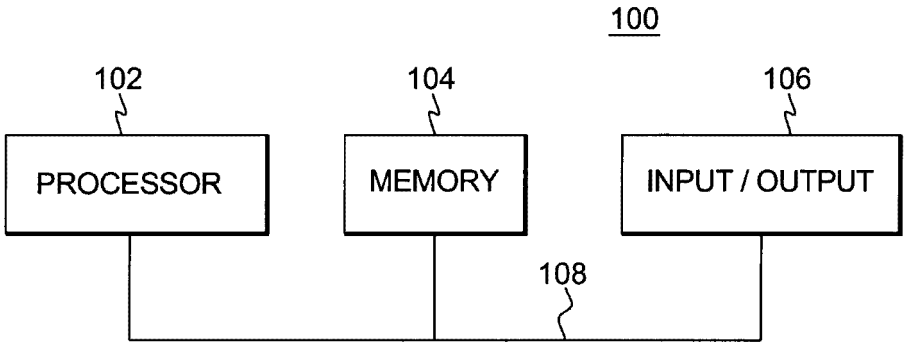

FIG. 1

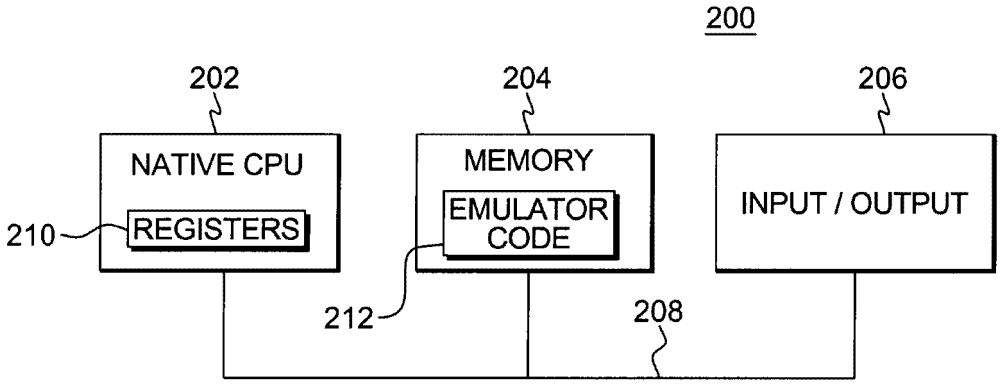

FIG. 2A

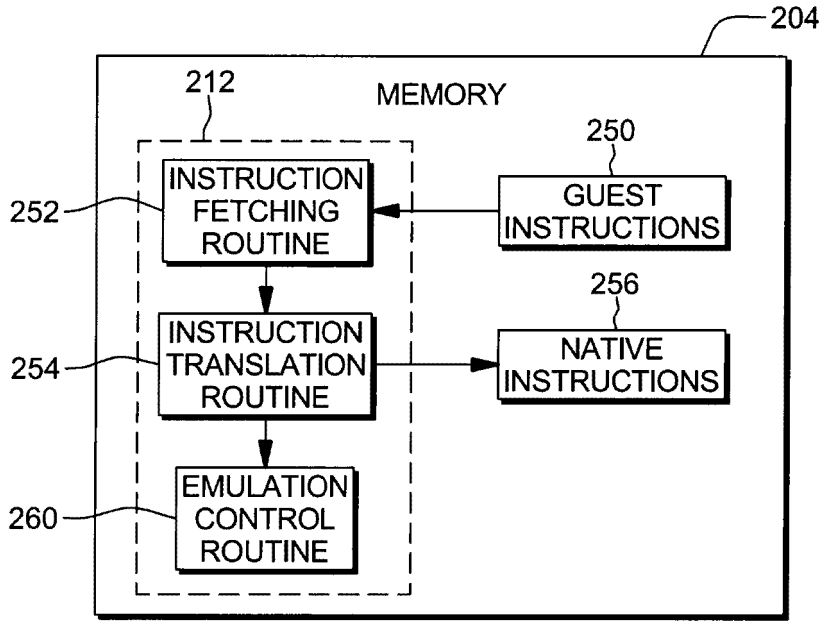

FIG. 2B

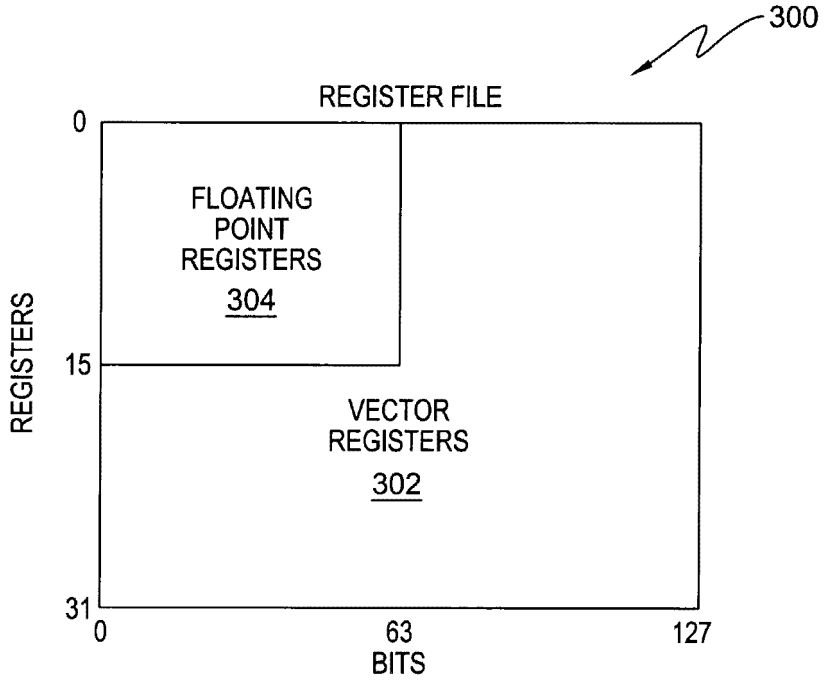

FIG. 3

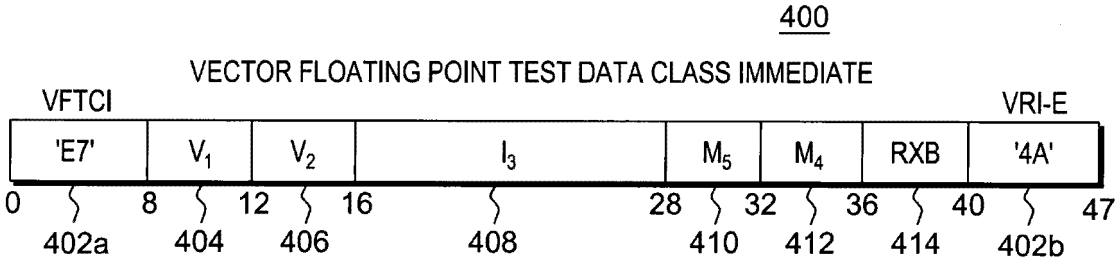

FIG. 4A

430 BFP ELEMENT CLASS	BIT USED WHEN SIGN IS 432	
	+	-
ZERO	0	1
NORMAL NUMBER	2	3
SUBNORMAL NUMBER	4	5
INFINITY	6	7
QUIET NAN	8	9
SIGNALING NAN	10	11

FIG. 4B

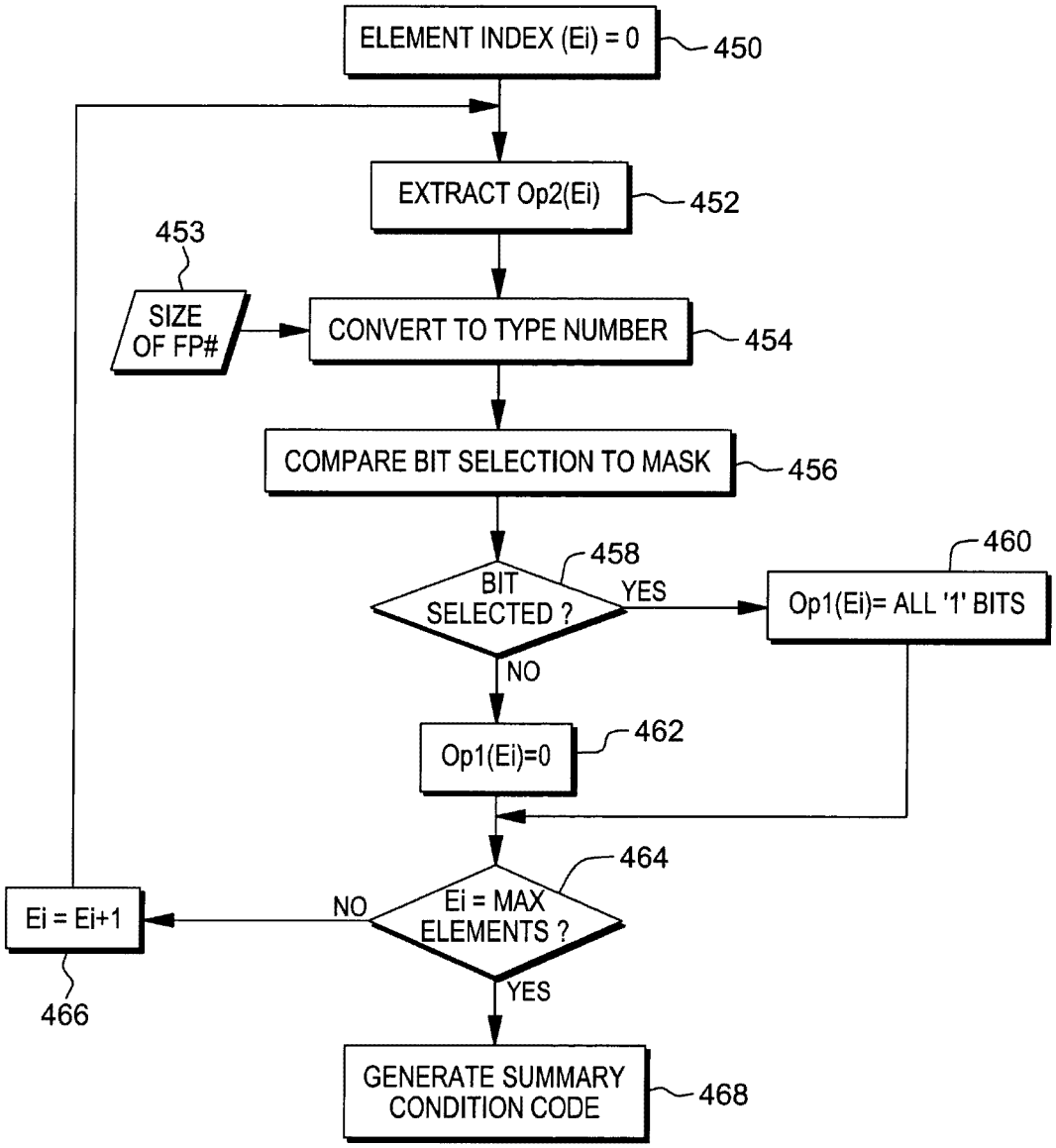
ELEMENT INDEX (Ei) = 0
450
EXTRACT Op2(Ei)
452
453
SIZE OF FP#
CONVERT TO TYPE NUMBER
454
COMPARE BIT SELECTION TO MASK
456
458
BIT SELECTED ?
YES
460
Op1(Ei)= ALL '1' BITS
NO
Op1(Ei)=0
462
464
Ei = MAX ELEMENTS ?
NO
Ei = Ei+1
466
YES
GENERATE SUMMARY CONDITION CODE
468

FIG. 4C

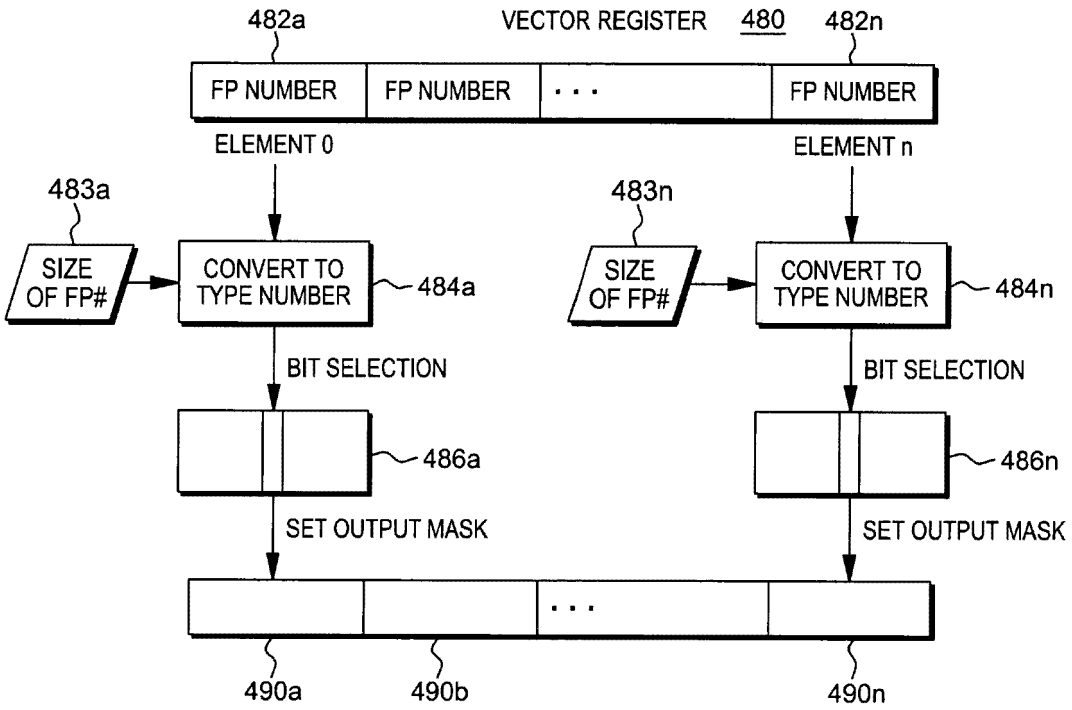

FIG. 4D

ENTITY	SIGN	BIASED EXPONENT	UNIT BIT *	FRACTION
TRUE ZERO	±	0	0	0
DENORMALIZED NUMBERS	±	0**	0	NOT 0
NORMALIZED NUMBERS	±	NOT 0, NOT ALL ONES	1	ANY
INFINITY	±	ALL ONES	-	0
QUIET NAN	±	ALL ONES	-	FO=1, Fr=ANY
SIGNALING NAN	±	ALL ONES	-	FO=0, Fr≠0

EXPLANATION:

* THE UNIT BIT IS IMPLIED

** THE BIASED EXPONENT IS TREATED ARITHMETICALLY AS IF IT HAD THE VALUE ONE

NAN NOT A NUMBER

FO LEFTMOST BIT OF FRACTION

Fr REMAINING BITS OF FRACTION

FIG. 4E

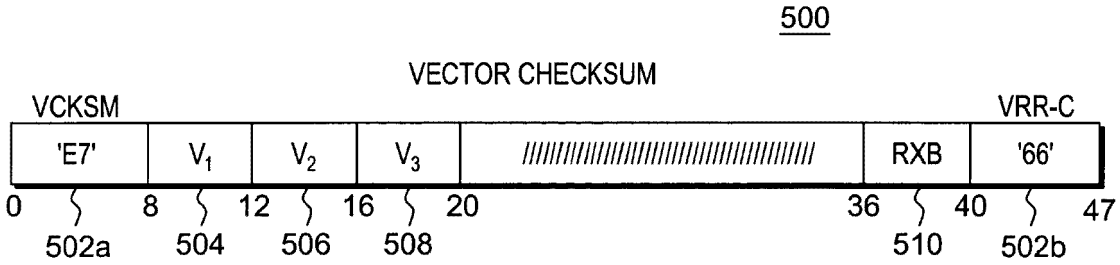
500
VECTOR CHECKSUM
VCKSM
VRR-C
'E7'
V1
V2
V3
RXB
'66'
0
8
12
16
20
36
40
47
502a
504
506
508
510
502b

FIG. 5A

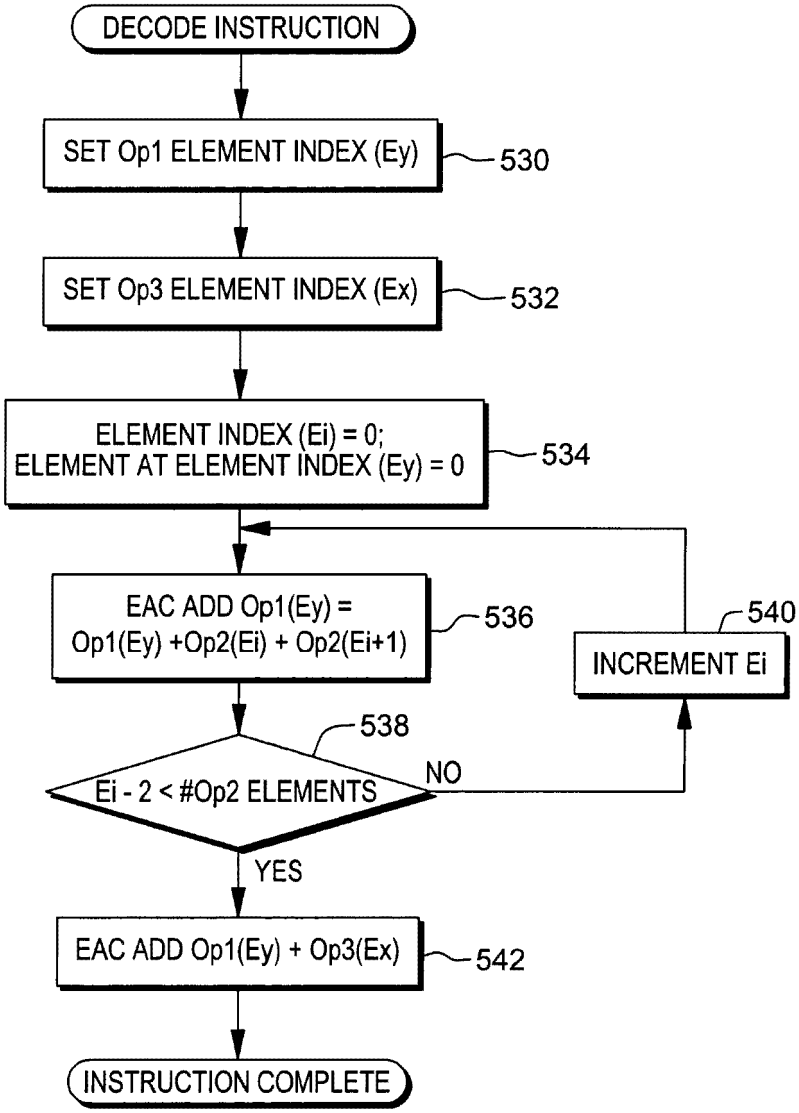
DECODE INSTRUCTION
SET Op1 ELEMENT INDEX (Ey)
530
SET Op3 ELEMENT INDEX (Ex)
532
ELEMENT INDEX (Ei) = 0;
ELEMENT AT ELEMENT INDEX (Ey) = 0
534
EAC ADD Op1(Ey) =
Op1(Ey) +Op2(Ei) + Op2(Ei+1)
536
INCREMENT Ei
540
538
Ei - 2 < #Op2 ELEMENTS
NO
YES
EAC ADD Op1(Ey) + Op3(Ex)
542
INSTRUCTION COMPLETE

FIG. 5B

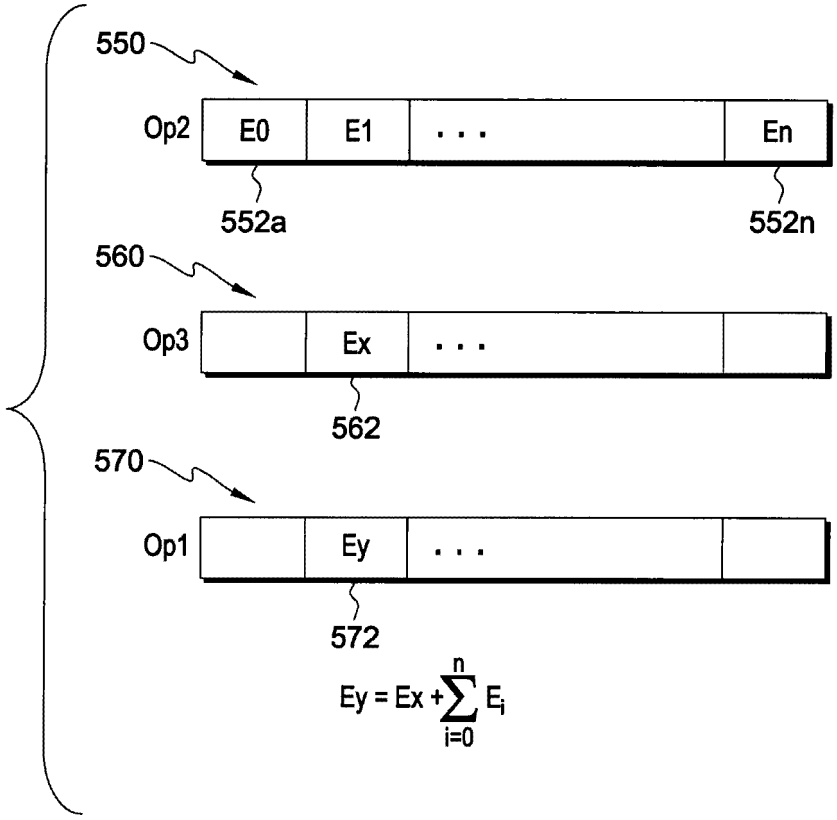
550
Op2
E0
E1
. . .
En
552a
552n
560
Op3
Ex
. . .
562
570
Op1
Ey
. . .
572
Ey = Ex + $\sum_{i=0}^{n} E_i$

FIG. 5C

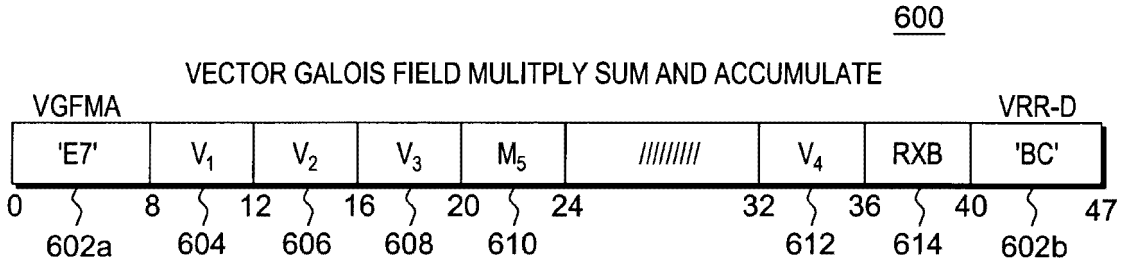
600
VECTOR GALOIS FIELD MULITPLY SUM AND ACCUMULATE
VGFMA
VRR-D
'E7'
V1
V2
V3
M5
////////
V4
RXB
'BC'
0
8
12
16
20
24
32
36
40
47
602a
604
606
608
610
612
614
602b

FIG. 6A

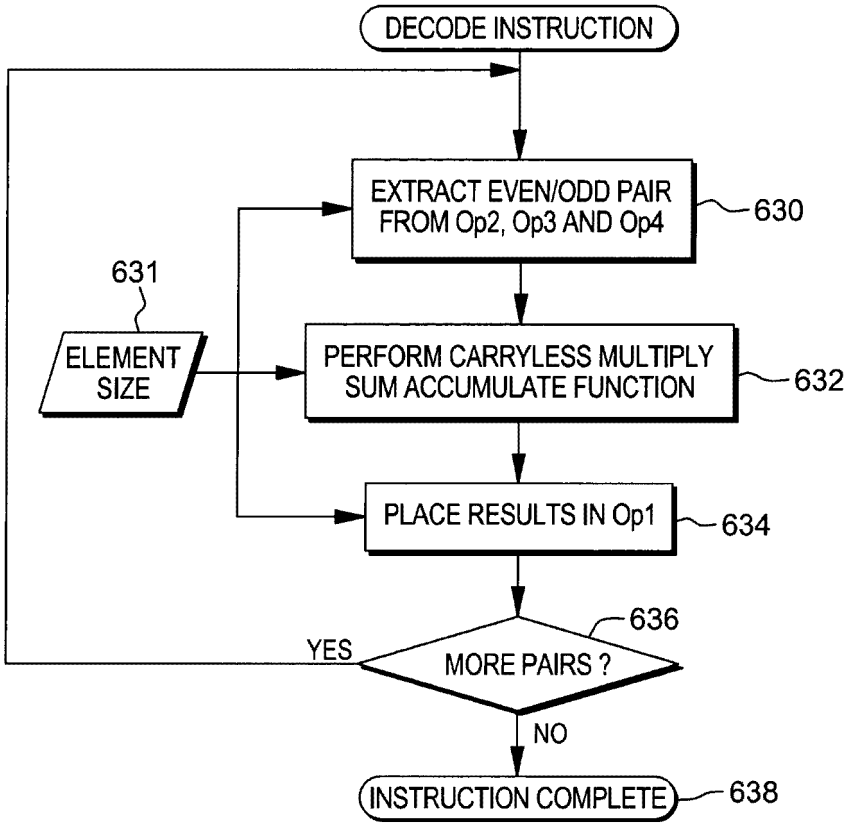
DECODE INSTRUCTION
EXTRACT EVEN/ODD PAIR FROM Op2, Op3 AND Op4
630
631
ELEMENT SIZE
PERFORM CARRYLESS MULTIPLY SUM ACCUMULATE FUNCTION
632
PLACE RESULTS IN Op1
634
636
YES
MORE PAIRS ?
NO
INSTRUCTION COMPLETE
638

FIG. 6B

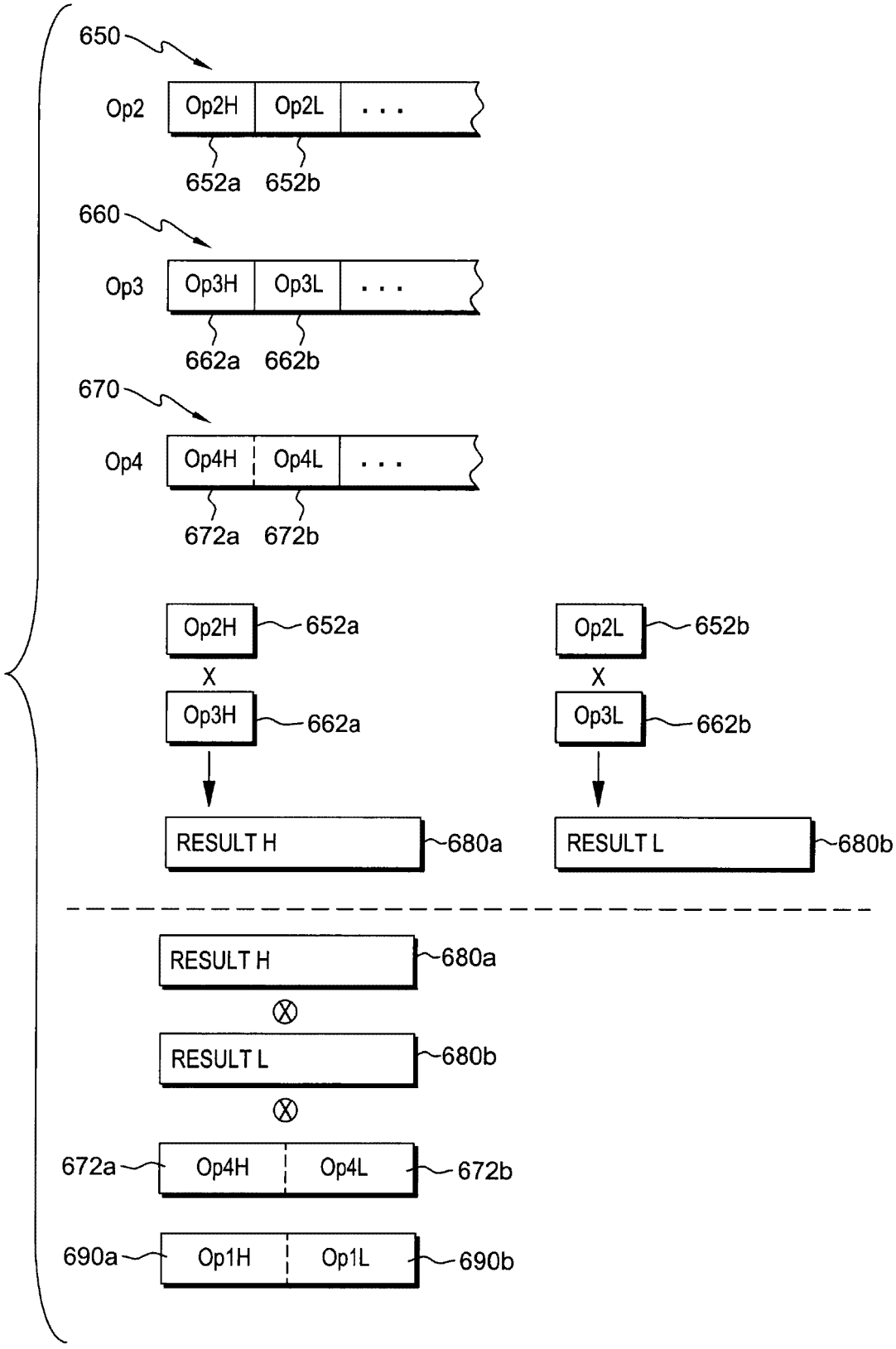
650
Op2
Op2H
Op2L
. . .
652a
652b
660
Op3
Op3H
Op3L
. . .
662a
662b
670
Op4
Op4H
Op4L
. . .
672a
672b
Op2H
652a
X
Op3H
662a
Op2L
652b
X
Op3L
662b
RESULT H
680a
RESULT L
680b
RESULT H
680a
RESULT L
680b
672a
Op4H
Op4L
672b
690a
Op1H
Op1L
690b

FIG. 6C

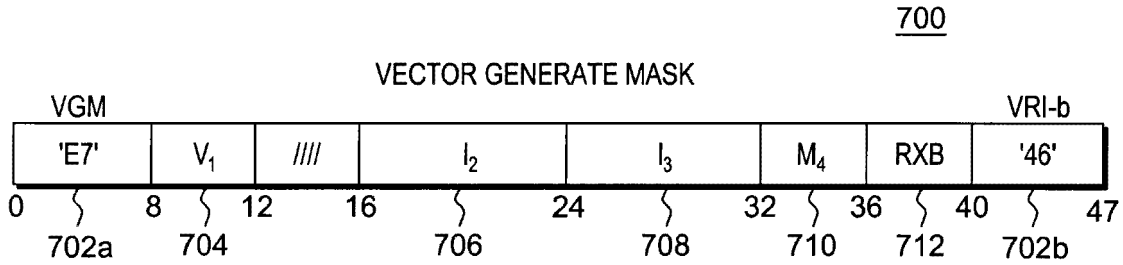
700
VECTOR GENERATE MASK
VGM
VRI-b
'E7'
V1
////
I2
I3
M4
RXB
'46'
0
8
12
16
24
32
36
40
47
702a
704
706
708
710
712
702b

FIG. 7A

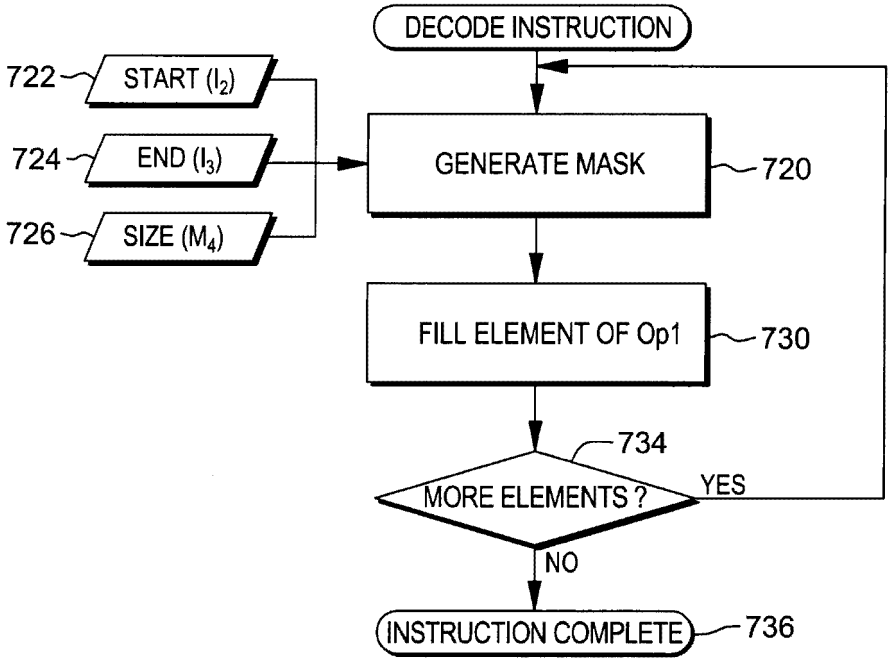
DECODE INSTRUCTION
722
START (I2)
724
END (I3)
726
SIZE (M4)
GENERATE MASK
720
FILL ELEMENT OF Op1
730
734
MORE ELEMENTS ?
YES
NO
INSTRUCTION COMPLETE
736

FIG. 7B

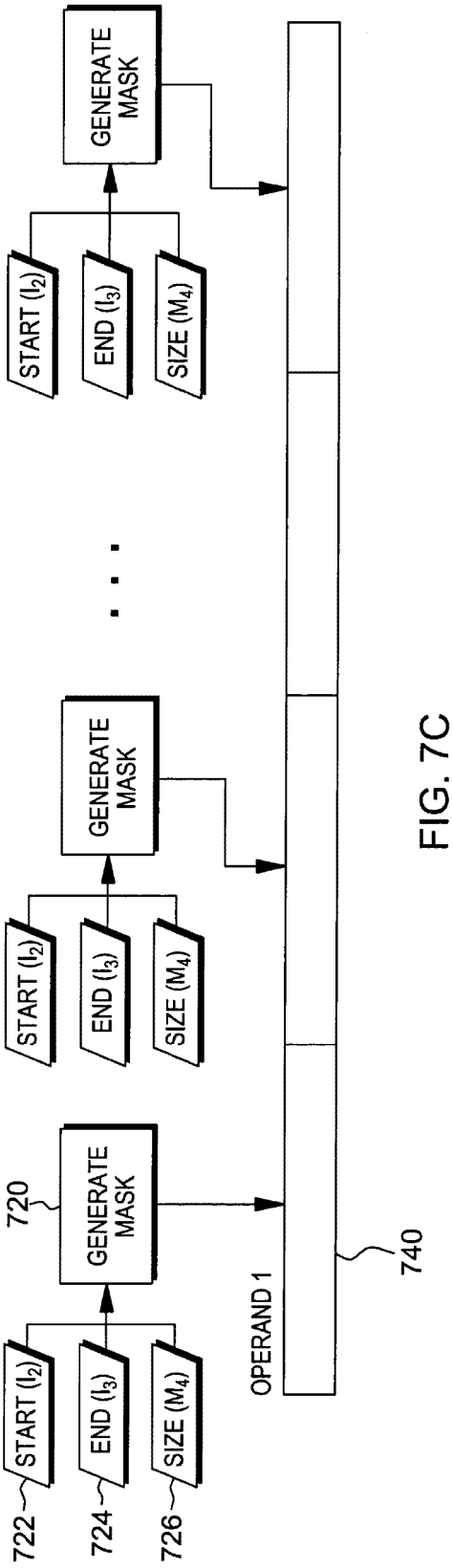
GENERATE MASK
START (I_2)
END (I_3)
SIZE (M_4)
GENERATE MASK
START (I_2)
END (I_3)
SIZE (M_4)
GENERATE MASK
720
START (I_2)
END (I_3)
SIZE (M_4)
722
724
726
OPERAND 1
740

FIG. 7C

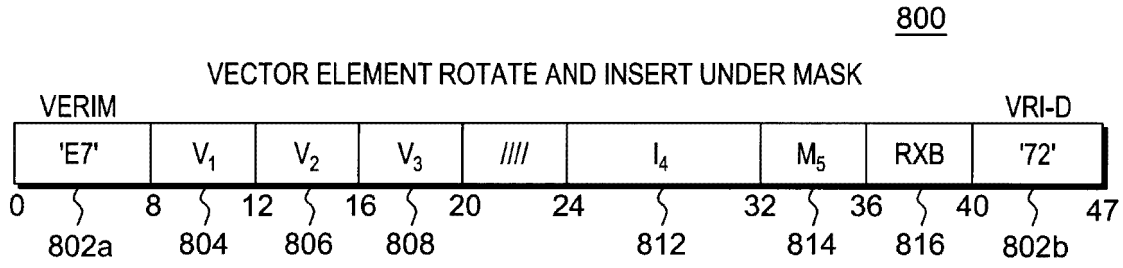
800
VECTOR ELEMENT ROTATE AND INSERT UNDER MASK
VERIM
VRI-D
'E7'
V1
V2
V3
////
I4
M5
RXB
'72'
0
8
12
16
20
24
32
36
40
47
802a
804
806
808
812
814
816
802b

FIG. 8A

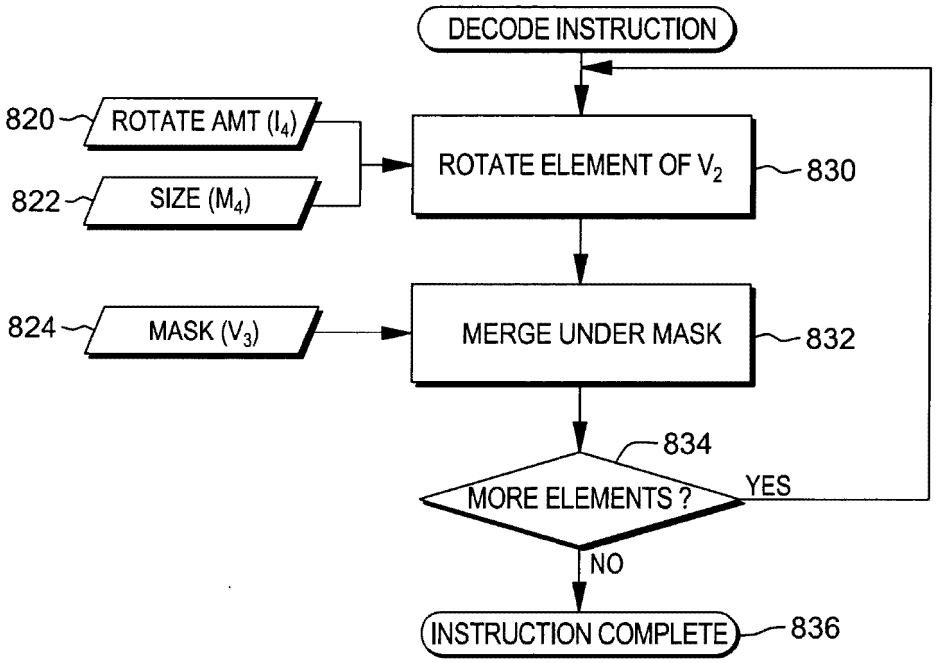
DECODE INSTRUCTION
820
ROTATE AMT (I4)
822
SIZE (M4)
ROTATE ELEMENT OF V2
830
824
MASK (V3)
MERGE UNDER MASK
832
834
MORE ELEMENTS ?
YES
NO
INSTRUCTION COMPLETE
836

FIG. 8B

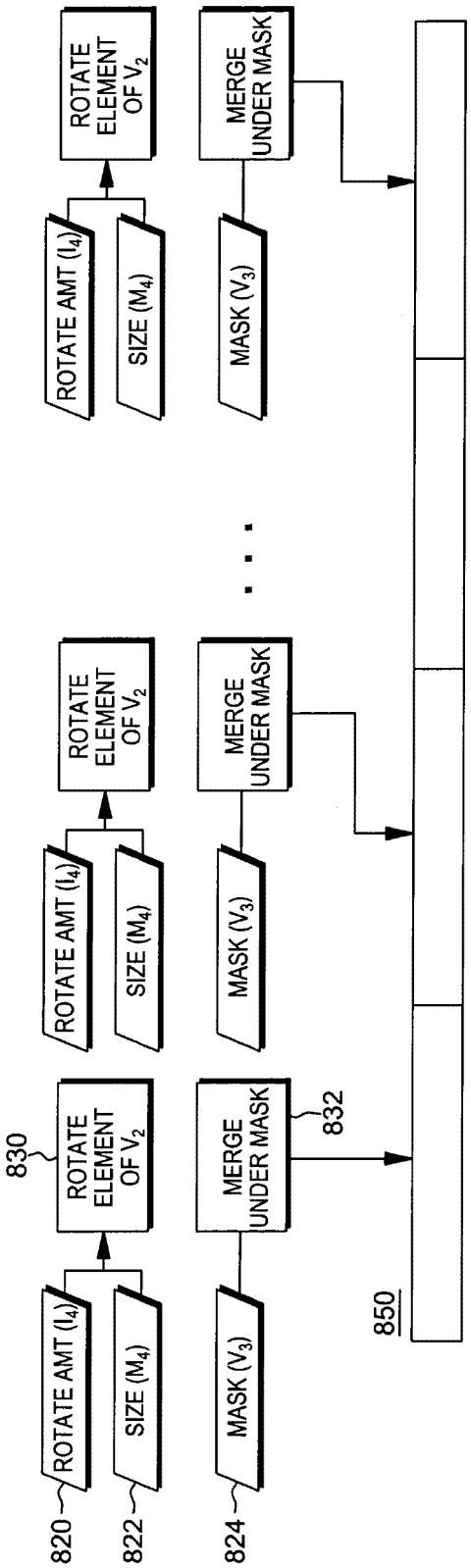
ROTATE AMT (I_4)
SIZE (M_4)
MASK (V_3)
ROTATE ELEMENT OF V_2
MERGE UNDER MASK
820
822
824
830
832
850

FIG. 8C

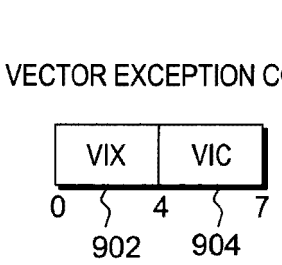
900
VECTOR EXCEPTION CODE
VIX
VIC
0
4
7
902
904

FIG. 9A

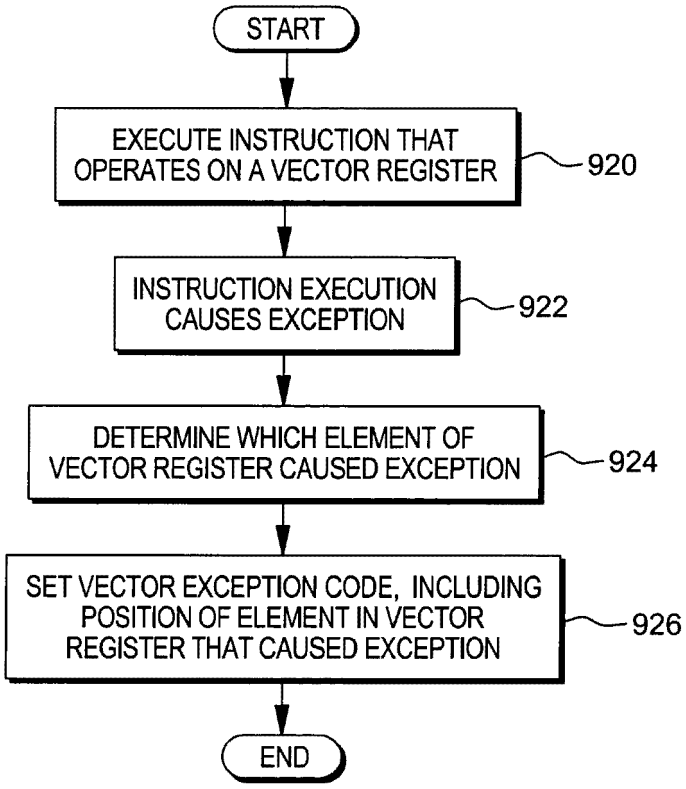
START
EXECUTE INSTRUCTION THAT OPERATES ON A VECTOR REGISTER
920
INSTRUCTION EXECUTION CAUSES EXCEPTION
922
DETERMINE WHICH ELEMENT OF VECTOR REGISTER CAUSED EXCEPTION
924
SET VECTOR EXCEPTION CODE, INCLUDING POSITION OF ELEMENT IN VECTOR REGISTER THAT CAUSED EXCEPTION
926
END

FIG. 9B

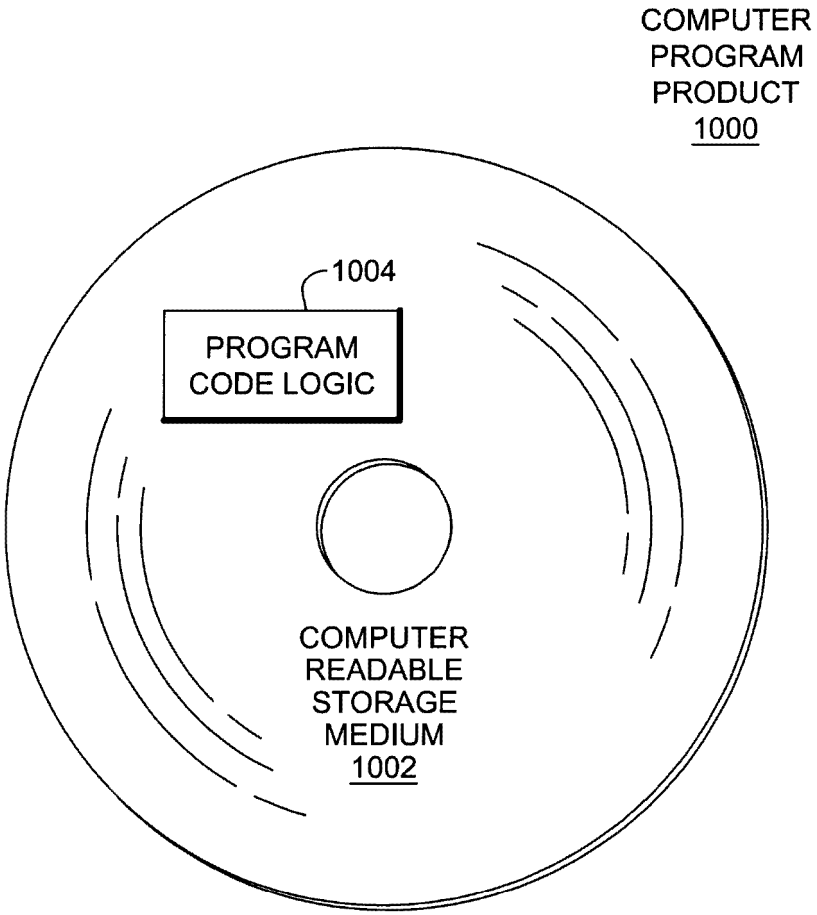
COMPUTER
PROGRAM
PRODUCT
1000
1004
PROGRAM
CODE LOGIC
COMPUTER
READABLE
STORAGE
MEDIUM
1002

FIG. 10

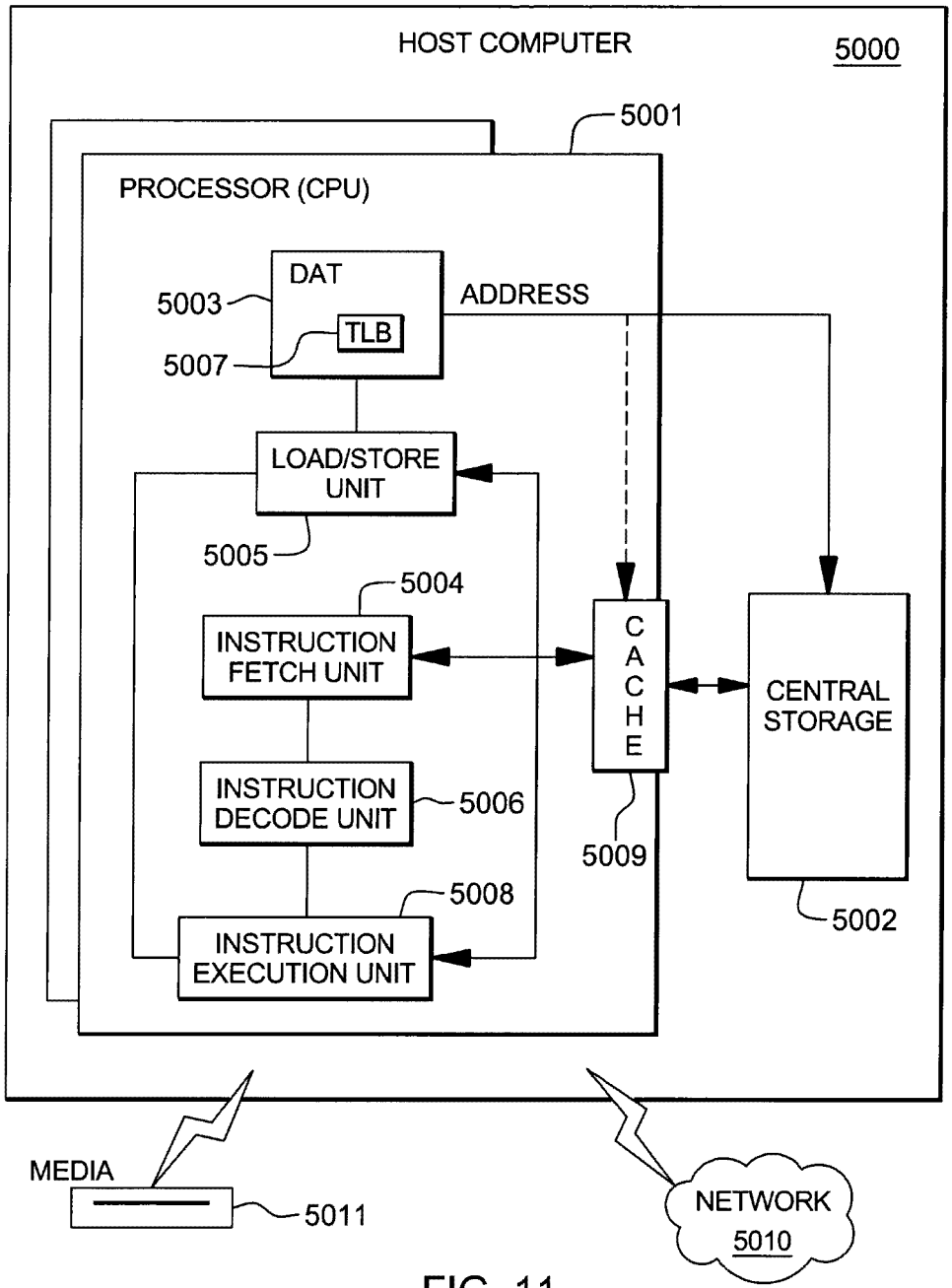
HOST COMPUTER
5000
5001
PROCESSOR (CPU)
DAT
5003
TLB
5007
ADDRESS
LOAD/STORE UNIT
5005
5004
INSTRUCTION FETCH UNIT
INSTRUCTION DECODE UNIT
5006
5008
INSTRUCTION EXECUTION UNIT
CACHE
5009
CENTRAL STORAGE
5002
MEDIA
5011
NETWORK
5010

FIG. 11

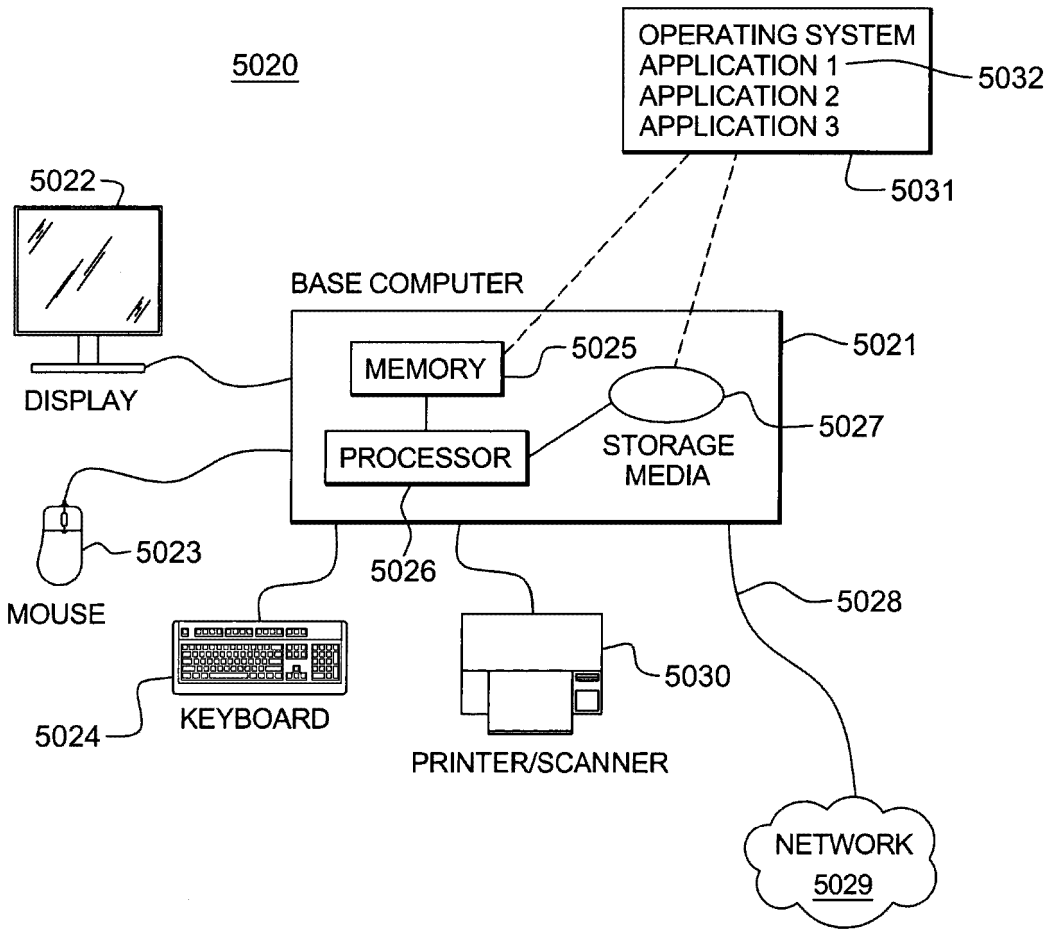
5020
OPERATING SYSTEM
APPLICATION 1
APPLICATION 2
APPLICATION 3
5032
5031
5022
BASE COMPUTER
MEMORY
5025
5021
5027
PROCESSOR
STORAGE MEDIA
DISPLAY
5023
MOUSE
5026
5028
5030
5024
KEYBOARD
PRINTER/SCANNER
NETWORK
5029

FIG. 12

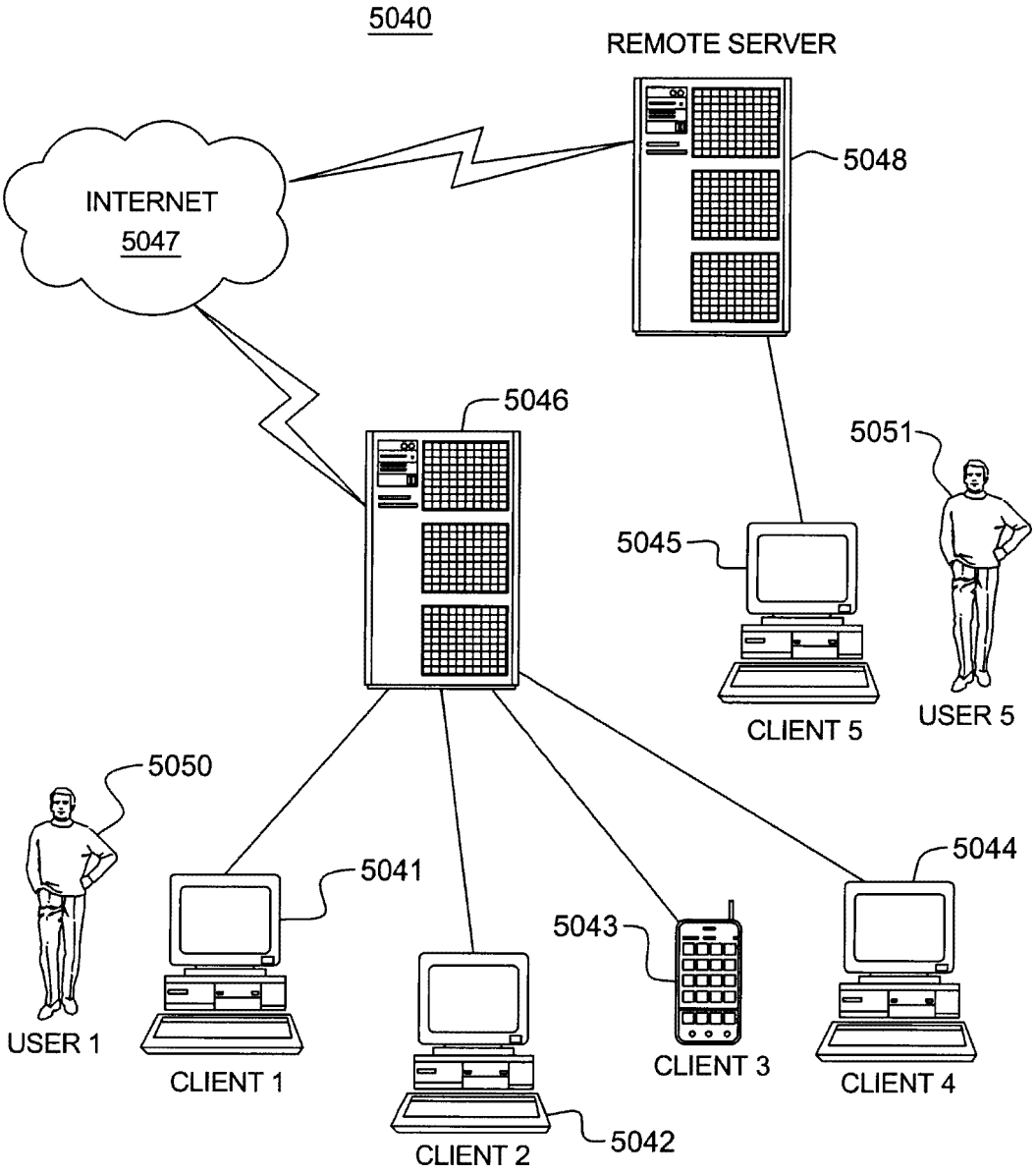
5040
REMOTE SERVER
5048
INTERNET
5047
5046
5051
5045
CLIENT 5
USER 5
5050
5041
5044
5043
USER 1
CLIENT 1
CLIENT 3
CLIENT 4
CLIENT 2
5042

FIG. 13

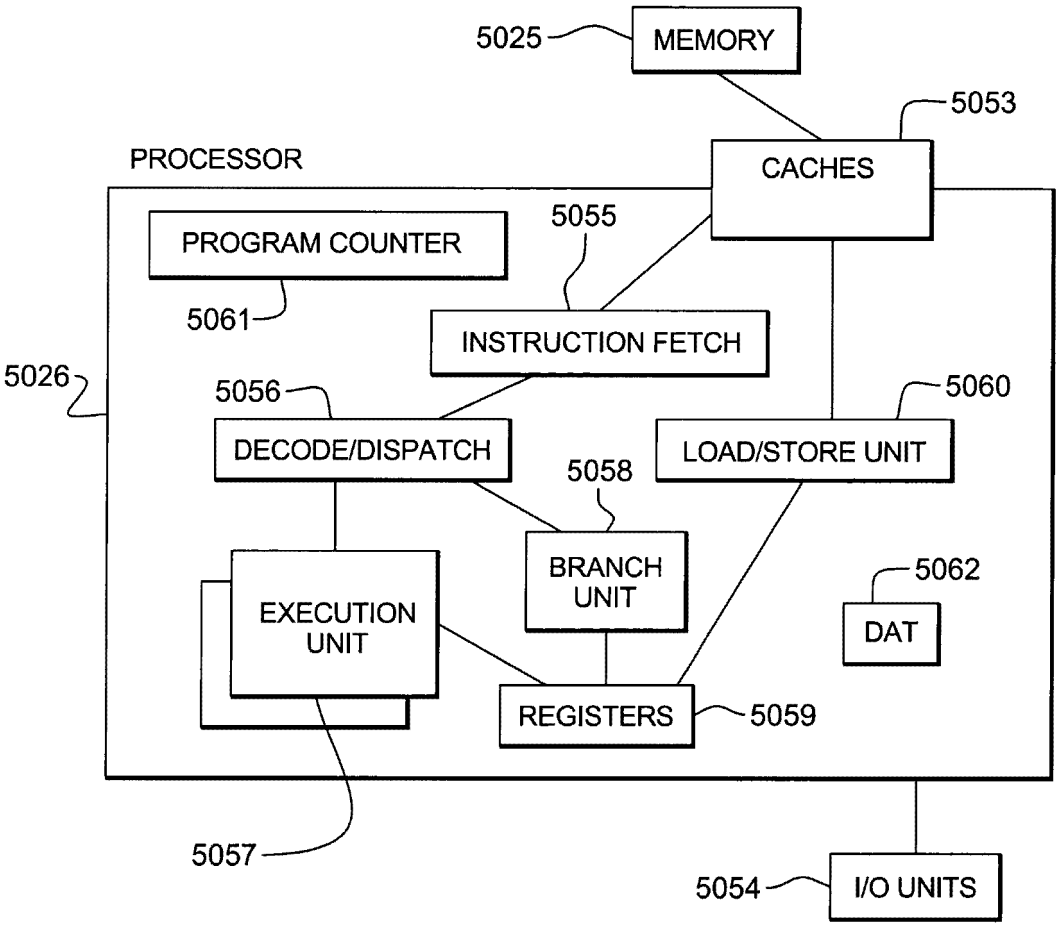
5025
MEMORY
5053
CACHES
PROCESSOR
PROGRAM COUNTER
5055
5061
INSTRUCTION FETCH
5026
5056
5060
DECODE/DISPATCH
LOAD/STORE UNIT
5058
BRANCH UNIT
5062
DAT
EXECUTION UNIT
REGISTERS
5059
5057
5054
I/O UNITS

FIG. 14

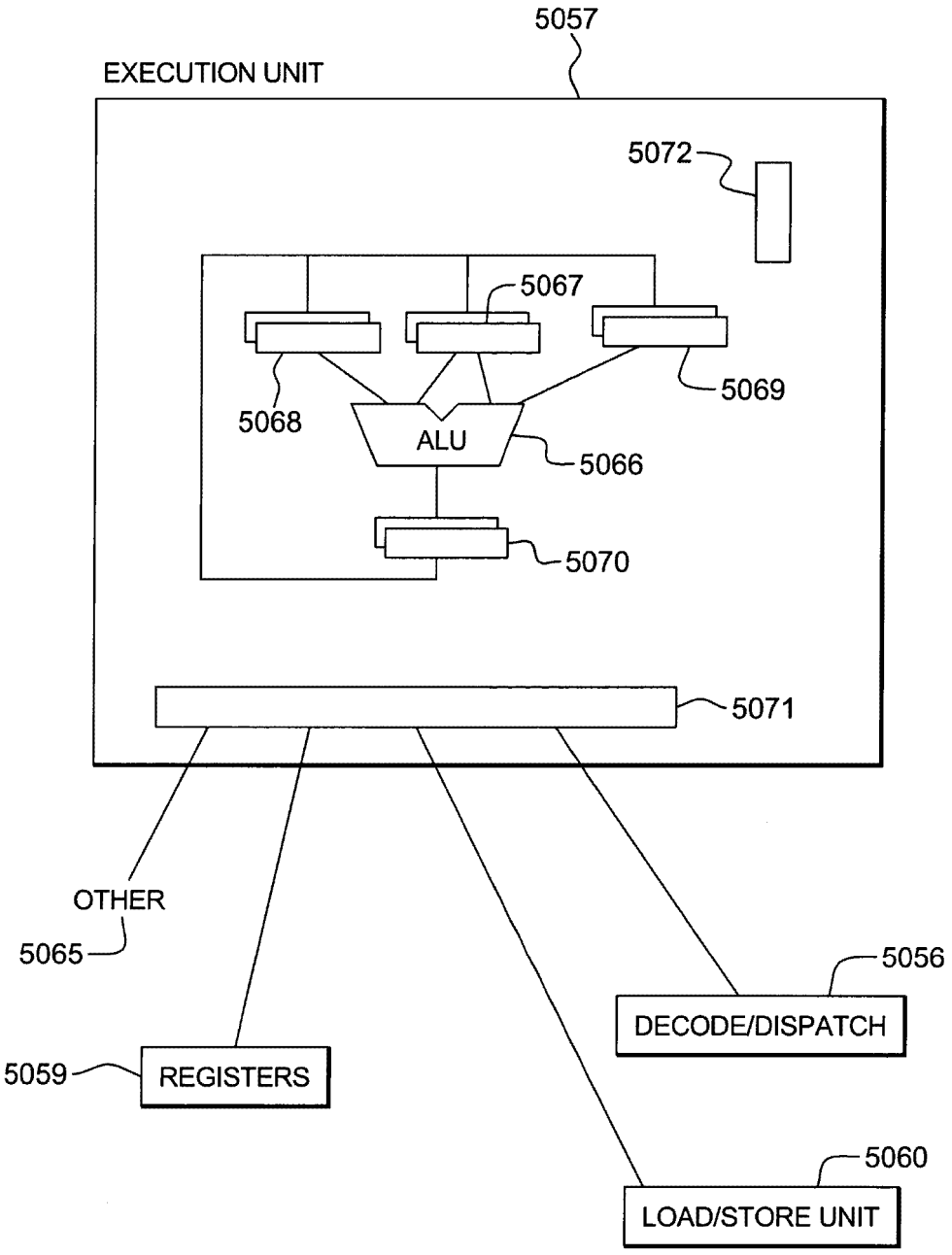
5057
EXECUTION UNIT
5072
5067
5068
5069
ALU
5066
5070
5071
OTHER
5065
5056
DECODE/DISPATCH
5059
REGISTERS
5060
LOAD/STORE UNIT

FIG. 15A

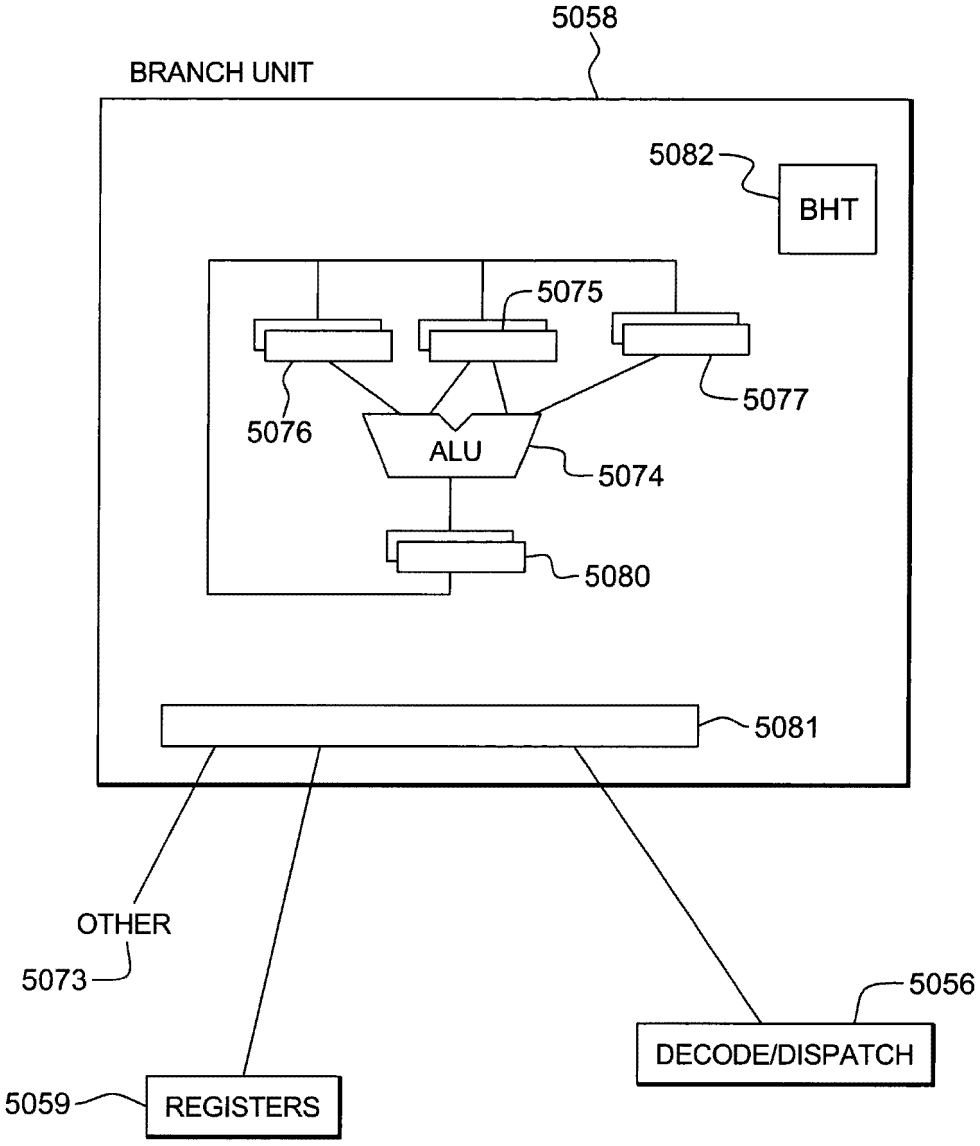
5058
BRANCH UNIT
5082
BHT
5075
5076
5077
ALU
5074
5080
5081
OTHER
5073
5056
DECODE/DISPATCH
5059
REGISTERS

FIG. 15B

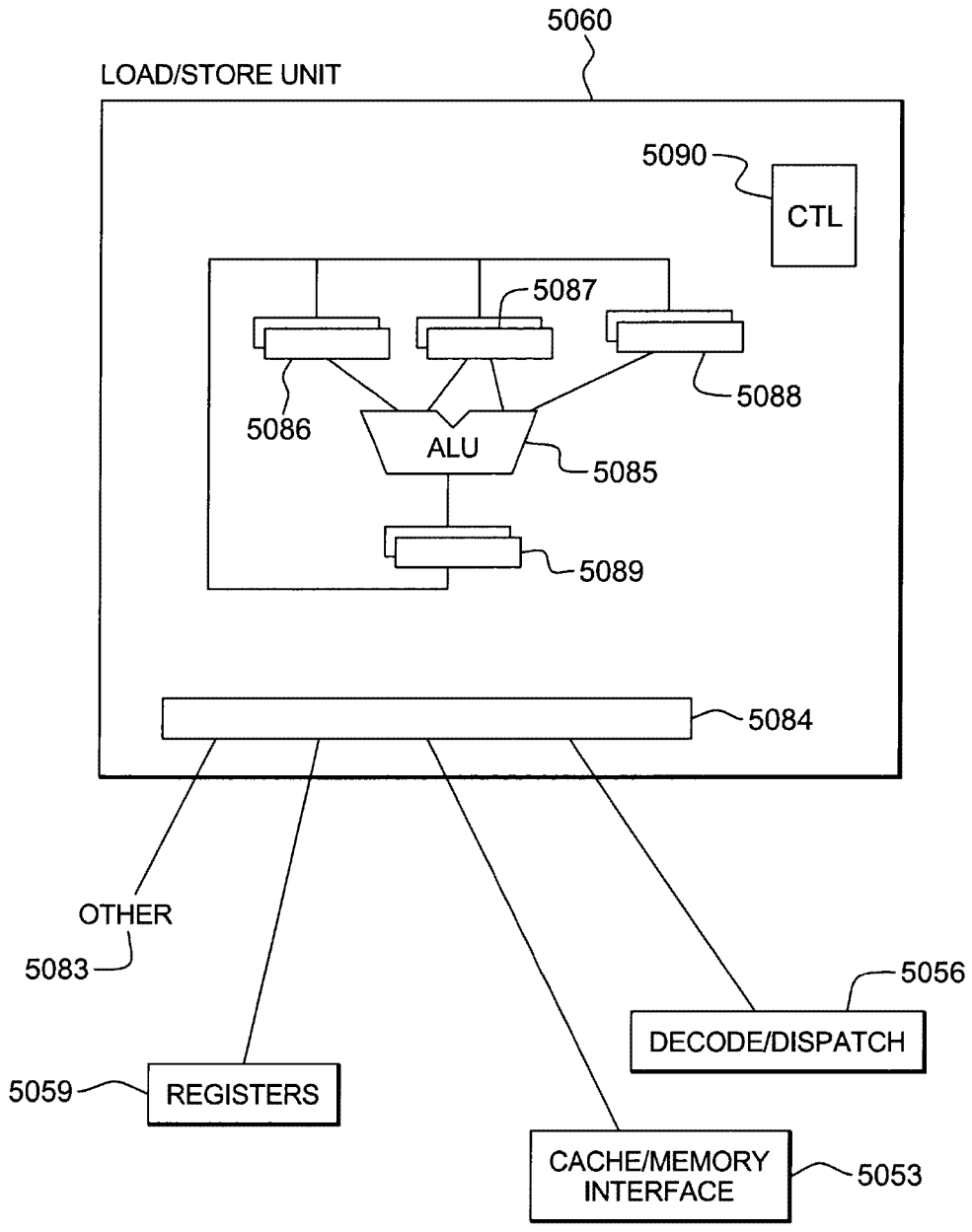
5060
LOAD/STORE UNIT
5090
CTL
5087
5086
5088
ALU
5085
5089
5084
OTHER
5083
5056
DECODE/DISPATCH
5059
REGISTERS
CACHE/MEMORY
INTERFACE
5053

FIG. 15C

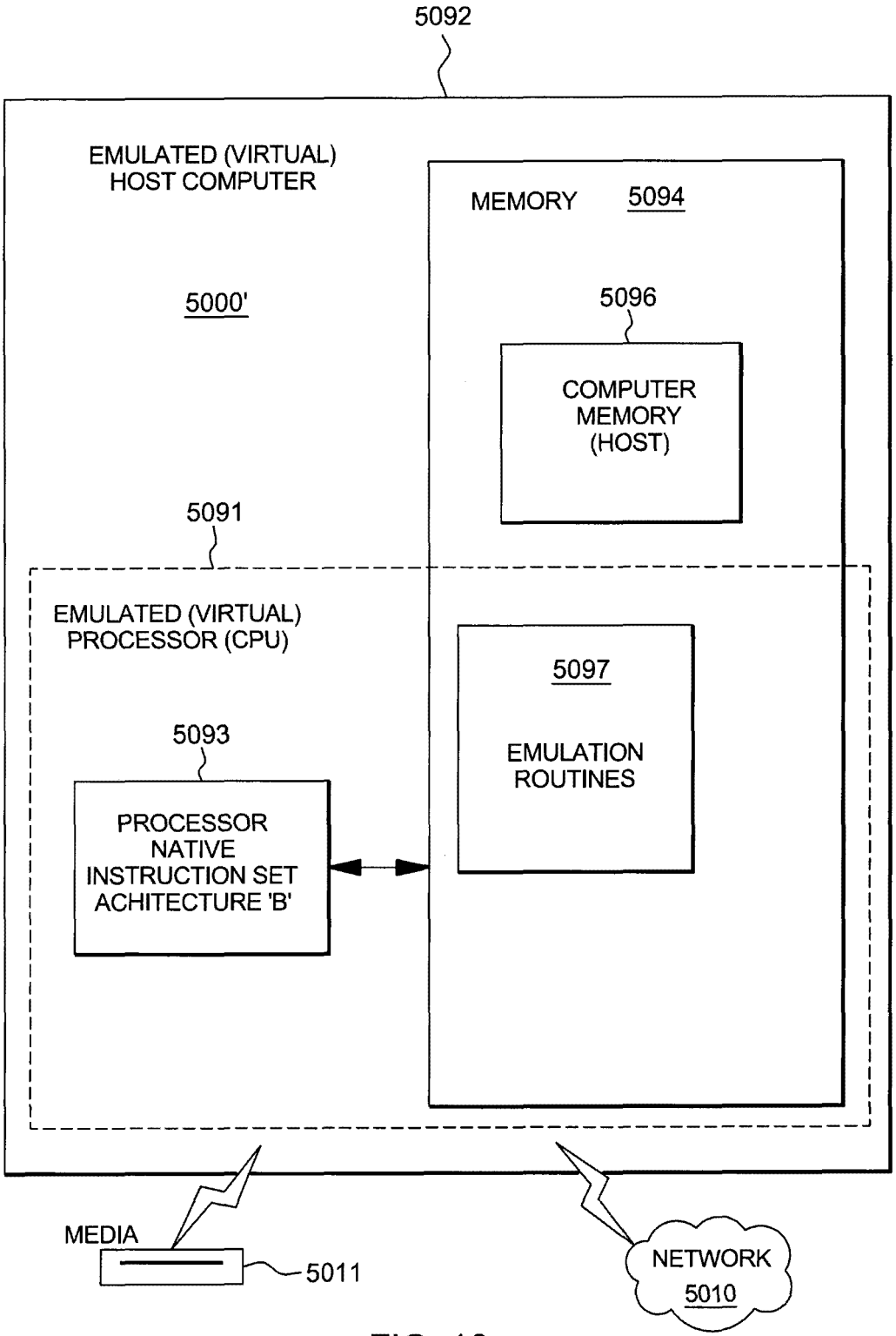
5092
EMULATED (VIRTUAL)
HOST COMPUTER
5000'
MEMORY 5094
5096
COMPUTER
MEMORY
(HOST)
5091
EMULATED (VIRTUAL)
PROCESSOR (CPU)
5097
EMULATION
ROUTINES
5093
PROCESSOR
NATIVE
INSTRUCTION SET
ACHITECTURE 'B'
MEDIA
5011
NETWORK
5010

FIG. 16