(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 January 2010 (07.01.2010)

PCT

(10) International Publication Number
WO 2010/002515 A2

(51) International Patent Classification:
H01L 21/20 (2006.01)

(21) International Application Number:
PCT/US2009/044810

(22) International Filing Date:
21 May 2009 (21.05.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0803696 30 June 2008 (30.06.2008) FR
61/093,887 3 September 2008 (03.09.2008) US

(71) Applicant *(for all designated States except US)*: **S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES** [FR/FR]; Parc Technologique Des Fontaines, F-38190 Bernin (FR).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **MAZURE, Carlos** [FR/FR]; 143 Chemin Du Bas Bernin, Residence Cidex 64a, F-38190 Bernin (FR). **NGUYEN, Bich-yen** [US/US]; 110 S. Laurelwood Drive, Austin, TX 78733 (US).

(74) Agents: **FANUCCI, Allan, A.** et al.; Winston & Strawn Llp, Patent Department, 1700 K Street, N.w., Washington, DC 20006-3817 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) Title: LOW-COST SUBSTRATES HAVING HIGH-RESISTIVITY PROPERTIES AND METHODS FOR THEIR MANUFACTURE

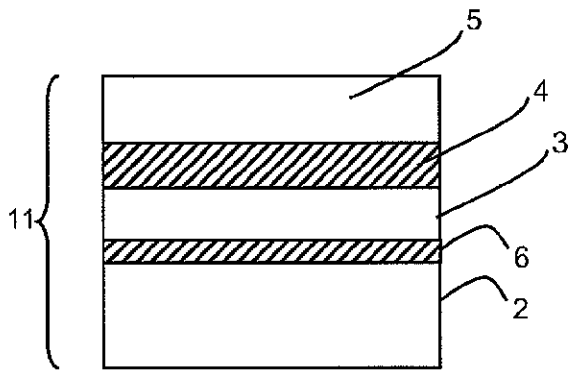


Figure 2

(57) Abstract: In one embodiment, the invention provides substrates that are structured so that devices fabricated in a top layer thereof have properties similar to the same devices fabricated in a standard high resistivity substrate. Substrates of the invention include a support having a standard resistivity, a semiconductor layer arranged on the support substrate having a high-resistivity, preferably greater than about 1000 Ohms-cm, an insulating layer arranged on the high-resistivity layer, and a top layer arranged on the insulating layer. The invention also provides methods for manufacturing such substrates.

WO 2010/002515 A2