Detachable substrate with controlled mechanical hold and method for production thereof

Field of the invention

The invention relates to a method of assembling two microelectronic wafers and the resulting structure. It finds applications in the fabrication of thin layer substrates and in transferring layers or components onto supports of any kind.

Description of the prior art

Increasingly, components must be integrated onto supports different from those used to produce them.

Components on plastics material substrates or on flexible substrates may be cited, for example. By component is meant any microelectronic, optoelectronic or sensor (for example chemical, mechanical, thermal, biological or biochemical sensor) device that is completely or partly "processed", i.e. completely or partly produced.

A layer transfer method can be used to integrate the components onto flexible supports.

There are many other examples of applications in which layer transfer techniques can provide a suitable solution for integrating components or layers onto a support that is *a priori* different from that used for their production. In the same line of thinking, layer transfer techniques are also very useful when it is required to isolate a thin layer, with or without components, from its original substrate, for example by demounting or eliminating the latter. Still in the same line of thinking, turning over a thin layer and transferring it onto another support provides engineers with valuable freedom to design structures that would otherwise be impossible. Sampling and turning over thin films can be used to produce buried structures, for example, such as buried capacitors for dynamic random access memory (DRAM) where, in contradistinction to the usual situation, the capacitors

are formed first and then transferred onto another silicon substrate before fabricating the remainder of the circuits on the new substrate. Another example relates to the production of transistor structures referred to as double gate structures. The first gate of the CMOS transistor is produced on a substrate using a conventional technology and then turned over and transferred to a second substrate to produce the second gate and finish the transistor, thereby leaving the first gate buried in the structure (see, for example, K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie and T. Sugii, "High-Speed and Low-Power n+-p+ Double-Gate SOI CMOS", IEICE Trans. Electron., vol. E78-C, 1995, pp. 360-367).

The requirement to isolate a thin layer from its original substrate is encountered in the field of light-emitting diodes (LED), for example, for instance as reported in the documents W.S Wong *et al.*, Journal of Electronic MATERIALS, page 1409, Vol. 28, N° 12, 1999 and I. Pollentier *et al.*, page 1056, SPIE Vol. 1361 Physical Concepts of Materials for Novel Optoelectronic Device Applications I (1990). One of the objects sought here is to improve the control of extraction of the emitted light. Another object relates to the fact that in this particular example the sapphire substrate used to produce the epitaxial stack is *a posteriori* bulky, in particular because it is electrically insulative, which prevents making electrical contacts. To be able to remove afterwards the sapphire substrate, which was advantageous for the phase of growing the material, would thus appear to be desirable.

An identical situation is encountered in the field of applications to telecommunications and microwaves, for example. In this situation, it is preferable for the components to be finally integrated onto a support having a high resistivity, typically at least several kohms.cm.

However, a highly resistive substrate is not necessarily available at the same cost and with the same quality as the standard substrates usually employed. In the case of silicon, 200 and 300 mm diameter silicon wafers of standard resistivity are available, whereas for resistivities greater than 1 kohm.cm, there is very little on offer in the 200 mm size and nothing at all in the 300 mm size. One solution consists in producing the components on an original structure including a standard substrate (for example of p-type silicon having a resistivity from 14 to 22 ohm.cm) and then, during the final process steps, transferring a thin layer containing the components onto a glass, quartz, sapphire, *etc.* insulative substrate.

From a technical point of view, the major benefit of these transfer operations is to decorrelate the properties of the layer in which the components are formed and those of the final support, and they are consequently beneficial in many other situations.

There may also be cited situations in which the original substrate that is beneficial for the production of the components is excessively costly. In the case of silicon carbide, for example, offering improved performance (higher temperatures of use, significantly improved maximum powers and frequencies of use, *etc.*), but whose cost compared to silicon is very high, it would be beneficial to transfer a thin layer of the costly original substrate (in this instance silicon carbide) onto the inexpensive final substrate (here silicon), and to recover the remainder of the costly original substrate for reuse, possibly after a recycling operation. The transfer operation can be carried out before, during or after the production of the components.

The above techniques can also prove beneficial in all fields in which obtaining a thin final substrate is important for the final application. Power applications in

particular may be cited, whether for reasons associated with the evacuation of heat or because in some cases the current must flow through the thickness of the substrates with losses that are to a first approximation proportional to the thickness through which the current passes. Smart card applications for which a thin substrate is required for reasons of flexibility may also be cited. For these applications, the circuits are produced on thick or standard thickness original substrates, which has the advantage, firstly, of good mechanical resistance to the various process steps, and, secondly, of conforming to standards with regard to their use on certain production equipment. The final thinning is then achieved by demounting. This demounting can be accompanied by transfer to another support. In some cases the transfer to another support is not indispensable, especially if the final thickness aimed at during thinning is sufficient to produce self-supporting structures.

Various techniques can be used to transfer layers from one support to another. In some cases, the assembly of the layer and the support can be temporary. This is the case, for example, when using for the thin layer transfer handle substrates whose function is to provide a guaranteed hold during the transfer or during various treatments to which the layer is subjected before the transfer. On this subject see the document by T. Hamagushi *et al.*, IEDM 1985, p. 688 - 691. A problem then arises in choosing the means employed to assemble the layer and the substrate. The adhesion means must in particular be sufficiently strong to fulfill their role and in particular to resist the stresses imposed by the treatments applied to the portion to be transferred. Also, it must be possible to demount the assembly in order to free the layer to be transferred. There are additional stresses (thermal, mechanical, *etc.*) on the adhesion means when components (microelectronic,

optoelectronic, mechanical, piezoelectric, superconductor, or magnetic components) must be produced completely or in part before transferring the thin layer when that layer is fastened to the handle substrate. The adhesion means must therefore be both strong to provide the assembly between the thin layer and the handle substrate, even during the component fabrication processes, and at the same time reversible to enable the final demounting of the handle substrate.

More generally, the problem that arises is that of assembling a wafer with another wafer, which wafers can be substrates, thin layers, or sufficiently thick to be self-supporting, composite or otherwise, composed of at least one or more semiconductor materials, partly or completely processed or unprocessed, the assembly having to be demounted thereafter at the assembly interface. Before demounting, it must have been possible to produce a part or the whole of components on at least one of the two wafers or to carry out a step of epitaxial growth.

Various solutions have been envisaged.

The first solution consists in eliminating the support wafer by abrasion, but in this case the wafer is consumed (destroyed during the process). This is also the case if an etch stop layer is provided between the two wafers: the support wafer is consumed by a combination of abrasion and etching.

Other methods, based on the "lift-off" principle, also demount a thin layer previously bonded to an original support, again without the latter necessarily being consumed. These methods generally use selective chemical etching of a buried intermediate layer, possibly associated with mechanical forces. This type of method is very widely used to transfer III-V elements to different types of support (see C. Camperi *et al.*, IEEE Transactions on photonics technology, vol. 3, 12 (1991), 1123). As

explained in the paper by P. Demeester *et al.*, Semicond. Sci. Technol. 8 (1993), 1124-1135, the transfer, which generally takes place after an epitaxial growth step, can be carried out before or after the production of the components (by "post-processing" or "pre-processing", respectively). However, these techniques based on lifting off depend on the fact that it is difficult to obtain lift-off on a lateral scale exceeding 1 mm.

Another situation consists in exploiting the presence of a buried oxide in the case of a silicon on insulator (SOI) structure, however standard the latter may otherwise be (i.e. produced without seeking any particular demountability effect). If the structure is bonded sufficiently strongly to another substrate and a high stress is applied to the structure, uncontrolled fracture, preferentially achieved in the oxide, can lead to a cutting effect on the scale of the entire substrate. The document "PHILIPS Journal of Research", vol. 49, N° 1/2, 1995, shows an example of this on pages 53 to 55. Unfortunately, the fracture is difficult to control and necessitates high mechanical stresses to bring it about, which is not free of the risk of breaking of the substrate or damaging the components.

The document EP0703609 A1 discloses transferring a layer onto a final substrate by controlling the bonding energies. However, in the above document, there is a first bonding energy between a thin layer and a first substrate. The bonding energy of the adherent contact between the layer and the second substrate, the target substrate, or the manipulator is then controlled so that it is greater than the first bonding energy, between the layer and the first substrate.

The techniques used to increase a bonding energy between two wafers are widely known. They are used in the situations cited previously, but also in other situations.

There is the production of SOI structures, for example.

If SOI structures are to be obtained, the surface preparation operations are intended finally to provide, and often with the aid of annealing carried out after bonding, high bonding energies typically from 1 to 2 J/m^2. Conventionally, in the case of SiO_2/SiO_2 bonding with standard preparation operations, the bonding energy of the structure is a few tens of mJ/m^2 at room temperature and 500 mJ/m^2 after annealing at 400°C for 30 minutes, (bonding energy determined by the blade method developed by Maszara (see: Maszara *et al.*, J Appl. Phys., 64 (10), p. 4943, 1988). When the structure is annealed at a high temperature (1 100°C), the bonding energy is generally of the order of 2 J/m^2 (C. Maleville *et al.*, Semiconductor wafer bonding, Science Technology and Application IV, PV 97-36, 46, The Electrochemical Society Proceedings Series, Pennington, NJ (1998)). Other forms of preparation prior to bonding exist, for example exposure of the surfaces to be bonded to a plasma (for example an oxygen plasma), and can yield equivalent bonding energies without always necessitating such annealing (YA, Li and R.W. Bower, Jpn. J. Appl. Phys., vol. 37, p. 737, 1998). Sealing with energies of this magnitude is incompatible with demounting.

Some variants are known as bonded SOI (BSOI) and bond and etch back SOI (BESOI). In addition to molecular adhesion bonding, these variants are based on physical removal of the original substrate by polishing techniques and/or chemical etching techniques. In this case the substrate is consumed.

The inventors have shown that by modifying the hydrophilic properties and the roughness of the surfaces, different mechanical strengths can be obtained, greater than or less than the mechanical strengths conventionally obtained. For example, as indicated in the paper by O. Rayssac *et al.* (Proceedings of the 2nd International

Conference on Materials for Microelectronics, IOM Communications, p. 183, 1998), hydrofluoric acid etching increases the roughness of a silicon oxide layer. The paper states that an 8 000 Å etch increases the rms roughness by approximately 0.2 nm to 0.625 nm. It has been verified that SiO_2/SiO_2 bonding with an rms roughnesses of 0.625 nm and 0.625 nm for the facing surfaces yields a maximum bonding energy value of the order of 500 mJ/m^2 after annealing at 1 100°C, i.e. much lower than in the standard situation.

Technical problem and solution in accordance with the invention

The invention therefore consists in a technique of assembling by molecular adhesion bonding of two wafers, the resulting structure being intended to be demounted at the assembly interface. The demounting or lifting off of the structure is generally carried out after components or sensors have been completely or partly produced on the layer or after a step of epitaxial growth on one of the wafers.

The invention also consists in a structure comprising two wafers joined together by an interface or an intermediate layer having a level of mechanical strength that is easy to control, so that said structure is compatible with the complete or partial production of components (for example the deposition of an epitaxial stack), but also so that said structure can be demounted. The literature generally refers to such structures as "demountable structures" or "demountable substrates".

To this end the invention proposes to produce an interface by molecular adhesion bonding of one face of one wafer and one face of another wafer, with a prior treatment step applied to at least one of the faces to be bonded to control the level of mechanical strength of the interface. The molecular adhesion bonding can be carried out with or without an intermediate layer (oxide, nitride).

In a situation corresponding rather to demounting at the levels of portions of the wafer (dies, components or sets and subsets of dies, *etc.*), the preparation of the wafer preferably includes a step whereby at least one fragment of said layer is delimited before the demounting step.

To control the mechanical strength of the interface, a step of preparing at least one of the two faces to be assembled is necessary in order to control the roughness and/or the hydrophilic properties thereof.

- To prepare the surface by controlling the roughness, in the case of SiO_2 surfaces, for example, hydrofluoric acid etching can be used. Other chemical treatments are possible, of course, as a function of the nature of the material to be etched.

- To produce a demountable substrate of the SOI type, the examples of SiO_2/SiO_2 and Si/SiO_2 bonding are considered. In the case of layers of different kinds (Si_3N_4 is another conventional example, but there are also the silicides), it suffices to use suitable chemical treatment (for example H_3PO_4 or HF for Si_3N_4, by analogy with $NH_4OH/H_2O_2/H_2O$ (also called SC1) for Si).

- The mechanical strength of the interface is modified by treatment, for example heat treatment, to strengthen the interface in a controlled manner, i.e. so that it is compatible with subsequent demounting, by controlling the heat treatment parameters (the treatment time, the temperature, the temperature gradient, *etc.*). The heat treatments include those associated with the subsequent production of components. The faces treated in this way can then be molecular adhesion bonded, with or without an intermediate layer (such as an oxide or nitride layer, for example).

- The step of producing the interface is followed by a step of lifting off the two wafers; a step of producing a

part or the whole of microelectronic, optoelectronic, mechanical, pyroelectric, superconductor or magnetic components can be executed after demounting. Between the step of producing the interface and the lifting off step, another bonding step can advantageously be executed to create a second interface. This bonding step advantageously includes molecular adhesion bonding or adhesive bonding (for example using an adhesive hardened by UV radiation, a resin, a polymer adhesive). In this case, a lift-off step at the level of the second interface can advantageously be carried out by acid etching and/or application of mechanical stresses and/or thermal and/or photonic stresses.

The wafer that has not been processed or transferred can advantageously be used again after lift-off.

- The wafers are preferably of semiconductor materials preferably chosen from Si, Ge, SiGe, SiC, GaN and other equivalent nitrides, AsGa, InP or ferroelectric or piezoelectric materials ($LiNbO_3$, $LiTaO_3$) or magnetic materials, "processed" or otherwise.

- A thin layer can be produced in at least one of the two wafers. The thin layer can be obtained by thinning an original substrate.

- Thinning is obtained by planing and/or chemical-mechanical polishing or other polishing and/or chemical etching.

- The thin layer can be obtained by cutting.

- Cutting is achieved by fracturing a weak buried layer.

- The weak buried layer is obtained by implantation and the fracture is obtained by heat and/or mechanical and/or chemical treatment.

- The substance implanted is a gas (hydrogen, helium, *etc.*).

In terms of product, the invention proposes an

assembly comprising two wafers joined together at a bonding interface whose mechanical strength is at a controlled level, in particular through controlling the surface roughness and/or the hydrophilic properties.

According to preferred features, possibly in combination:

- A thin layer can be produced in at least one of the two wafers.
- Said layer is further bonded to a second substrate, advantageously by molecular adhesion bonding or adhesive bonding, for example using an adhesive hardened by UV radiation.
- The chemical and/or mechanical strength of the interface or connecting layer is modified selectively using localized or nonuniform treatments (heat treatment, UV exposure, laser irradiation, *etc.*) to reinforce selectively or to weaken selectively some regions more than others, according to whether it is a question of bonding roughened surfaces, porous materials, buried defects, gaseous or nongaseous microcavities.
- The layer is of semiconductor materials (Si, Ge, SiGe, SiC, GaN and other equivalent nitrides, AsGa, InP, *etc.*) or ferroelectric or piezoelectric materials ($LiNbO_3$, $LiTaO_3$) or magnetic or superconductor materials (YbaCuO, NbN, *etc.*), whether "processed" or not.

Brief description of the drawings

Aspects, features and advantages of the invention will emerge from the following description, which is given by way of illustrative and nonlimiting example and with reference to the appended drawings, in which:

- figure 1 is a diagrammatic view in section of an assembly comprising a thin layer on a substrate, the interface between the layer and the substrate having a bonding energy,
- figure 2 is a diagrammatic view of the figure 1

assembly after depositing or growing a surface layer,

- figure 3 is a view of the previous structure after molecular bonding a second substrate known as the final substrate,

- figure 4 is a view during a lifting off action at the interface between the thin layer and the first substrate,

- figure 5 is a diagrammatic view of a wafer obtained after lifting off and removing the freed interface layer,

- figure 6 is a view of a figure 1 type demountable assembly,

- figure 7 is a view thereof after the production of components, for example a first transistor gate,

- figure 8 is a view thereof after depositing oxide,

- figure 9 is a view thereof after planarization (for example by CMP),

- figure 10 is a view thereof after molecular adhesion bonding (including heat treatment),

- figure 11 is a view thereof after demounting and deoxidation to remove the freed interface layer,

- figure 12 is a view of a figure 1 type demountable assembly,

- figure 13 is a view thereof after production of components,

- figure 14 is a view thereof during demounting by hydrofluoric acid etching and/or application of mechanical forces without transfer to a target substrate,

- figure 15 is a view thereof after demounting into a final substrate and a substrate that can be recycled,

- figure 16 is a variant of figure 13, after cutting trenches or notches between the components,

- figure 17 is a view thereof showing a component being lifted off, for example after hydrofluoric acid etching,

- figure 18 is a view analogous to figure 1,

- figure 19 is a diagrammatic view in section of the figure 3 assembly after adhesive bonding of a transparent substrate,

- figure 20 is a view of the upper portion of this assembly after lifting off and polishing,

- figure 21 is a view of the upper portion of this assembly after lifting off and polishing,

- figure 22 is an overall view analogous to that of figure 1, showing regions that are eliminated by chemical and mechanical cutting,

- figure 23 is a view thereof after bonding an upper substrate,

- figure 24 is a view of an assembly analogous to that of figure 1,

- figure 25 is a view thereof after depositing an epitaxial stack based on GaN,

- figure 26 is a view thereof after bonding of a substrate,

- figure 27 is a view thereof at the time of lifting off,

- figure 28 is a view of the upper portion thereof after removing the freed interface layer, and

- figure 29 is a view thereof after removing the layer initially under the stack.

Description of the invention

The preferred examples selected for the detailed description primarily relate to silicon, which is generally available in the form of round substrates, for example of 200 mm diameter. These methods transfer readily to other systems characterized in particular by materials other than silicon, in a nonlimiting manner and without departing from the scope of the invention.

Some embodiments of the method according to the invention tend to encourage lifting of the layer off its substrate at the overall level, i.e. on the scale of the

whole of the substrate, while others tend to lift off delimited fragments.

For producing a demountable SOI substrate, examples of SiO_2/SiO_2 and Si/SiO_2 bonding are considered. In the case of layers of different kinds (Si_3N_4 is another conventional example, but there are also silicides), and by analogy with what is described hereinafter, it suffices to use appropriate chemical treatment (for example $NH_4OH/H_2O_2/H_2O$ (also known as SC1) for Si and H_3PO_4 or HF for Si_3N_4). Figure 1 shows the option in which the substrate (11) and the thin layer (14) are of monocrystalline silicon and two intermediate layers (12) and (13) are formed prior to bonding on the substrate (11) and the thin layer (14), respectively. Of course, only one of the two intermediate layers (12) or (13) may suffice, and neither of them may exist (i.e. that of Si/Si bonding). If the intermediate layers (12) and (13) exist and are both of SiO_2, the system is referred to as SiO_2/SiO_2 bonding. If only one of the two exists, and consists of SiO_2, then the system is referred to as Si/SiO_2 bonding.

A number of techniques can be employed to produce a structure like that shown in figure 1, in addition to specific aspects related to molecular adhesion bonding, including those previously cited, for the production of nondemountable SOI substrates (see Semiconductor Wafer Bonding, Science and Technology, Q. Y. Tong and U. Gösele, Wiley Interscience Publication [sic]). Hereinafter the layer (14) is referred to as the active layer, being the layer comprising the components, except for certain special cases in which an additional, for example epitaxial, layer is deposited onto the layer (14). Some variants are known as bonded SOI (BSOI) and bond and etch back SOI (BESOI). In addition to molecular adhesion bonding, these variants are based on physical removal of the original substrate by polishing techniques and/or chemical etching techniques.

Other variants, partially described hereinbefore as layer transfer techniques, are based, in addition to molecular adhesion bonding, on demounting by "cutting" along a weakened region, such as the methods described in the documents US-A-5374564 (or EP-A-533551) and US-A-6020252 (or EP-A-807970): demounting along an implanted region, or in the document EP 0925888: demounting by fracture along a buried layer that has been rendered porous.

With reference to specific aspects related to bonding for the production of demountable substrates, in the case of SiO_2/SiO_2 (or even Si/SiO_2) bonding, the oxide layer can be prepared in several ways (deposition, thermal oxidation of the silicon) and can have a thickness that varies according to the application. For this example, a 1 μm thick thermal oxide is chosen. The following structure is therefore obtained: a silicon substrate covered with 1 μm of oxide.

This is followed by hydrofluoric acid etching to roughen the surface of the oxide, the roughening increasing with the thickness of oxide removed. For each application, the roughness can be optimized, in particular as a function of the conditions of the method of producing the components (or of epitaxial growth), which must be used after bonding with no delamination during the production of components and the method adopted for the final demounting. Typically, hydrofluoric acid etching to remove a thickness of oxide of the order of a few tens to a few hundred nanometers is a good starting compromise. The hydrofluoric acid etching increases the roughness of the oxide layer(s) (12) and/or (13). This can be combined with selective wet or dry cleaning to obtain hydrophilic properties specific to the oxide layer. The resulting effect is one of weaker bonding than the standard bonding.

Another option for controlling the bonding energy of the demountable interface is to use thermal annealing after

the bonding operation. A temperature difference of around 100° in the annealing effected after bonding can, especially in the range of temperatures beyond 800°C, lead to significant variation of the bonding energy. This option can be used in combination with roughening of at least one intermediate layer (12) and/or (13), or on its own (i.e. without any roughening step at all). An option that is highly beneficial, but must not in any way be regarded as limiting on the invention, of implementation for bonding is not to anneal the whole of the structure shown in figure 4, or to anneal it at a sufficiently low temperature, preferably a temperature not exceeding that at which the components are to be produced, the epitaxial layer, *etc.*, or for a short time, *etc.* This alternative is particularly attractive for applications that do not necessitate high temperatures for the production of components and other structures, for applications that do not use mechanical stresses and very aggressive chemical treatment of structures, and for applications that do not necessitate transfer onto a further support after demounting (self-supporting final structures).

Roughening and deposition of oxide have been cited in the situation in which they are carried out on the substrate (11). An alternative is to carry out these operations on the side of the thin layer (14), or even on both sides.

Apart from the production of the demountable substrate itself, using techniques based on molecular bonding, there are several means as to its use and to the means to implement it.

The benefit of the demountable substrate, depending on the thickness of the unprocessed active layer or of the processed active layer (i.e. its thickness when it has been processed to produce a part or the whole of a component), is that it allows demounting of the active layer to obtain

either a self-supporting layer (a relatively thick layer, whether the thickness is already present in the demountable substrate as manufactured or obtained during deposition steps subsequent to its fabrication, as is the case in an epitaxial growth step) or a surface layer, which is generally thinner, transferred onto a target support, whether the latter is the final support or merely a temporary support which is itself intended to be demounted.

There are various ways to transfer the surface layer to the target substrate.

First of all, transfer can be effected by molecular adhesion bonding of what is to become the thin layer to be transferred to another substrate.

The benefit of demountable substrates is also being able at will to "mount" and "demount" thin layers on substrates, allowing, by overturning the layer, total or partial production of components on both faces of the layer.

By way of illustration, a demounting method is described next in the context of producing a new SOI structure that is referred to herein as the second SOI structure. This kind of method, *a priori* less direct than the techniques previously mentioned, nevertheless has a number of benefits. The example chosen here relates to the production of a second SOI substrate with a buried oxide layer 500 Å thick, which thickness is difficult to obtain using this kind of method directly.

The first structure is obtained by one of the methods previously described, yielding a demountable substrate corresponding to figure 1. In this example the monocrystalline silicon layer 14 is to become the active layer. On this demountable substrate, in which the connecting layer has been roughened before bonding and has not undergone any strengthening heat treatment at very high temperatures (preferably less than 1 100°C and even better

less than 1 000°C or even 900°C), a 500 Å oxide layer 16 is formed by thermal oxidation to yield the structure shown in figure 2. This oxide is to become the buried oxide of the second SOI structure. In the present example, the demountable substrate (11+12+13+14+15) is molecular adhesion bonded to a silicon substrate 16 (see figure 3) that is to become the final support of the active layer. The stack obtained is preferably stabilized at a high temperature (1 100°C) to consolidate strongly the second bond at the interface of the layers (15) and (16). The first bond, if subjected to the same treatment, nevertheless has a mechanical strength less than that of the second bond because it is roughened first. A chemical and/or mechanical lift-off method can be used. For example, the stack obtained as above is first immersed in a hydrofluoric acid bath, one object of which is to overetch the oxide layers (12) and 13, starting from the edges of the assembly. The two interfaces 12/13 and 15/16 are preferentially etched. Moreover, the interface 12/13 of the demountable substrate is advantageously an oxide/oxide interface. This facilitates etching at the interface 15/16 between the oxide and the silicon. Accordingly, during this first lifting off step, there is less surface etching at the interface of the second bond than at the interface of the demountable substrate. Mechanical demounting (by pressurized water jet, as in the document EP 0925888, by compressed air jet, as in the document FR 2796491, by traction, as in the document WO 00/26000, by insertion of a blade, *etc.*) completely frees the final structure 13+14+15+16 (see figure 4). Following removal of the oxide 13, for example by hydrofluoric acid etching, the final SOI structure is obtained (figure 5). The Si wafer 11 that served as a substrate within the demountable substrate can be recycled and reused, for example to produce another demountable substrate (preferably after eliminating the

layer 12).

Another way to facilitate the onset of demounting is to eliminate at least part of an outer ring of the substrate. Wet or dry chemical etching techniques or other mechanical polishing, laser cutting, *etc.* techniques can be employed for this, localized to the ring (which yields the figure 22 configuration in which the cross-hatched areas are to be removed, which yields the figure 23 configuration after fixing a second substrate).

Note that the 500 Å thick buried oxide layer 15 formed previously on the layer 14 could have been formed on the substrate 16 before bonding rather than on the layer 14. Another variant divides the 500 Å thickness into two portions, with one portion on the substrate 16, for example 250 Å thick, and the other portion on the layer 14, also 250 Å thick in this example.

Note that if the two molecular adhesion bonded interfaces are both of the oxide/oxide type, stabilization of the second bond at high temperature can be carried out in such a way as to guarantee that preferential hydrofluoric acid etching occurs at the first interface. In this method, the creation of a weak first interface achieves preferential demounting of the complete stack at the first bonding interface.

Another example of the use of the method according to the invention relates to the production of double-gate transistor structures (see figures 6 to 11). The first operations relating to the fabrication of the transistors essentially consist in producing the first CMOS transistor gate (figure 7) on a demountable substrate using conventional technology (figure 6), as shown in figure 1, for example, in exactly the same way as previously described for the production of SOI structures with a thin buried oxide layer. The bonding stabilization temperature can be reduced in a temperature range of the order of

900/1 000°C. An oxide layer with a thickness of the order of 1 µm is then deposited onto this substrate (figure 8) using a conventional deposition technique (for example CVD). The oxide is planarized (figure 9) using a conventional chemical/mechanical polishing technique. This is followed (figure 10) by molecular adhesion bonding to another silicon substrate 16. The bonding is preferentially stabilized at a temperature from 1 000 to 1 100°C if the structures formed for the first gate can withstand this high a temperature, or at temperatures of the order of 900/1 000°C otherwise. Finally (figure 11), demounting is carried out in exactly the same way as previously (insertion of a blade, pressurized water jet, compressed air jet, *etc.*). Before resuming the transistor fabrication process, in particular to produce the second gate, the remainder of the oxide layer 13 is removed by chemical etching. Because the oxide is etched with a hydrofluoric acid solution of known etching selectivity with respect to silicon, etching stops naturally once the oxide has been entirely etched, revealing a silicon surface. The major advantage of this demounting technique over other techniques, for example based on fractures obtained by way of implantation for example, is that it does not necessitate excessively complex finishing sequences that are problematic in terms of their potential to create defects, as for a final polishing operation, for example.

The same method can be used in many other applications. If the first SOI structure (see figure 1) is used to produce transistors, circuits, components, *etc.*, these can be finally transferred onto many types of dedicated support. For example, the substrate 16 can be chosen for its electrical insulation properties (high-resistivity silicon, quartz, sapphire, *etc.*) to provide an ideal support for microwave and telecommunication circuits, thereby limiting losses in the substrate. For applications

relating to flat screens, a transparent substrate, for example of molten silica, is chosen for the final support.

Another example of demounting is briefly described here in the case of producing circuits on thin substrates (figures 12 to 15). The final thicknesses of interest are typically less than a few hundred µm, even of the order of a few tens of µm. They relate, for example, to power applications or applications to smart cards and other circuits for which some flexibility is required (plastics material supports, curved supports, *etc.*). This example relates to a type of demounting necessitating no transfer to a target substrate. Here the object is to achieve demounting without transferring the layer 14 after producing the circuits or components, when the layer 14 is sufficiently thick to be self-supporting but too thin to withstand without damage a collective circuit production process (typically less than a few hundred µm thick, and even of the order of a few tens of µm). The method of producing the demountable substrate is identical in every respect to any of those described previously to produce the figure 1 structure, for example. In the case of 200 mm diameter silicon wafers, the standard substrate thickness is 725 µm. If the application requires a final substrate thickness of 80 µm, for example, a silicon substrate 725 - 80 = 645 µm thick is chosen (figure 12) for the support substrate 11. The resulting assembly therefore corresponds to the standard thicknesses and offers satisfactory resistance to the processes for fabricating components. After production of the latter (figure 13), one of the demounting techniques previously cited may be used (figure 14), except that the substrate 16 can be omitted. After demounting, the self-supporting layer 14 (figure 15) alone represents the final substrate of interest, characterized by a substrate thickness of 80 µm, including the components.

The parameters for preparing the demounting interface have to be adapted to the technological operations that have to be carried out on the demountable substrate prior to demounting, in particular thermal and chemical treatments, and according to the nature of the mechanical stresses. For example, if the demountable substrate consists of a surface layer of germanium having an SiO_2-SiO_2 bonding interface that has to withstand an epitaxial growth temperature of 550°C (which is typical in the case of growing GaInAs to constitute a solar cell for use in space), then the rms roughness must advantageously be 0.4 nm for the substrate to be demountable.

Another example of use concerns the production of circuits for smart cards, where the flexibility of the support becomes critical, firstly because of the increase in the size of the circuits, and secondly because the trend is to require cards with ever higher resistance to deformation. A monocrystalline silicon support whose thickness is greater than around 50 µm is too fragile in this context, because its thickness is too high if it is subjected to a bending force, as can happen regularly with a smart card.

Note that, for the production of dies, there can be provided (see figure 16), starting from the figure 13 configuration, notches isolating fragments that a pull-off tool SA can remove individually (figure 17).

Figure 18 shows a starting assembly similar to that shown in figure 1, with a starting substrate 11' covered with a layer 12' of silicon oxide that is molecular adhesion bonded to a second layer 13' of silicon oxide, in turn covered with a silicon layer 14'. The circuits are produced within the silicon layer 14'. Then, for assembly to the second support 16', an adhesive is preferably chosen that produces a very thin layer 15, whilst having the highest possible mechanical strength at low temperature,

for example < 400°C, so as not to risk damaging the components of the active layer produced before this bonding step. These can advantageously be adhesives hardened by heat or by exposure to UV radiation (in this latter case, it is sufficient to choose a final substrate 16' that is transparent to UV) (see figure 19).

To lift off the demountable substrate (here at the bonding interface 12'/13'), it may appear difficult to produce purely chemical lift-off because adhesives and substrates transparent to UV (in practice made of quartz and glass) are not totally inert to the chemical products (hydrofluoric acid, solvents, *etc.*). On the other hand, a purely mechanical action may be sufficient to lift off the structure at the interface 12'/13' if the bonding energy at the demounting interface is made lower than the strength of the adhesive and the various layers constituting the integrated circuits (this can be achieved relatively easily). It is then possible to use the substrate 11' several times. To facilitate demounting, it may be advantageous to eliminate an outer ring of the substrate. Apart from limited chemical etching of the outer ring of the substrate, it is further possible to eliminate the ring by making a circular cut in the structure after adhesive bonding. The cutting can advantageously be effected by a laser (see figures 22 and 23).

As a general rule, the residue of the first substrate is obtained, the support of the substrate referred to until now as "demountable" (figure 20), and is reusable, preferably after polishing the layer 12' and the active layer 14', which is either transferred onto another support 16', as in figure 21, or free and self-supporting if the thickness of the layer 14' is appropriate.

Unlike the preceding examples, the second substrate 16' can instead be merely an intermediate substrate in a much longer process.

The structure shown in figure 21 can itself be a demountable structure. Production will then continue either with the pure and simple elimination of the intermediate substrate 16' or another layer transfer operation onto a yet further support, generally involving elimination of the substrate 16'. The demountable substrate obtained with the aid of the technique previously described is adhesive bonded to the intermediate substrate after it has been "processed". The intermediate substrate can be rigid or flexible (see the above examples). If it is rigid, it can even be a silicon wafer.

The use of adhesive films known to the person skilled in the art can be envisaged for the adhesive bonding, in particular for the operations of cutting silicon wafers and encapsulating integrated circuits or packaging or back-ending ("Blu-Tack®", Teflon® adhesive film, *etc.*). If the adhesive film is double-sided, it may be as well to stick an intermediate substrate to the rear face of the film, to act as a substrate or support for stiffening the assembly at cutting time.

The lift-off techniques that can be envisaged include the application of traction and/or shear and/or bending forces. It may be as well to combine the application of force with chemical etching of the interface, or other means, such as ultrasound. If the interface to be lifted off is of the oxide type, etching of the low energy interface is facilitated at the bonding interface and this encourages the transfer of the processed layer to the intermediate substrate. Under these conditions, it is advantageous for the processed layers to be protected (for example by an additional deposit of nitride in the case of hydrofluoric acid etching).

The means for applying stresses can be mechanical (in particular by inserting a blade at the bonding interface), and/or use a lift-off tool (see WO 00/26000),

and/or a jet, or involve inserting a gas flow, as described in the document FR 2796491, and/or a liquid (see EP 0925888, EP 0989593). In the case of a gas flow (or even a liquid flow, for example a flow of hydrofluoric acid if the interface is of oxide), the demountable substrate can advantageously be prepared beforehand (for example by chemical etching) to feed the fluid locally to the bonding interface. This facilitates preferential lifting off at the multilayer structure bonding interface, where the lifting off must take place, while protecting the various layers of the structure incorporating the components. Thus it is possible to lift off the bonding interface even when the adhesion between the internal component layers is weak.

The intermediate substrate, which is sometimes referred to as a "handle", can then be cut, totally or in part (to form notches or cutting precursors), into elements corresponding to the electronic components, and which can be transferred to different supports. The transfer can be collective, in which case all of the components, even if they are interconnected only by a support, are transferred at the same time in the same technological operation, or component by component (or die by die), if the latter are transferred one after the other. The supports can be of plastics material, as in the case of a smart card, and in this case an adhesive is advantageously used for the transfer. The elements can also be transferred onto a wafer incorporating other electronic or optoelectronic devices, in which case the transfer can again use a molecular adhesion technique (see figures 1 to 5, imagining the additional presence of components formed in the layer (14)). The elements can be transferred by conventional means such as pick and place means. The elements can also be transferred onto another support to improve the thermal properties, for example.

Then, by applying stress or localized heating (for

example using a laser), the thin layer, previously bonded to its final support, can be demounted (element by element, or globally) from its handle by means of mechanical forces.

As opposed to embodiments of the method according to the invention that tend to encourage demounting of the layer from its substrate at the global level, i.e. on the scale of the whole of the substrate, others tend to delimit fragments, the shape of which is clearly related to the dies or components to be produced from the active layer. One interesting variant consists in using conventional component cutting techniques (sawing, laser cutting, *etc.*) to cut or delimit trenches, at least partially around dies, fragments, *etc.* Another beneficial variant is based on the use of chemical etching associated with a photolithography operation to produce identical trenches and/or to remove the connecting region at the contour of the dies. For example, after preparing molecular adhesion bonding over a large area, only layers 3 and 4 are cut (figure 16) to the contour shown, after which each fragment is lifted off the substrate, which amounts to considering that the substrate is lifted off each fragment (as an alternative, all the layers or all of the fragments can be cut at one and the same time).

Of course, the embodiments previously described are not limited to the single case of monocrystalline silicon, and can be extended to many materials, such as other semiconductor materials (Ge, SiGe, SiC, GaN and other equivalent nitrides, AsGa, InP, *etc.*), ferroelectric and piezoelectric materials ($LiNbO_3$, $LiTaO_3$), and magnetic materials, whether components are produced before demounting or not.

As already mentioned, for the situation of a demountable substrate consisting of a surface layer of germanium having an SiO_2-SiO_2 bonding interface that has to be subjected to an epitaxial growth temperature of 550°C

(as is typical in the case of growing GaInAs to constitute a solar cell for use in space), the rms roughness should advantageously be 0.4 nm for the substrate to be demountable.

Another example (figures 24 to 29) is that of epitaxially growing an epitaxial stack on a demountable substrate (figure 24). This applies in particular to the production of blue and white LEDs and thin layer laser diodes (for example, for improved extraction of the light emitted or improved evacuation of heat, thanks to transfer onto a substrate that is a good conductor of heat, such as copper or diamond). In this case, the epitaxial stack concerned (figure 25) is based on composite semiconductors derived from GaN (AlN, GaAlN, GaAlInN, *etc.*). One method consists of using one of the processes previously described to form a demountable structure equivalent to that of figure 1 (or the like figures previously cited) in which the layer (14) is of SiC_6H (the transferred Si face is at the top in the figures), the layers (12) and (13) are of silicon oxides, as in the figure 1 example, and the substrate (11) is of polycrystalline SiC (or sapphire). The stack based on nitrides is grown epitaxially on this structure. The epitaxial techniques used can be those well known to the person skilled in the art, for example, such as molecular beam epitaxy (MBE) for one category, and metallo-organic chemical vapor deposition (MOCVD) for another category. In the former case, the epitaxial growth temperatures rarely exceed 600°C, whereas the typical temperatures for the second category can be as high as 1 100°C. For each of the above two techniques, the choice of parameters related to the mechanical strength of the bonding interface (roughening, strengthening by heat treatment, hydrophilic properties, *etc.*) must be optimized. In the second case, one of the processes previously described based on roughening of the two oxide layers (12)

and (13) by hydrofluoric acid etching is chosen, for example. Subsequent MOCVD epitaxial growth on this structure at 1 100°C produces a stack whose thickness is of the order of 1 μm. The structure is optionally annealed before the epitaxial growth stage, typically in the temperature range from 900 to 1 200°C, in order to consolidate strongly the mechanical strength of the ring. After the growth step, the assembly is subjected to deposition of oxide, planarization by CMP, and where applicable molecular adhesion bonding of a substrate 16 (for example onto a silicon substrate), and annealing at 1 100°C to strength this latter bonding. Finally, the demountable substrate is demounted at the bonding interface (figure 27). A preliminary step consisting of a few hours in a 50% hydrofluoric acid bath is advantageously sufficient to etch the oxide layer laterally to a depth of a few millimeters from the edges of the substrate. This is followed by demounting by means of mechanical forces, for example by inserting a blade, applying a pressurized water jet, or applying a compressed air jet, using the techniques previously described, for example, yielding what is shown in figure 28. A final deoxidation step removes the residue of the oxide layer (13). At least the SiC layer 14 that served as a nucleation layer for the epitaxial stack can optionally be eliminated by etching (figure 29). Diodes can be produced before or after the final transfer.

Note that, according to the invention, an alternative to roughening or modifying the hydrophilic properties is to use low temperatures for annealing the bonding interface, instead of the traditional temperatures of approximately 1 100 to 1 200°C in the case of bonding where the surfaces are not necessarily roughened. The annealing temperatures are advantageously optimized to obtain a bonding energy sufficient for the components but sufficiently low to allow demounting at the required time.

In accordance with one aspect of the invention that is original in its own right, there is, after production of the interface, and an optional technological production step (production of homogeneous or nonhomogeneous structures, complete or partial production of components, epitaxial growth, *etc.*), lifting off with chemical etching and/or application of mechanical forces, for example by jets of air or other fluids, localized to the bonding interface of the demountable substrate.

The inventors have thus demonstrated that roughening or modification of the hydrophilic properties of the surfaces can produce demountable bonding interfaces, even after annealing at high temperatures, up to 1 100°C. By judiciously combining the roughening preparation before bonding with suitable thermal annealing treatments, it has been shown that demountable SOI substrates can withstand, without untimely demounting at the assembly interface, most of the steps of a method for the production of CMOS transistors (including in particular heat treatment steps at high temperatures, typically 1 100°C, as well as steps of depositing constrained layers, for example of nitride), and could *a posteriori* be demounted at the bonding interface by the intentional application of controlled mechanical stresses. This has also been demonstrated for other applications, relating, for example, to the execution of an epitaxial deposition step before demounting the substrate.

CLAIMS

1. A method of producing a demountable structure by molecular adhesion bonding of one face of a first wafer to one face of a second wafer, which method includes, prior to bonding, a step of treating at least one of said faces to produce a controlled level of mechanical strength of the interface between the two wafers compatible with the production on at least one of the two wafers of a part or the whole of components and likewise compatible with subsequent demounting of the structure.

2. A method according to claim 1, characterized in that the treatment step includes a step of modifying the roughness and/or the hydrophilic properties of at least one of the faces.

3. A method according to claim 2, characterized in that the step of modifying the roughness consists in a step of increasing the roughness.

4. A method according to claim 3, characterized in that the step of increasing the roughness of one face includes localized chemical etching of said face.

5. A method according to claim 4, characterized in that the chemical etching is acid etching.

6. A method according to claim 5, characterized in that the acid etching is carried out using hydrofluoric acid.

7. A method according to any one of claims 1 to 6, characterized in that a thin layer is produced in at least one of the two wafers.

8. A method according to claim 7, characterized in that the thin layer is obtained by chemical and/or mechanical thinning of a wafer.

9. A method according to claim 7, characterized in that the thin layer is obtained by fracturing a buried weak region of one wafer.

10. A method according to claim 9, characterized in

that the buried weak region is obtained by implanting gaseous substances.

11. A method according to any one of claims 1 to 10, characterized in that the step of producing the structure is followed by a step of demounting the structure at the bonding interface.

12. A method according to claim 11, characterized in that the demounting step is carried out by chemical etching and/or application of thermal stresses and/or application of mechanical forces.

13. A method according to claim 11 or claim 12, characterized in that at least one of the wafers is cut into at least one element before lifting off.

14. A method according to claim 13, characterized in that the demounting is carried out element by element.

15. A method according to any one of claims 11 to 14, characterized in that, between the step of producing the structure and the demounting step, a second bonding step is effected during which the structure is bonded to a substrate (16, 16') at the level of its thin layer.

16. A method according to claim 15, characterized in that said bonding step includes molecular adhesion bonding.

17. A method according to claim 15, characterized in that said bonding step includes adhesive bonding.

18. A method according to claim 17, characterized in that said adhesive bonding is carried out using an adhesive hardened by UV radiation.

19. A method according to any one of claims 15 to 18, characterized in that the step of lifting off the substrate is effected by chemical etching and/or application of mechanical and/or thermal and/or photonic stresses.

20. A method according to any one of claims 1 to 19, characterized in that, between the step of producing the structure and the demounting step, a step is effected of

producing all a part or the whole of microelectronic, optoelectronic, mechanical, piezoelectric, superconductor, or magnetic components.

21. A method according to any one of claims 1 to 20, characterized in that, after demounting the structure, at least one of the wafers is used again.

22. A method according to any one of claims 7 to 21, characterized in that the thin layer is a layer of semiconductor material.

23. A demountable structure comprising two wafers bonded together at respective surfaces by molecular adhesion, at least one of said surfaces having been treated to have a controlled roughness and/or controlled hydrophilic properties to obtain a chosen mechanical strength at the interface between the two wafers.

24. A structure according to claim 23, characterized in that each of the faces has been treated.

25. A structure according to either claim 23 or claim 24, characterized in that one of the wafers is a substrate and the other is a thin layer bonded to a second substrate (16, 16').

26. A structure according to claim 25, characterized in that said second substrate is molecular adhesion bonded.

27. A structure according to claim 25, characterized in that said second substrate is adhesive bonded.

28. A structure according to claim 27, characterized in that said adhesive bonding is effected using an adhesive which can be hardened by UV radiation.

29. A structure according to any one of claims 25 to 29 [sic], characterized in that the thin layer is a layer of semiconductor material.