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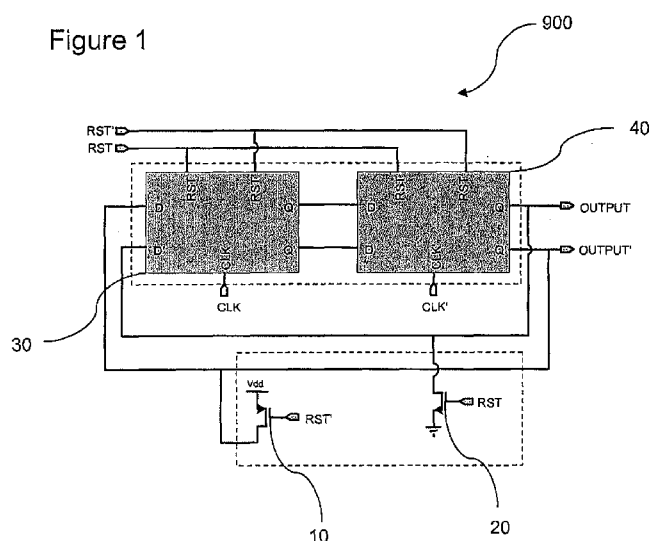
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- (54) Title:** A FREQUENCY DIVIDER

Figure 1



- (S7) Abstract:** There is disclosed a frequency divider, comprising: a clock input (CLK) adapted to receive a clock signal; a reset input (RST) adapted to receive a reset signal; a division circuit (30, 40) adapted to divide the clock signal by a factor to produce an output signal; an output adapted to output the output signal and a clock disable circuit connected to the reset input and the clock input. The clock disable circuit is controlled by the reset signal to disable the clock signal to the division circuit. A setting circuit (10, 20) is connected to the reset input and the output. The setting circuit (10, 20) is controlled by the reset signal to set the output signal to a designated state.