

ABSTRACT

MITIGATING DISTURBANCES OF MEMORY CELLS

Methods, systems, and devices for techniques to mitigate disturbances of unselected memory cells in a memory array during an access operation are described. A shunt line may be formed between a plate of a selected memory cell and a digit line of the selected memory cell to couple the plate to the digit line during the access operation. A switching component may be positioned on the shunt line. The switching component may selectively couple the plate to the digit line based on instructions received from a memory controller. By coupling the plate to the digit line during the access operation, voltages resulting on the plate by changes in the voltage level of the digit line may be reduced in magnitude or may be altered in type.

Figure 1