CLAIMS

1. A synchronization signal generating circuit for generating a synchronization signal for M node groups, each of the node groups comprising at least two nodes, and M being an integer greater than 1, wherein

the synchronization signal generating circuit comprises: a synchronization signal generating unit and M group ready signal generating units;

the M group ready signal generating units are in one-to-one correspondence with the M node groups;

a first group ready signal generating unit of the M group ready signal generating units is connected to K nodes in a first node group to be synchronized, wherein the first group ready signal generating unit is for generating a first to-be-started signal for the first node group to be synchronized, and K is an integer greater than 1;

output terminals of the M group ready signal generating units are connected to the synchronization signal generating unit; and

the synchronization signal generating unit generates a first synchronization signal based on the first to-be-started signal, wherein the first synchronization signal is for instructing the K nodes in the first node group to start synchronization;

wherein the synchronization signal generating unit comprises: M shielding units, M to-be-synchronized group indicating units, and M group synchronization signal generating units;

the M to-be-synchronized group indicating units are respectively connected to the M shielding units;

an input terminal of each of the M shielding units is connected to the output terminals of the M group ready signal generating units;

output terminals of the M shielding units are respectively connected to corresponding units of the M group synchronization signal generating units;

a first shielding unit of the M shielding units outputs a first group quasi-synchronization signal based on an instruction from a first to-be-synchronized group indicating unit connected to the first shielding unit; and

a first group synchronization signal generating unit of the M group synchronization signal generating units generates a first group synchronization signal based on the first group quasi-synchronization signal;

wherein each to-be-synchronized group indicating unit comprises a register; and

the register comprises at least M register bits, the M register bits are in one-to-one correspondence with the M node groups, and a register bit in the M register bits corresponding to the first node group to be synchronized is configured as a first value, and register bits in the M register bits corresponding to node groups in the M node groups other than the first node group to be synchronized are configured as a second value.

2. The synchronization signal generating circuit according to claim 1, wherein the first group ready signal generating unit is for generating the first to-be-started signal based on ready signals from all K nodes in the first node group to be synchronized.

3. The synchronization signal generating circuit according to claim 1 or 2, wherein the first synchronization signal is for instructing the K nodes in the first node group to start computing simultaneously, or to start transmitting data simultaneously.

4. A chip, comprising: a synchronization signal generating circuit according to any one of claims 1-3 and N processing nodes, wherein the N processing nodes are divided into M processing node groups, N is an integer greater than 1, and M is less than or equal to N.

5. The chip according to claim 4, wherein the chip further comprises N first communication hardware lines for transmitting ready signals from the N processing nodes to corresponding group ready signal generating units.

6. The chip according to claim 5, wherein the chip further comprises N second communication hardware lines for transmitting synchronization signals from the synchronization signal generating unit to corresponding processing nodes.

7. The chip according to any one of claims 4-6, wherein the chip further comprises a control unit for changing settings of a register.

8. The chip according to any one of claims 4-7, wherein the chip further comprises a control unit for controlling execution and allocation of tasks for each of processing nodes in a processing node group.

9. The chip according to any one of claims 4-8, wherein the N processing nodes comprise RISC-V cores.

10. A synchronous parallel processing control method based on a multi-core architecture, being a synchronous parallel processing control method based on a synchronization signal generating circuit according to any one of claims 1-3, the method comprising:

sending, by a first node, a ready signal to a group ready signal generating unit to which the first node is connected, when the first node in the node group enters an idle state;

generating, by the group ready signal generating unit, a to-be-started signal in response to a state that all nodes in the node group have sent ready signals;

generating, by a synchronization signal generating unit, a synchronization signal based on the to-be-started signal; and

starting synchronization, by all nodes in the node group, in response to the synchronization signal received.

11. A synchronous parallel processing device based on a multi-core architecture, comprising:

a processing module, which has N processing nodes, wherein the N processing nodes are divided into M processing node groups, N is an integer greater than 1, and M is less than or equal to N; and

a synchronization signal generating module, which comprises a synchronization signal generating unit and M group ready signal generating units; wherein the M group ready signal generating units are in one-to-one correspondence with the M node groups; a first group ready signal generating unit of the M group ready signal generating units is connected to K nodes in a first node group to be synchronized, wherein the first group ready signal generating unit is for generating a first to-be-started signal for the first node group to be synchronized, and K is an integer greater than; output terminals of the M group ready signal generating units are connected to the synchronization signal generating unit; and the synchronization signal generating unit generates a first synchronization signal based on the first to-be-started signal, wherein the first synchronization signal is for instructing the K nodes in the first node group to start synchronization;

wherein the synchronization signal generating unit comprises: M shielding units, M to-be-synchronized group indicating units, and M group synchronization signal generating units; the M to-be-synchronized group indicating units are respectively connected to the M shielding units; an input terminal of each of the M shielding units is connected to the output terminals of the M group ready signal generating units; output terminals of the M shielding units are respectively connected to corresponding units of the M group synchronization signal generating units; a first shielding unit of the M shielding units outputs a first group quasi-synchronization signal based on an instruction from a first to-be-synchronized group indicating unit connected to the first shielding unit; and a first group synchronization signal generating unit of the M group synchronization signal generating units generates a first group synchronization signal based on the first group quasi-synchronization signal;

wherein each to-be-synchronized group indicating unit comprises a register; and the register comprises at least M register bits, the M register bits are in one-to-one correspondence with the M node groups, and a register bit in the M register bits corresponding to the first node group to be synchronized is configured as a first value, and register bits in the M register bits corresponding to node groups in the M node groups other than the first node group to be synchronized are configured as a second value.

12. The synchronous parallel processing device according to claim 11, wherein the processing node is at least one of: a processing circuit, a processor, a processing chip, and a server.

13. A computing device comprising a processor and a memory, wherein the processor is configured to execute computer instructions stored in the memory, so that the computing device executes the synchronous parallel processing control method according to claim 10.

14. A computer readable storage medium storing a computer program which, upon execution by a processor, implements the steps of the synchronous parallel processing control method according to claim 10.

15. A computer program product comprising computer instructions which, upon execution by a computing device, cause the computing device to execute the synchronous parallel processing control method according to claim 10.