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# WAFER AND METHOD OF WORKING THE SAME

The present invention relates to a wafer and a method of working the same. It is applicable, for example, to semiconductor wafers.

In general, semiconductor devices such as transistors, integrated circuits (ICs) or large-scale integrated circuits (LSIs) are made from a wafer, which is a substantially circular flat member made of a semiconductor material such as silicon (Si). If foreign matter such as dust, chippings, etc. adhere on the surface of the wafer during processes such as diffusion, coating with a resist, etching and evaporation, they form causes for scratches in the wafer surface and for defects such as an ununiform film thickness and drawbacks arising during transportation.

There are various causes for the appearance of such foreign matter. As one of the causes, it has been known that, during the transportation of wafers by way of example, the outer peripheral part of the wafer collides against any transport mechanism or the wafers come

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into contact with each other, whereby the outer peripheral part of the wafer itself breaks off locally. Chippings due to the breakage adhere on the surface of the wafer as foreign matter, and cause various defects. Heretofore, in order to prevent the aforementioned breakage of the outer peripheral part of the wafer, both the major surfaces of the wafer outer-peripheral part have been chamfered by mechanical or chemical means (refer to Japanese Patent Application Publication No. 53-38594).

The inventors, however, have found out that, even when both the major surfaces of the wafer outer-peripheral part are chamfered in this manner, the wafer chips frequently.

The inventors earnestly researched into the cause of such chipping. As a result, important facts to be described below have been revealed. In general, a wafer is formed with a flat portion called the "orientation flatness (principal flatness)" by cutting a part of the wafer rectilinearly, in order to indicate the crystal orientation of the wafer and also to position the wafer. The formation of such flat portion, however, results in forming acute corners at the junction between the flat portion and the contour of the peripheral edge of the wafer. Consequently, the junction part is liable to chipping. That is, during the transportation of the wafer, the junction part collides against the guide of an air bearing or comes into contact with another wafer, whereby this junction part

breaks off to give rise to chipping.

As described above, the acute corners are formed in the junction parts between the flat portion (the orientation flatness) and the adjacent peripheral regions of the wafer. In this regard, the inventors have found that harmful phenomena occur in the regions of the acute corners, as stated below. In the processing of the wafer, when a photoresist film for a photolithographic process is formed on the surface of the wafer, crowns and fringes appear in the photoresist film. When a thin film such as an epitaxially vapor-grown layer is formed on the wafer surface, a film of abnormal thickness is formed due to, e.g. abnormal growth.

The present invention provides, in one aspect, a semiconductor wafer ready for the formation of a semiconductor device, having as seen in plan a periphery which generally is a circle with at least one periphery portion deviating inwardly from the said circle and chamfer-shaped portions of the periphery between said deviating portion and the adjacent portions conforming to said circle, said chamfer-shaped portions deviating inwardly from the circle so as at least partly to smooth the acuteness of the transition from the circle to the deviating portion, said inwardly deviating portion and said chamfer-shaped portions having been formed by removal of material.

The present invention provides, in a second aspect, a method of working a semiconductor wafer to provide a wafer in accordance with the invention as described above, including the step of removing material from the wafer in order to form said inwardly deviating periphery portion of the wafer and chamfering the junction regions between said inwardly deviating periphery portion and the periphery portions adjacent thereto to provide said chamfer-shaped portions.

This invention can best be understood by reference to the following description taken in connection with

the accompanying illustrative drawings, wherein:

Figure 1 is a plan view showing a semiconductor wafer which is an embodiment of the present invention;

Figure 2 is a sectional view taken along line II - II in Figure 1;

Figure 3 is an enlarged view of Figure 2;

Figure 4 is an explanatory view for elucidating the positioning of wafers;

Figure 5 is a plan view for explaining the determination of chamfer regions in the wafer shown in Figures 1 to 3;

Figure 6 is a plan view of another embodiment of wafer according to the present invention;

Figure 7 is a plan view showing still another embodiment of the present invention;

Figure 8 is a sectional view taken along line VIII-VIII in Figure 7; and

Figures 9 to 17 are schematic views showing three examples of chamfering devices which can be used for performing a method of working a wafer according to the present invention.

Now, the present invention will be described in detail in connection with embodiments illustrated in the drawings.

Figure 1 is a plan view showing an embodiment of a wafer according to the present invention, Figure 2 is a sectional view taken along line II - II in Figure 1, and Figure 3 is an enlarged view of Figure 2.

The wafer 1 of this embodiment has a circular shape prepared by, for example, slicing an ingot of silicon (Si) whose sectional shape is substantially circular. In a part of the wafer 1, a principal flatness (flat) or orientation flatness or orientation flat (O. F.) 2 is formed rectilinearly, and provides a cut-away positioning portion for indicating the direction of a crystal axis and for positioning the wafer 1 in various processing steps.

As seen from Figure 3, the outer peripheral portion 3 of the wafer 1 is chamfered , e.g. so as to be arcuate.

Further, according to the wafer 1 of this embodiment, in the junction parts 4 between the two ends of the orientation flatness 2 and the contour of the wafer 1, corner regions indicated by two-dot chain lines are chamfered into the shape of circular arcs indicated by solid lines. Owing to such structure, the wafer 1 is so constructed that the corner regions of the junction parts 4 are prevented from chipping during the various processing of the wafer 1, the chipping causing defects such as the appearance of foreign matters in the form of broken chipping pieces.

More specifically, each of the chamfered regions 5 of the joint parts 4 in the embodiment of Figure 1 is a region enclosed by the solid line and the two-dot chain line. The inner edge of the chamfered region 5 is defined by the circular arc of a common inscribed circle which is inscribed to the contour of the wafer 1 and the orientation flatness 2.

When performing the arcuate chamfering of the junction part 4, the preferable chamfer range of the chamfered region 5 is determined in a way to be described in detail below with reference to Figures 4 and 5.

The wafers 1 are usually positioned by rotating them while the peripheries of the wafers are held in touch with a roller 6. Herein, the phenomenon is exploited in which when the orientation flatness of the wafer 1 has moved up to the roller 6, the wafer 1 stops rotating owing to the flatness of this orientation flatness.

When the circular periphery of the wafer is in contact with the roller, the wafer is rotated along with the rotation of the roller. With the orientation flatness, however, even when the wafer and the roller lie in contact, the turning effort of the roller does not contribute to the rotation of the wafer. Thus, in spite of the rotation of the roller, the wafer stops rotating and moving and holds its state.

Shown in Figure 4 is an example of such expedient.

A wafer jig 100 receiving a large number of wafers 1 is placed on a positioning rest 101 which has two rollers 6. When the rollers 6 are subsequently rotated, the wafers 1 received in the wafer jig 100 start rotating. When the orientation flatness portions of the respective wafers have moved up to the positions of the rollers 6, the wafers do not rotate any longer. Such state is established for all the wafers. Eventually, all the wafers are aligned in the state in which the orientation flatness portions of the respective wafers are located on the lower side.

In executing such positioning, regulation or alignment of the wafers, there are various methods other than the aforementioned one, such as a method employing a single roller and a method resorting to optical means composed of photoelectric elements etc.

Referring to Figure 5, a wafer 1 having a thickness W as shown in Figure 3 has a radius R, and its center is $O_1$. The distance from the center $O_1$ to the orientation flatness 2 of the wafer is denoted by $\underline{y}$. When a perpendicular is drawn from the center $O_1$ down to the orientation flatness 2, the point of intersection P is supposed to be the middle point of the orientation flatness 2. Denoted by $\underline{b}$ is the distance between the midpoint of the orientation flatness 2 before chamfering (namely,

the point P) and a junction part 4 between the orientation flatness 2 and the contour of the wafer 1.

It is stipulated in SEMI standards that the relationship between the length of the orientation flatness 2, the width W of the wafer 1 and the diameter D = 2R of the wafer 1 should be as indicated in Table 1 in the mirror wafer state.

Table 1

| Diameter of Wafer | 3 inches | 100 mm | 125 mm | 150 mm |
|---|---|---|---|---|
| Allowable Range of Diameter (mm) | 75.56 - 76.84 | ± 1 | ± 1 | ± 1 |
| Width (μm) | 360 - 410 | 500 - 550 | 600 - 650 | 650 - 700 |
| Length of Orientation Flatness | 19.05 - 25.40 | 30 - 35 | 40 - 45 | 55 - 60 |

On the other hand, since the wafers 1 need to be positioned by utilizing the orientation flatnesses 2, the orientation flatness 2 has that length of the flat portion which must be possessed, at the minimum, for accurate positioning. Letting a denote one half of such length, the length a is the distance from the point P to the point of inscription $i_1$ between a common inscribed circle and the orientation flatness 2. Numeral 6 designates a roller for the positioning. It is as stated before that photoelectric elements etc. other than the roller may well be used as the positioning means.

Letting $i_2$ denote the point of inscription between the common inscribed circle and the contour of the wafer 1, the center $O_2$ of the common inscribed circle lies on a straight line which connects the center $O_1$ of the wafer 1 and the point of inscription $i_2$. The angle between this straight line and the straight line $\overline{O_1P}$ is expressed by $\theta$.

Accordingly, the radius $\underline{r}$ of the common inscribed circle which is inscribed to both the contour of the wafer 1 and the orientation flatness 2 is obtained as stated below.

First, the minimum required length for the positioning by the rollers 6, namely, the length $\underline{a}$ ($a = \overline{Pi_1}$) of that flat portion in the orientation flatness 2 which is not chamfered is given by:

$$a = (R - r) \sin \theta \qquad \cdots\cdots(1)$$

Secondly, the length $\underline{y}$ of the perpendicular $\overline{O_1P}$ drawn from the center $O_1$ of the wafer 1 to the orientation flatness 2 is given by:

$$y = (R - r) \cos \theta + r \qquad \cdots\cdots(2)$$

From a right-angled triangle $O_1P4$, $y^2 = R^2 - b^2$ holds. Therefore,

$$y = \sqrt{R^2 - b^2} \qquad \cdots\cdots(3)$$

Substituting Equation (3) into Equation (2),

$$\sqrt{R^2 - b^2} = (R - r) \cos \theta + r$$

$$\cos\theta = \frac{\sqrt{R^2 - b^2} - r}{(R - r)} \qquad \cdots\cdots(4)$$

From Equation (1),

$$\sin\theta = \frac{a}{(R - r)} \qquad \cdots\cdots(5)$$

Since $\sin^2\theta + \cos^2\theta = 1$, Equations (4) and (5) yield:

$$\frac{a^2}{(R - r)^2} + \frac{(\sqrt{R^2 - b^2} - r)^2}{(R - r)^2} = 1 \qquad \cdots\cdots(6)$$

Putting Equation (6) in order,

$$r = \frac{b^2 - a^2}{2\,(R - \sqrt{R^2 - b^2})} \qquad \cdots\cdots(7)$$

In the present embodiment, accordingly, the chamfer region 5 in the junction region between the contour of the wafer 1 and the orientation flatness 2 may be worked along a circular arc of any radius as long as this circular arc is the arc of the common inscribed circle of radius r in Equation (7) or falls within a region outside it, as indicated by oblique lines in Figure 5.

That is, the radius r of the inscribed circle common to both the contour line of the wafer 1 and the orientation flatness 2 may lie within a range given by the following expression, and the junction part may be arcuately chamfered within this range of radius r:

$$r \leqq \frac{b^2 - a^2}{2\,(R - \sqrt{R^2 - b^2})} \qquad \cdots\cdots(8)$$

On the other hand, the minimum value of the radius r in the chamfering can be set as stated below.

Figure 3 is an enlarged sectional view showing the silicon wafer which is one embodiment of the present invention. As shown in the figure, the silicon wafer 1 has the peripheral parts of both its major surfaces chamfered. The dimensions of the chamfering, namely, the length A of a slant face portion and the length B of an end face portion are stipulated from experimental values. It is experimentally indicated that the length B of the chamfer end face portion differs depending upon the thickness W of the wafer 1. It has been experimentally found that when the length B is at most 0.32 mm (320 μm) and at least 0.15 mm (150 μm) for W of 0.4 mm, the chipping of the peripheral part of the wafer exhibits the minimum value. It has been similarly found that the chipping of the peripheral part of the wafer exhibits the minimum value when 150 μm $\leqq$ B $\leqq$ 420 μm holds for W = 0.5 mm and when 150 μm $\leqq$ B $\leqq$ 520μm holds for W = 0.6 mm. That is, the chipping of the peripheral part of the wafer is minimized when the length B of the chamfer end face portion in the wafer periphery is at least 150 μm and at most a value obtained by subtracting 80 μm from the wafer thickness W, in other words, it falls within the range of 150 μm $\leqq$ B and B $\leqq$ (W − 80) μm. Thus,

in the chamfer dimensions of the silicon wafer 1 according to the present invention, the length B of the end face portion is set by the following expression, whereby the breakage and chipping of the wafer 1 attributed to mechanical shocks etc. during the processing or transportation of the wafer decrease extraordinarily:

$$150\ \mu m \leqq B \leqq (W - 80)\ \mu m \qquad \cdots\cdots(9)$$

On the other hand, the length A of the slant face portion in the chamfer dimensions of the silicon wafer 1 according to the present invention is experimentally set to be at least 0.2 mm (200 $\mu$m), whereby the breakage and chipping of the wafer 1 attributed to mechanical shocks etc. during the processing or transportation of the wafer can be reduced extraordinarily.

In view of the above and Figure 3, it is understood that the peripheral parts of both the major surfaces of the semiconductor wafer may be chamfered. Herein, the chamfering dimensions as to the sectional shape of the wafer may be such that the length B of the chamfer end face portion is set at a value within the range not smaller than 150 $\mu$m and not greater than the value obtained by subtracting 80 $\mu$m from the thickness of the wafer, while the length A of the chamfer slant face portion is rendered at least 200 $\mu$m.

Accordingly, the radius r of the inscribed circle

common to both the contour of the wafer 1 and the orientation flatness 2 may fall within a range given by the following expression, and the junction part may be chamfered arcuately within this range of radius r:

$$\frac{W - B}{2} \leqq r \qquad \cdots\cdots(10)$$

In conclusion, from Expressions (8) and (10), the chamfering radius r may lie within a range given by the following expression:

$$\frac{W - B}{2} \leqq r \leqq \frac{b^2 - a^2}{2\,(R - \sqrt{R^2 - b^2})} \qquad \cdots\cdots(11)$$

where r = radius of the wafer chamfering circle,

R = radius of the wafer,

a = half of the length of the unchamfered portion (flat portion) in the wafer cut-away portion,

b = half of the full length of the wafer cut-away portion before being chamfered,

W = thickness of the wafer,

B = length of the wafer end face portion.

In this manner, the wafer 1 according to the present invention is chamfered in the peripheral parts of the sliced silicon wafer with the predetermined dimensions and is thus smoothed so as not to protrude the corners. Therefore, it is difficult to break off. Moreover, even when an impact has acted on the wafer 1, a load

does not locally concentrate. Therefore, the strength of the peripheral part of the wafer increases, and the quantity of the chipping of the peripheral part can be reduced extraordinarily. It is accordingly possible to avoid the problem that silicon chippings float in the air as dust and that some of them adhere to the surface of the silicon wafer. In the wafer processing for producing a semiconductor device, therefore, a photoresist film in a photolithographic process can have the external appearance of its surface enhanced and have the lowering of its resolution prevented, and favorable vapor growth etc. free from any abnormal epitaxial growth can be effected. Further, since the chamfering dimensions are adapted to relieve the crowns and fringes of the photoresist and to enhance the resolution thereof, various patterns can be formed on the wafer by fine working.

According to the present embodiment, no acute corner exists in the junction region between the contour of the wafer 1 and the orientation flatness 2. It is therefore possible to prevent the junction region breaking off and developing chipping due to, for example, the collision against the guide of an air bearing or contact ' with another wafer during the transportation of the wafer 1. Besides the defect of the foreign matter ascribable to the appearance of such chipping pieces,

it is possible to conspicuously reduce defects such as inferior transportation attributed to the fact that the acute corner hitches on the guide of the air bearing, etc. during the transportation, and an inferior thickness of a resist film attributed to the fact that the thickness of the resist film disperses partially due to the turbulence of air current in the acute corner during the application of the resist. This is especially favorable for wafers of large diameter.

Figure 6 is a plan view which shows another embodiment of the wafer according to the present invention.

In this embodiment, the joint regions between the contour of a wafer 1 and an orientation flatness 2 are rectilinearly chamfered within the ranges of chamfer regions 5 indicated by oblique lines. In this case, the maximum chamfer range of the chamfer region 5 is defined by a straight line which connects the points of inscription $i_1$ and $i_2$ of an inscribed circle common to both the contour of the wafer 1 and the orientation flatness 2, as explained before with reference to Figure 5. The radius $r$ of the common inscribed circle can be selected within the same range as indicated by Expression (11).

With the present embodiment also, there is no acute corner in the junction part 4 between the contour of the wafer 1 and the orientation flatness 2,

so that the defect of the foreign matter due to the appearance of chipping pieces, the defect of the transportation, the defect of the thickness of a resist film, etc. can be sharply reduced.

The chamfering according to the present invention may be in any shapes other than the arcuate and rectilinear shapes in the foregoing embodiments, such as various curved shapes and polygonal shapes insofar as they can remove acute corners.

The present invention is applicable, not only to the case of providing the principal flatness or the orientation flatness, but also to a case of providing a sub flatness or a second flatness. In this case, as illustrated in Figures 7 and 8, the chamfer regions 5 of the junction regions between both the ends of the orientation flatness 2 and the contour of the wafer 1 are chamfered, and as in ranges indicated by symbol 5a, also the junction regions between each of the ends of the second flatness 7 and the contour of the wafer 1 are chamfered along the arcs of common inscribed circles inscribed to both the second flatness 7 and the contour of the wafer 1 or along straight lines connecting the points of inscription of the common inscribed circles, or in the regions outside them.

Further, the present invention is applicable to

a case where, besides the flat portions such as the orientation flatness 2 and the second flatness 7, a curved positioning notch is formed in the wafer 1 as exemplified by symbol 8 in Figure 7. In this case, the joint regions between each of the ends of the positioning notch 8 and the contour of the wafer 1 may be chamfered along the arcs of common inscribed circles inscribed to both the positioning notch 8 and the contour of the wafer 1 or along straight lines connecting the points of inscription of the common inscribed circles, or in the regions outside them, as in ranges indicated by symbol 5b.

The chamfering of the present invention may well be performed simultaneously with the formation of the orientation flatness 2, or with the chamfering of the outer peripheral part 3 in the thickness direction. Such simultaneous chamfering is very favorable from the point of view of the job efficiency, but separate chamfering may well be performed. Of course, the present invention does not always require the chamfering of the outer peripheral part 3 of the wafer 1 in the thickness direction.

Three examples of devices suitable for performing the chamfering are illustrated in Figures 9 to 17.

The chamfering device in Figures 9 to 13 belongs to the so-called shape profiling type. While a grindstone 8 having a rectilinear groove 9 is being rotated, it is moved in the horizontal direction and the vertical direction so as to perform chamfering. It can also perform the chamfering of the outer peripheral part of the wafer 1 in the thickness direction. In the illustrated device, numeral 102 designates a chuck mechanism for the wafer 1, and numeral 103 a chuck mechanism for the grindstone 8. They can rotate and can move vertically and horizontally, respectively.

The chamfering device in Figures 14 to 16 is of the so-called shape transfer type. While being rotated, a grindstone 10 having a curved groove 11 which is conformed to the shape of the chamfering of the outer peripheral part of the wafer 1 in the thickness direction is moved in the horizontal direction. Thus, the outer peripheral part of the wafer 1 can be chamfered as shown in Figures 1 to 3. Besides, the chamfer regions 5, 5a and 5b shown in Figures 5 to 8 can be chamfered.

In this manner, the chamfering devices in Figures 9 to 16 can perform both the chamfering of the chamfer regions 5, 5a, 5b and that of the outer peripheral part of the wafer 1. Therefore, these mechanical chamfering operations should efficiently be performed at the same

time, though they may well be executed individually.

The chamfering device in Figure 17 performs chamfering chemically. A rotary supporter 12 in which a large number of wafers 1 are sandwiched is immersed in a liquid etchant 14 (for example, a solution having a composition which consists of fluoric acid, nitric acid and glacial acetic acid at a volumetric ratio of 2 : 5 : 3) contained in an etching bath 13. While being rotated along with the rotary supporter 12, the wafers 1 have their outer peripheral parts etched by the liquid etchant 14. In this case, in order to chamfer only the chamfer regions 5, 5a and 5b, the other outer peripheral parts of the wafers 1 need to be masked so as not to touch the liquid etchant 14. However, the corners of the whole outer peripheries may well be chemically chamfered in the thickness direction by the liquid etchant after the chamfer regions 5, 5a and 5b have been formed by mechanical grinding in advance. In the case of Figure 17, mechanical shocks on the wafers 1 can be relieved.

The present invention is not restricted to wafers made of silicon (Si), but is also applicable to wafers made of germanium (Ge) or various compound semiconductor materials such as gallium arsenic (GaAs) and gallium garnet.

With the present embodiments set forth above,

no acute corner exists in the junction regions between the contour of the wafer and the cut-away portion of the wafer such as a removed portion for positioning. It is therefore possible to remarkably reduce defects ascribable to the existence of such acute corners, such as the defect of foreign matter due to the chipping of the wafer, the defect of transportation and the defect of the thickness of a resist film.

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CLAIMS

1. A semiconductor wafer ready for the formation of a semiconductor device, having as seen in plan a periphery which generally is a circle with at least one periphery portion deviating inwardly from the said circle and chamfer-shaped portions of the periphery between said deviating portion and the adjacent portions conforming to said circle, said chamfer-shaped portions deviating inwardly from the circle so as at least partly to smooth the acuteness of the transition from the circle to the deviating portion, said inwardly deviating portion and said chamfer-shaped portions having been formed by removal of material.

2. A wafer according to claim 1, wherein said inwardly deviating periphery portion of the wafer is an orientation flatness.

3. A wafer according to claim 1, wherein the wafer has two of said inwardly deviating periphery portions of which one is an orientation flatness and the other a portion for wafer positioning.

4. A wafer according to any one of the preceding claims, wherein the outlines of the chamfer shaped portions are arcs of inscribed circles common to the wafer circle and the inwardly deviating periphery portion or lie in regions outside such arcs.

5. A wafer according to claim 4, wherein the radius of each said inscribed circle is denoted by the following expression:

$$\frac{W - B}{2} \leq r \leq \frac{b^2 - a^2}{2\,(R - \sqrt{R^2 - b^2})}$$

wherein r = radius of the inscribed circle,
R = radius of the wafer,
a = half the length of an orientation flatness which forms said inwardly deviating periphery portion,
b = half the length of the orientation flatness before chamfering,
W = thickness of the wafer,
B = height of the peripheral face of the wafer.

6. A wafer according to any one of claims 1 to 3 wherein the outline of the chamfer shaped portions are straight lines respectively connecting points of inscription of inscribed circles common to the wafer circle and the inwardly deviating portions, or lie in regions outside such lines.

7. A semiconductor wafer substantially as herein described with reference to and as shown in Figs. 1 to 5, Fig. 6 or Figs. 7 and 8.

8. A method of working a semiconductor wafer to produce a wafer in accordance with any one of the preceding claims including the step of removing material from the wafer in order to form said inwardly deviating periphery portion of the wafer and chamfering the junction regions between said inwardly deviating periphery portion and the periphery portions adjacent thereto to provide said chamfer-shaped portions.

9. A method according to claim 8 wherein the chamfering of said junction regions is performed simultaneously with chamfering of an outer peripheral part of the wafer in a thickness direction.

10. A method of working a semiconductor wafer according to claim 8 substantially as any such method herein described with reference to the accompanying drawings.