SEMICONDUCTOR METHOD AND DEVICE OF FORMING A FAN-OUT POP DEVICE WITH PWB VERTICAL INTERCONNECT UNITS

Field of the Invention

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device and method of forming a fan-out package-on-package (Fo-PoP) with printed wiring board (PWB) modular vertical interconnect units.

Background of the Invention

Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), small signal transistor, resistor, capacitor, inductor, and power metal oxide semiconductor field effect transistor (MOSFET). Integrated semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor devices include microcontrollers, microprocessors, charged-coupled devices (CCDs), solar cells, and digital micro-mirror

devices (DMDs).

Semiconductor devices perform a wide range of functions such as signal processing, high-speed calculations, transmitting and receiving electromagnetic signals, controlling electronic devices, transforming sunlight to electricity, and creating visual projections for television displays. Semiconductor devices are found in the fields of entertainment, communications, power conversion, networks, computers, and consumer products. Semiconductor devices are also found in military applications, aviation, automotive, industrial controllers, and office equipment.

Semiconductor devices exploit the electrical properties of semiconductor materials. The atomic structure of semiconductor material allows its electrical conductivity to be manipulated by the application of an electric field or base current or through the process of doping. Doping introduces impurities into the semiconductor material to manipulate and control the conductivity of the semiconductor device.

A semiconductor device contains active and passive electrical structures. Active structures, including bipolar and field effect transistors, control the flow of electrical current. By varying levels of doping and application of an electric field or base current, the transistor either promotes or restricts the flow of electrical current. Passive structures, including resistors, capacitors, and inductors, create a relationship between voltage and current necessary to perform a variety of electrical functions. The passive and active structures are electrically connected to form circuits, which enable the semiconductor device to perform high-speed calculations and other useful functions.

Semiconductor devices are generally manufactured using

two complex manufacturing processes, i.e., front-end manufacturing, and back-end manufacturing, each involving potentially hundreds of steps. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each semiconductor die is typically identical and contains circuits formed by electrically connecting active and passive components. Back-end manufacturing involves singulating individual semiconductor die from the finished wafer and packaging the die to provide structural support and environmental isolation. The term "semiconductor die" as used herein refers to both the singular and plural form of the words, and accordingly, can refer to both a single semiconductor device and multiple semiconductor devices.

One goal of semiconductor manufacturing is to produce smaller semiconductor devices. Smaller devices typically consume less power, have higher performance, and can be produced more efficiently. In addition, smaller semiconductor devices have a smaller footprint, which is desirable for smaller end products. A smaller semiconductor die size can be achieved by improvements in the front-end process resulting in semiconductor die with smaller, higher density active and passive components. Back-end processes may result in semiconductor device packages with a smaller footprint by improvements in electrical interconnection and packaging materials.

One approach to achieving the objectives of greater integration and smaller semiconductor devices is to focus on three dimensional (3D) packaging technologies including PoP. However, PoP often require laser drilling to form interconnect structures, which increases equipment cost and requires drilling through an entire package thickness. Laser drilling increases

cycle time and decreases manufacturing throughput. Vertical interconnections formed exclusively by a laser drilling process can result in reduced control for vertical interconnections. Unprotected contacts can also lead to increases in yield loss for interconnections formed with subsequent surface mount technology (SMT). Furthermore, conductive materials used for forming vertical interconnects within PoP, such as copper (Cu), can incidentally be transferred to semiconductor die during package formation, thereby contaminating the semiconductor die within the package.

Summary of the Invention

A need exists for vertical interconnects in a Fo-PoP without laser drilling through the package. Accordingly, in one embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a carrier with a die attach area, mounting a first semiconductor die to the die attach area, mounting a modular interconnect unit over the carrier in a peripheral region around the first semiconductor die, depositing a first encapsulant over the carrier, first semiconductor die, and modular interconnect unit, removing a portion of the encapsulant to expose the first semiconductor die and modular interconnect unit, removing the carrier, and forming an interconnect structure over the first semiconductor die and modular interconnect unit.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a carrier, mounting a semiconductor die to the carrier, mounting a modular interconnect unit over the carrier in a peripheral region around the semiconductor die, depositing

an encapsulant over the carrier, semiconductor die, and modular interconnect unit, and removing a portion of the encapsulant to expose the modular interconnect unit and the semiconductor die.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a semiconductor die, disposing a modular interconnect unit in a peripheral region around the semiconductor die, and depositing an encapsulant over the semiconductor die and modular interconnect unit.

In another embodiment, the present invention is a semiconductor device comprising a semiconductor die. A modular interconnect unit is disposed in a peripheral region around the semiconductor die. An encapsulant is deposited around the semiconductor die and modular interconnect unit.

Brief Description of the Drawings

FIG. 1 illustrates a printed circuit board (PCB) with different types of packages mounted to its surface;

FIGs. 2a-2c illustrate further detail of the representative semiconductor packages mounted to the PCB;

FIGs. 3a-3c illustrate a semiconductor wafer with a plurality of semiconductor die separated by saw streets;

FIGs. 4a-4h illustrate a process of forming PWB modular units with vertical interconnect structures for a Fo-PoP;

FIGs. 5a-5i illustrate a process of forming a Fo-PoP with semiconductor die interconnected by PWB modular units having vertical interconnect structures;

FIGs. 6a-6r illustrate another process of forming a Fo-PoP with semiconductor die interconnected by PWB modular

units having vertical interconnect structures;

FIGs. 7a-7i illustrate various conductive vertical interconnect structures for PWB modular units;

FIGs. 8a-8c illustrate a process of forming a PWB modular unit with a vertical interconnect structures containing bumps;

FIG. 9 illustrates a Fo-PoP with semiconductor die interconnected by PWB modular units having vertical interconnect structures containing bumps;

FIG. 10 illustrates another Fo-PoP with semiconductor die interconnected by PWB modular units having vertical interconnect structures;

FIGs. 11a-11b illustrate mounting a second semiconductor die to the PWB modular unit;

FIGs. 12a-12b illustrate a process of forming modular units from an encapsulant panel with fine filler.

FIGs. 13a-13i illustrate another process of forming a Fo-PoP with a modular unit formed from an encapsulant panel without embedded conductive pillars or bumps;

FIG. 14 illustrates another Fo-PoP with a modular unit formed from an encapsulant panel without embedded conductive pillars or bumps;

FIGs. 15a-15b illustrate a process of forming modular units from a PCB panel; and

FIG. 16 illustrates another Fo-PoP with a modular unit formed from a PCB panel without embedded conductive pillars or bumps.

Detailed Description of the Drawings

The present invention is described in one or more embodiments in the following description with reference to the figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

Semiconductor devices are generally manufactured using two complex manufacturing processes: front-end manufacturing and back-end manufacturing. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die on the wafer contains active and passive electrical components, which are electrically connected to form functional electrical circuits. Active electrical components, such as transistors and diodes, have the ability to control the flow of electrical current. Passive electrical components, such as capacitors, inductors, resistors, and transformers, create a relationship between voltage and current necessary to perform electrical circuit functions.

Passive and active components are formed over the surface of the semiconductor wafer by a series of process steps including doping, deposition, photolithography, etching, and planarization. Doping introduces impurities into the semiconductor material by techniques such as ion implantation or thermal diffusion. The doping process modifies the electrical conductivity of semiconductor material in active devices,

transforming the semiconductor material into an insulator, conductor, or dynamically changing the semiconductor material conductivity in response to an electric field or base current. Transistors contain regions of varying types and degrees of doping arranged as necessary to enable the transistor to promote or restrict the flow of electrical current upon the application of the electric field or base current.

Active and passive components are formed by layers of materials with different electrical properties. The layers can be formed by a variety of deposition techniques determined in part by the type of material being deposited. For example, thin film deposition can involve chemical vapor deposition (CVD), physical vapor deposition (PVD), electrolytic plating, and electroless plating processes. Each layer is generally patterned to form portions of active components, passive components, or electrical connections between components.

The layers can be patterned using photolithography, which involves the deposition of light sensitive material, e.g., photoresist, over the layer to be patterned. A pattern is transferred from a photomask to the photoresist using light. In one embodiment, the portion of the photoresist pattern subjected to light is removed using a solvent, exposing portions of the underlying layer to be patterned. In another embodiment, the portion of the photoresist pattern not subjected to light, the negative photoresist, is removed using a solvent, exposing portions of the underlying layer to be patterned. The remainder of the photoresist is removed, leaving behind a patterned layer. Alternatively, some types of materials are patterned by directly depositing the material into the areas or voids formed by a previous deposition/etch process using techniques such as electroless and electrolytic plating.

Patterning is the basic operation by which portions of the top layers on the semiconductor wafer surface are removed. Portions of the semiconductor wafer can be removed using photolithography, photomasking, masking, oxide or metal removal, photography and stenciling, and microlithography. Photolithography includes forming a pattern in reticles or a photomask and transferring the pattern into the surface layers of the semiconductor wafer. Photolithography forms the horizontal dimensions of active and passive components on the surface of the semiconductor wafer in a two-step process. First, the pattern on the reticle or masks is transferred into a layer of photoresist. Photoresist is a light-sensitive material that undergoes changes in structure and properties when exposed to light. The process of changing the structure and properties of the photoresist occurs as either negative-acting photoresist or positive-acting photoresist. Second, the photoresist layer is transferred into the wafer surface. The transfer occurs when etching removes the portion of the top layers of semiconductor wafer not covered by the photoresist. The chemistry of photoresists is such that the photoresist remains substantially intact and resists removal by chemical etching solutions while the portion of the top layers of the semiconductor wafer not covered by the photoresist is removed. The process of forming, exposing, and removing the photoresist, as well as the process of removing a portion of the semiconductor wafer can be modified according to the particular resist used and the desired results.

In negative-acting photoresists, photoresist is exposed to light and is changed from a soluble condition to an insoluble condition in a process known as polymerization. In polymerization, unpolymerized material is exposed to a light or energy source and polymers form a cross-linked material that is

etch-resistant. In most negative resists, the polymers are polyisopremes. Removing the soluble portions (i.e., the portions not exposed to light) with chemical solvents or developers leaves a hole in the resist layer that corresponds to the opaque pattern on the reticle. A mask whose pattern exists in the opaque regions is called a clear-field mask.

In positive-acting photoresists, photoresist is exposed to light and is changed from relatively nonsoluble condition to much more soluble condition in a process known as photosolubilization. In photosolubilization, the relatively insoluble resist is exposed to the proper light energy and is converted to a more soluble state. The photosolubilized part of the resist can be removed by a solvent in the development process. The basic positive photoresist polymer is the phenol-formaldehyde polymer, also called the phenol-formaldehyde novolak resin. Removing the soluble portions (i.e., the portions exposed to light) with chemical solvents or developers leaves a hole in the resist layer that corresponds to the transparent pattern on the reticle. A mask whose pattern exists in the transparent regions is called a dark-field mask.

After removal of the top portion of the semiconductor wafer not covered by the photoresist, the remainder of the photoresist is removed, leaving behind a patterned layer. Alternatively, some types of materials are patterned by directly depositing the material into the areas or voids formed by a previous deposition/etch process using techniques such as electroless and electrolytic plating.

Depositing a thin film of material over an existing pattern can exaggerate the underlying pattern and create a non-uniformly flat surface. A uniformly flat surface is required to produce smaller and more densely packed active and passive

components. Planarization can be used to remove material from the surface of the wafer and produce a uniformly flat surface. Planarization involves polishing the surface of the wafer with a polishing pad. An abrasive material and corrosive chemical are added to the surface of the wafer during polishing. The combined mechanical action of the abrasive and corrosive action of the chemical removes any irregular topography, resulting in a uniformly flat surface.

Back-end manufacturing refers to cutting or singulating the finished wafer into the individual semiconductor die and then packaging the semiconductor die for structural support and environmental isolation. To singulate the semiconductor die, the wafer is scored and broken along non-functional regions of the wafer called saw streets or scribes. The wafer is singulated using a laser cutting tool or saw blade. After singulation, the individual semiconductor die are mounted to a package substrate that includes pins or contact pads for interconnection with other system components. Contact pads formed over the semiconductor die are then connected to contact pads within the package. The electrical connections can be made with solder bumps, stud bumps, conductive paste, or wirebonds. An encapsulant or other molding material is deposited over the package to provide physical support and electrical isolation. The finished package is then inserted into an electrical system and the functionality of the semiconductor device is made available to the other system components.

FIG. 1 illustrates electronic device 50 having a chip carrier substrate or PCB 52 with a plurality of semiconductor packages mounted on its surface. Electronic device 50 can have one type of semiconductor package, or multiple types of semiconductor packages, depending on the application. The

different types of semiconductor packages are shown in FIG. 1 for purposes of illustration.

Electronic device 50 can be a stand-alone system that uses the semiconductor packages to perform one or more electrical functions. Alternatively, electronic device 50 can be a subcomponent of a larger system. For example, electronic device 50 can be part of a cellular phone, personal digital assistant (PDA), digital video camera (DVC), or other electronic communication device. Alternatively, electronic device 50 can be a graphics card, network interface card, or other signal processing card that can be inserted into a computer. The semiconductor package can include microprocessors, memories, application specific integrated circuits (ASIC), logic circuits, analog circuits, RF circuits, discrete devices, or other semiconductor die or electrical components. Miniaturization and weight reduction are essential for these products to be accepted by the market. The distance between semiconductor devices must be decreased to achieve higher density.

In FIG. 1, PCB 52 provides a general substrate for structural support and electrical interconnect of the semiconductor packages mounted on the PCB. Conductive signal traces 54 are formed over a surface or within layers of PCB 52 using evaporation, electrolytic plating, electroless plating, screen printing, or other suitable metal deposition process. Signal traces 54 provide for electrical communication between each of the semiconductor packages, mounted components, and other external system components. Traces 54 also provide power and ground connections to each of the semiconductor packages.

In some embodiments, a semiconductor device has two packaging levels. First level packaging is a technique for mechanically and electrically attaching the semiconductor die to

an intermediate carrier. Second level packaging involves mechanically and electrically attaching the intermediate carrier to the PCB. In other embodiments, a semiconductor device may only have the first level packaging where the die is mechanically and electrically mounted directly to the PCB.

For the purpose of illustration, several types of first level packaging, including bond wire package 56 and flipchip 58, are shown on PCB 52. Additionally, several types of second level packaging, including ball grid array (BGA) 60, bump chip carrier (BCC) 62, dual in-line package (DIP) 64, land grid array (LGA) 66, multi-chip module (MCM) 68, quad flat non-leaded package (QFN) 70, and quad flat package 72, are shown mounted on PCB 52. Depending upon the system requirements, any combination of semiconductor packages, configured with any combination of first and second level packaging styles, as well as other electronic components, can be connected to PCB 52. In some embodiments, electronic device 50 includes a single attached semiconductor package, while other embodiments call for multiple interconnected packages. By combining one or more semiconductor packages over a single substrate, manufacturers can incorporate pre-made components into electronic devices and systems. Because the semiconductor packages include sophisticated functionality, electronic devices can be manufactured using less expensive components and a streamlined manufacturing process. The resulting devices are less likely to fail and less expensive to manufacture resulting in a lower cost for consumers.

FIGs. 2a-2c show exemplary semiconductor packages. FIG. 2a illustrates further detail of DIP 64 mounted on PCB 52. Semiconductor die 74 includes an active region containing analog or digital circuits implemented as active devices, passive

devices, conductive layers, and dielectric layers formed within the die and are electrically interconnected according to the electrical design of the die. For example, the circuit can include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements formed within the active region of semiconductor die 74. Contact pads 76 are one or more layers of conductive material, such as aluminum (Al), Cu, tin (Sn), nickel (Ni), gold (Au), or silver (Ag), and are electrically connected to the circuit elements formed within semiconductor die 74. During assembly of DIP 64, semiconductor die 74 is mounted to an intermediate carrier 78 using a gold-silicon eutectic layer or adhesive material such as thermal epoxy or epoxy resin. The package body includes an insulative packaging material such as polymer or ceramic. Conductor leads 80 and bond wires 82 provide electrical interconnect between semiconductor die 74 and PCB 52. Encapsulant 84 is deposited over the package for environmental protection by preventing moisture and particles from entering the package and contaminating semiconductor die 74 or bond wires 82.

FIG. 2b illustrates further detail of BCC 62 mounted on PCB 52. Semiconductor die 88 is mounted over carrier 90 using an underfill or epoxy-resin adhesive material 92. Bond wires 94 provide first level packaging interconnect between contact pads 96 and 98. Molding compound or encapsulant 100 is deposited over semiconductor die 88 and bond wires 94 to provide physical support and electrical isolation for the device. Contact pads 102 are formed over a surface of PCB 52 using a suitable metal deposition process such as electrolytic plating or electroless plating to prevent oxidation. Contact pads 102 are electrically connected to one or more conductive signal traces 54 in PCB 52. Bumps 104 are formed between contact pads

98 of BCC 62 and contact pads 102 of PCB 52.

In FIG. 2c, semiconductor die 58 is mounted face down to intermediate carrier 106 with a flipchip style first level packaging. Active region 108 of semiconductor die 58 contains analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed according to the electrical design of the die. For example, the circuit can include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements within active region 108. Semiconductor die 58 is electrically and mechanically connected to carrier 106 through bumps 110.

BGA 60 is electrically and mechanically connected to PCB 52 with a BGA style second level packaging using bumps 112. Semiconductor die 58 is electrically connected to conductive signal traces 54 in PCB 52 through bumps 110, signal lines 114, and bumps 112. A molding compound or encapsulant 116 is deposited over semiconductor die 58 and carrier 106 to provide physical support and electrical isolation for the device. The flipchip semiconductor device provides a short electrical conduction path from the active devices on semiconductor die 58 to conduction tracks on PCB 52 in order to reduce signal propagation distance, lower capacitance, and improve overall circuit performance. In another embodiment, the semiconductor die 58 can be mechanically and electrically connected directly to PCB 52 using flipchip style first level packaging without intermediate carrier 106.

FIG. 3a shows a semiconductor wafer 120 with a base substrate material 122, such as silicon, germanium, gallium arsenide, indium phosphide, or silicon carbide, for structural support. A plurality of semiconductor die or components 124 is formed on wafer 120 separated by a non-active, inter-die wafer

area or saw street 126 as described above. Saw street 126 provides cutting areas to singulate semiconductor wafer 120 into individual semiconductor die 124.

FIG. 3b shows a cross-sectional view of a portion of semiconductor wafer 120. Each semiconductor die 124 has a back surface 128 and active surface 130 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 130 to implement analog circuits or digital circuits, such as digital signal processor (DSP), ASIC, memory, or other signal processing circuit. Semiconductor die 124 may also contain integrated passive devices (IPDs), such as inductors, capacitors, and resistors, for RF signal processing.

An electrically conductive layer 132 is formed over active surface 130 using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 132 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 132 operates as contact pads electrically connected to the circuits on active surface 130. Conductive layer 132 can be formed as contact pads disposed side-by-side a first distance from the edge of semiconductor die 124, as shown in FIG. 3b. Alternatively, conductive layer 132 can be formed as contact pads that are in multiple rows such that a first row of contact pads is disposed a first distance from the edge of the die, and a second row of contact pads alternating with the first row is disposed a second distance

from the edge of the die.

An insulating or passivation layer 134 is conformally applied over active surface 130 using PVD, CVD, screen printing, spin coating, or spray coating. The insulating layer 134 contains one or more layers of silicon dioxide (SiO2), silicon nitride (Si3N4), silicon oxynitride (SiON), tantalum pentoxide (Ta2O5), aluminum oxide (Al2O3), or other material having similar insulating and structural properties. The insulating layer 134 covers and provides protection for active surface 130. A portion of insulating layer 134 is removed by laser direct ablation (LDA) using laser 136 or other suitable process to expose conductive layer 132 and provide for subsequent electrical interconnect.

In FIG. 3c, semiconductor wafer 120 is singulated through saw street 126 using a saw blade or laser cutting tool 138 into individual semiconductor die 124.

FIGs. 4a-4h and 5a-5i illustrate, in relation to FIGs. 1 and 2a-2c, a process of forming a Fo-PoP with PWB modular vertical interconnect units. FIG. 4a shows a cross-sectional view of a portion of laminate core 140. An optional conductive layer 142 is formed over surface 144 of core 140, and optional conductive layer 146 is formed over surface 148 of the core. Conductive layers 142 and 146 are formed using a metal deposition process such as Cu foil lamination, printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layers 142 and 146 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, titanium (Ti), tungsten (W), or other suitable electrically conductive material. In one embodiment, conductive layers 142 and 146 are Cu foil having a thickness of 20-200 micrometers (μm). Conductive layers 142 and 146 can be thinned by a wet etching process.

In FIG. 4b, a plurality of vias 150 is formed through laminate core 140 and conductive layers 142 and 146 using laser drilling, mechanical drilling, deep reactive ion etching (DRIE), or other suitable process. Vias 150 extend through laminate core 140. Vias 150 are cleaned by desmearing process.

In FIG. 4c, a conductive layer 152 is formed over laminate core 140, conductive layers 142 and 146, and sidewalls of vias 150 using a metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 152 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material. In one embodiment, conductive layer 152 includes a first Cu layer formed by electroless plating, followed by a second Cu layer formed by electrolytic plating.

In FIG. 4d, the remaining portion of vias 150 is filled with an insulating or conductive material with filler material 154. The insulating material with insulating filler can be polymer dielectric material with filler and one or more of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other material having similar insulating and structural properties. The conductive filler material can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. In one embodiment, filler material 154 can be a polymer plug. Alternatively, filler material 154 is Cu paste. Vias 150 can also be left as a void, i.e. without filler material. Filler material 154 is selected to be softer or more compliant than conductive layer 152. Vias 150 with filler material 154 reduce the incidence of cracking or delamination by allowing deformation or change of shape of conductive layer 152 under stress. Vias 150 can also be completely filled with conductive layer 152.

In FIG. 4e, a conductive layer 156 is formed over conductive layer 152 and filler material 154 using a metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 156 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material. In one embodiment, conductive layer 156 includes a first Cu layer formed by electroless plating, followed by a second Cu layer formed by electrolytic plating.

In FIG. 4f, a portion of conductive layers 142, 146, 148, 152, and 156 is removed by a wet etching process through a patterned photoresist layer to expose laminate core 140 and leave conductive pillars or conductive vertical interconnect structures 158 through laminate core 140. An insulating or passivation layer 160 is formed over laminate core 140 and conductive vertical interconnect structures 158 using vacuum lamination, spin coating, spray coating, screen printing, or other printing process. The insulating layer 160 contains one or more layers of polymer dielectric material with or without insulating filler of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other material having similar insulating and structural properties. A portion of insulating layer 160 is removed by an etching process or LDA to expose conductive layer 156 and facilitate the formation of subsequent conductive layers.

An optional conductive layer 162 can be formed over the exposed conductive layer 156 using a metal deposition process such as electrolytic plating and electroless plating. Conductive layer 162 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material. In one embodiment, conductive layer 162 is a Cu protective layer.

Laminate core 140 with vertical interconnect structures 158 constitute one or more PWB modular vertical interconnect units, which are disposed between semiconductor die or packages to facility electrical interconnect for a Fo-PoP. FIG. 4g shows a plan view of laminate core 140 organized into PWB modular units 164-166. PWB modular units 164-166 contain multiple rows of vertical interconnect structures 158 extending between opposing surfaces of the PWB units. PWB units 164-166 are configured for integration into Fo-PoP, and as such, differ in size one from another according to a final device configuration as discussed in more detail below. While PWB units 164-166 are illustrated in FIG. 4g as including square or rectangular footprints, alternatively, the PWB units can include cross-shaped (+), angled or "L-shaped," circular, oval, hexagonal, octagonal, star shaped, or any geometrically shaped footprint. FIG. 4h shows laminate core 140 singulated into individual PWB modular units 164 and 166 with saw blade or laser cutting tool 168.

FIG. 5a shows a cross-sectional view of a portion of a carrier or temporary substrate 170 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 172 is formed over carrier 170 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer.

PWB modular units 164-166 from FIGs. 4h are mounted to interface layer 172 and carrier 170 using a pick and place operation. After placing PWB units 164-166, semiconductor die 124 from FIG. 3c are mounted to interface layer 172 and carrier 170 using a pick and place operation with active surface 130 oriented toward the carrier. FIG. 5b shows semiconductor die

124 and PWB units 164-166 mounted to carrier 170 as a reconstituted wafer 174. Semiconductor die 124 extend above PWB units 164-166 by distance D1 greater than 1 μm, e.g. 1-150 μm. The offset between PWB units 164-166 and semiconductor die 124 reduces contamination during a subsequent backgrinding step.

In FIG. 5c, an encapsulant or molding compound 176 is deposited over semiconductor die 124, PWB units 164-166, and carrier 170 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 176 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 176 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.

In FIG. 5d, carrier 170 and interface layer 172 are removed by chemical etching, mechanical peeling, chemical mechanical polishing (CMP,) mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping to expose insulating layer 134, PWB units 164-166, and encapsulant 176.

In FIG. 5e, a build-up interconnect structure 180 is formed over semiconductor die 124, PWB units 164-166, and encapsulant 176. An insulating or passivation layer 182 is formed over semiconductor die 124, PWB units 164-166, and encapsulant 176 using PVD, CVD, lamination, printing, spin coating, or spray coating. The insulating layer 182 contains one or more layers of low temperature (less than 250°C) curing polymer dielectric with or without insulating fillers, like SiO2, Si3N4, SiON, Ta2O5, Al2O3, rubber particles, or other material having similar insulating and structural properties. A portion of insulating layer 182 can be removed by an etching

process to expose vertical interconnect structures 158 of PWB units 164-166 and conductive layer 132 of semiconductor die 124.

An electrically conductive layer or RDL 184 formed over insulating layer 182 using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 184 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. In one embodiment, conductive layer 184 contains Ti/Cu, TiW/Cu, or Ti/NiV/Cu. One portion of conductive layer 184 is electrically connected to contact pads 132 of semiconductor die 124. Another portion of conductive layer 184 is electrically connected to vertical interconnect structures 158 of PWB units 164-166. Other portions of conductive layer 184 can be electrically common or electrically isolated depending on the design and function of semiconductor die 124.

An insulating or passivation layer 186 is formed over insulating layer 182 and conductive layer 184 using PVD, CVD, lamination, printing, spin coating, or spray coating. The insulating layer 186 contains one or more layers of low temperature (less than 250°C) curing polymer dielectric with or without insulating fillers, like SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, rubber particles, or other material having similar insulating and structural properties. A portion of insulating layer 186 can be removed by an etching process to expose conductive layer 184.

An electrically conductive layer or RDL 188 formed over conductive layer 184 and insulating layer 186 using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 188 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. In one

embodiment, conductive layer 188 contains Ti/Cu, TiW/Cu, or Ti/NiV/Cu. One portion of conductive layer 188 is electrically connected to conductive layer 184. Other portions of conductive layer 188 can be electrically common or electrically isolated depending on the design and function of semiconductor die 124.

An insulating or passivation layer 190 is formed over insulating layer 186 and conductive layer 188 using PVD, CVD, printing, spin coating, or spray coating. The insulating layer 190 contains one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, or other material having similar insulating and structural properties. A portion of insulating layer 190 can be removed by an etching process to expose conductive layer 188.

The number of insulating and conductive layers included within build-up interconnect structure 180 depends on, and varies with, the complexity of the circuit routing design. Accordingly, build-up interconnect structure 180 can include any number of insulating and conductive layers to facilitate electrical interconnect with respect to semiconductor die 124.

An electrically conductive bump material is deposited over build-up interconnect structure 180 and electrically connected to the exposed portion of conductive layer 188 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 188 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form spherical balls or bumps 192. In some applications, bumps 192 are reflowed a second time to improve

electrical contact to conductive layer 188. An under bump metallization (UBM) can be formed under bumps 192. Bumps 192 can also be compression bonded to conductive layer 188. Bumps 192 represent one type of interconnect structure that can be formed over conductive layer 188. The interconnect structure can also use stud bump, micro bump, or other electrical interconnect.

In FIG. 5f, a portion of encapsulant 176 and semiconductor die 124 is removed by a grinding operation with grinder 194 to planarize the surface and reduce a thickness of the encapsulant. Encapsulant 176 remains over PWB units 164-166 with a thickness D2 of 1-150 μm between back surface 128 of semiconductor die and PWB units 164-166. In one embodiment, D2 is 100 μm. A chemical etch, CMP, or plasma dry etch can also be used to remove back grinding damage and residue stress on semiconductor die 124 and encapsulant 176 to enhance the package strength.

In FIG. 5g, a backside balance layer 196 is applied over encapsulant 176, PWB units 164-166, and semiconductor die 124. Backside balance layer 196 balances the coefficient of thermal expansion (CTE), e.g. 30-150ppm/K, of conductive layers 184 and 188 and reduces warpage in the package. In one embodiment, backside balance layer 196 has a thickness of 10-100 μm. Backside balance layer 196 can be any suitable balance layer with suitable thermal and structural properties, such as resin coated copper (RCC) tape.

In FIG. 5h, a portion of backside balance layer 196 and encapsulant 176 removed to expose vertical interconnect structures 158. Reconstituted wafer 174 is singulated through PWB modular unit 164 with saw blade or laser cutting tool 202 into separate Fo-PoP 204.

FIG. 5i shows Fo-PoP 210 with bumps 198 formed over the exposed vertical interconnect structures 158. Bumps 198 are disposed at least 1 μm below back surface 128 of semiconductor die 124. Alternatively, bumps 198 extend above backside balance layer 196 and can have a height of 25-67% of the thickness of semiconductor die 124.

PWB modular units 164-166 disposed within Fo-PoP 204 can differ in size and shape one from another while still providing through vertical interconnect for the Fo-PoP. PWB modular units 164-166 include interlocking footprints having square and rectangular shapes, a cross-shape (+), an angled or "L-shape," a circular or oval shape, a hexagonal shape, an octagonal shape, a star shape, or any other geometric shape. At the wafer level, and before singulation, PWB modular units 164-166 are disposed around semiconductor die 124 in an interlocking pattern such that different sides of the semiconductor die are aligned with, and correspond to, a number of different sides of the PWB units in a repeating pattern. PWB units 164-166 may also include additional metal layers to facilitate design integration and increased routing flexibility before build-up interconnect structure 180 is formed over the PWB units.

PWB modular units 164-166 provide a cost effective alternative to using standard laser drilling processes for vertical interconnection in Fo-PoP for a number of reasons. First, PWB units 164-166 can be made with low cost manufacturing technology such as substrate manufacturing technology. Second, standard laser drilling includes high equipment cost and requires drilling through an entire package thickness, which increases cycle time and decrease manufacturing throughput. Furthermore, the use of PWB units 164-166 for vertical interconnection provides an advantage of improved control for

vertical interconnection with respect to vertical interconnections formed exclusively by a laser drilling process.

In another embodiment, FIG. 6a shows a cross-sectional view of a portion of a carrier or temporary substrate 220 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 224 is formed over carrier 220 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer.

In FIG. 6b, semiconductor die 124 from FIG. 3c are mounted to interface layer 224 and carrier 220 using a pick and place operation with active surface 130 oriented toward the carrier. Semiconductor die 124 are pressed into interface layer 224 such that insulating layer 134 is disposed into the interface layer. When semiconductor die 124 is mounted to interface layer 224, a surface 225 of insulating layer 134 is separated by a distance D1 from carrier 220.

In FIG. 6c, PWB modular units 164-166 from FIG. 4h are mounted to interface layer 224 and carrier 220 using a pick and place operation. PWB units 164-166 are pressed into interface layer 224 such that contacting surface 226 is disposed into the interface layer. When PWB units 164-166 are mounted to interface layer 224, surface 226 is separated by a distance D2 from carrier 220. D2 may be greater than D1 such that surface 226 of PWB units 164-166 is vertically offset with respect to surface 225 of insulating layer 134.

FIG. 6d shows semiconductor die 124 and PWB modular units 164-166 mounted to carrier 220 as a reconstituted wafer 227. A surface 228 of PWB units 164-166, opposite surface 226, is vertically offset with respect to back surface 128 of

semiconductor die 124 by a distance of D3, e.g. 1-150 μm. By separating surface 228 of PWB units 166 and back surface 128 of semiconductor die 124 a subsequent backgrinding step is facilitated by preventing material from vertical interconnect structures 158, such as Cu, from contaminating a material of semiconductor die 124, such as Si.

FIG. 6e shows a plan view of a portion of reconstituted wafer 227 having PWB modular units 164-166 mounted over interface layer 224. PWB units 164-166 contain multiple rows of vertical interconnect structures 158 that provide through vertical interconnection between opposing sides of the PWB units. PWB units 164-166 are disposed around semiconductor die 124 in an interlocking pattern. PWB units 164-166 are disposed around semiconductor die 124 in such a way that different sides of the semiconductor die are aligned with, and correspond to, a number of different sides of the PWB units in a repeating pattern across reconstituted wafer 227. A plurality of saw streets 230 are aligned with respect to the semiconductor die and extend across PWB units 164-166 such that when reconstituted wafer 227 is singulated along the saw streets, each semiconductor die 124 has a plurality of vertical interconnect structures 158 from singulated PWB units 164-166 that are disposed around or in a peripheral region around the semiconductor die. While PWB units 164-166 are illustrated with interlocking square and rectangular footprints, the PWB units disposed around semiconductor die 124 can include PWB units having footprints with a cross-shape (+), an angled or "L-shape," a circular or oval shape, a hexagonal shape, an octagonal shape, a star shape, or any other geometric shape.

FIG. 6f shows a plan view of a portion of a reconstituted wafer 240 having cross-shaped (+) PWB modular

units 242 mounted over interface layer 224. PWB units 242 are formed in a process similar to PWB units 164-166 as shown in FIGs. 4a-4h. PWB units 242 contain multiple rows of vertical interconnect structures 244 that are similar to vertical interconnect structures 158, and provide through vertical interconnection between opposing sides of the PWB units. PWB units 242 are disposed around semiconductor die 124 in an interlocking pattern. PWB units 242 are disposed around semiconductor die 124 in such a way that different sides of the semiconductor die are aligned with, and correspond to, a number of different sides of the PWB units in a repeating pattern across reconstituted wafer 240. A plurality of saw streets 246 are aligned with respect to semiconductor die 124 and extend across PWB units 242 such that when reconstituted wafer 240 is singulated along the saw streets, each semiconductor die 124 has a plurality of vertical interconnect structures 244 from singulated PWB units 242 that are disposed around or in a peripheral region around the semiconductor die. Vertical interconnect structures 244 are disposed in one or more rows offset from a perimeter of the semiconductor die after singulation through saw streets 246.

FIG. 6g shows a plan view of a portion of a reconstituted wafer 250 having angled or “L-shaped” PWB modular units 252 mounted over interface layer 224. PWB units 252 are formed in a process similar to PWB units 164-166 as shown in FIGs. 4a-4h. PWB units 252 contain multiple rows of vertical interconnect structures 254 that are similar to vertical interconnect structures 158, and provide through vertical interconnection between opposing sides of the PWB units. PWB units 252 are disposed around semiconductor die 124 in an interlocking pattern. PWB units 252 are disposed around

semiconductor die 124 in such a way that different sides of the semiconductor die are aligned with, and correspond to, a number of different sides of the PWB units in a repeating pattern across reconstituted wafer 250. A plurality of saw streets 256 are aligned with respect to semiconductor die 124 and extend across PWB units 252 such that when reconstituted wafer 250 is singulated along the saw streets, each semiconductor die 124 has a plurality of vertical interconnect structures 254 from singulated PWB units 252 that are disposed around or in a peripheral region around the semiconductor die. Vertical interconnect structures 254 are disposed in one or more rows offset from a perimeter of the semiconductor die after singulation through saw streets 256.

FIG. 6h shows a plan view of a portion of a reconstituted wafer 260 having circular or oval shaped PWB modular units 262 and 263 mounted over interface layer 224. PWB units 262 and 263 are formed in a process similar to PWB units 164-166 as shown in FIGs. 4a-4h. PWB units 262 and 263 contain multiple rows of vertical interconnect structures 264 that are similar to vertical interconnect structures 158, and provide through vertical interconnection between opposing sides of the PWB units. PWB units 262 and 263 are disposed around semiconductor die 124 in an interlocking pattern. PWB units 262-263 are disposed around semiconductor die 124 in such a way that different sides of the semiconductor die are aligned with, and correspond to, a number of different portions of the PWB units in a repeating pattern across reconstituted wafer 260. A plurality of saw streets 265 are aligned with respect to semiconductor die 124 and extend across PWB units 262 and 263 such that when reconstituted wafer 260 is singulated along the saw streets, each semiconductor die 124 has a plurality of

vertical interconnect structures 264 from singulated PWB units 262 and 263 that are disposed around or in a peripheral region around the semiconductor die. Vertical interconnect structures 264 are disposed in one or more rows offset from a perimeter of the semiconductor die after singulation through saw streets 265.

FIG. 6i shows a plan view of a portion of a reconstituted wafer 266 having a continuous PWB or PCB panel 267 mounted over interface layer 224. PWB panel 267 is aligned with and laminated on interface layer 224 on temporary carrier 220. PWB panel 267 is formed in a process similar to PWB units 164-166 as shown in FIGs. 4a-4h, and is formed at panel scale, for example as a 300-325 millimeters (mm) round panel or 470 mm x 370 mm rectangular panel. The final panel size is about 5 mm to 15 mm smaller than final fan-out panel substrate size either in diameter or length or width. PWB panel 267 has a thickness ranging from 50-250 μm. In one embodiment, PWB panel 267 has a thickness of 80 μm. Multiple rows of vertical interconnect structures 268 that are similar to vertical interconnect structures 158 are formed through PWB panel 267 to separate individual PWB units 270. Vertical interconnect structures 268 are formed around a peripheral area of PWB units 270.

A central portion of each PWB unit 270 is removed by punching, etching, LDA, or other suitable process to form openings 271. Openings 271 are formed centrally with respect to the vertical interconnect structures 268 of each PWB unit 270 and are formed through PWB units 270 to expose interface layer 224. Openings 271 have a generally square footprint and are formed large enough to accommodate semiconductor die 124 from FIG. 3c. Semiconductor die 124 are mounted to interface layer 224 within openings 271 using a pick and place operation with active surface 130 of semiconductor die 124 oriented toward

interface layer 224. The clearance or distance between the edge 272 of opening 271 and semiconductor die 124 is at least 50 μm. PWB panel 267 is singulated along saw streets 269 into individual PWB units 270, and each semiconductor die 124 has a plurality of vertical interconnect structures 268 disposed around or in a peripheral region of the semiconductor die. Vertical interconnect structures 268 can be disposed in the peripheral region of semiconductor 124 as one or more rows offset from a perimeter of the semiconductor die after singulation through saw streets 269.

Continuing from FIG. 6d, FIG. 6j shows that after semiconductor die 124 and PWB modular units 164-166 are mounted to interface layer 224, reconstituted wafer 227 is partially singulated through saw street 230 using a saw blade or laser cutting tool 274 to form channels or openings 276. Channel 276 extends through PWB units 164-166, and additionally may extend through interface layer 224 and partially but not completely through carrier 220. Channel 276 forms a separation among vertical interconnect structures 158 and the semiconductor die 124 to which the conductive vias will be subsequently joined in a Fo-PoP.

In FIG. 6k, an encapsulant or molding compound 282 is deposited over semiconductor die 124, PWB units 164-166, and carrier 220 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 282 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 282 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.

In FIG. 6l, surface 290 of encapsulant 282 undergoes a grinding operation with grinder 292 to planarize the surface and reduce a thickness of the encapsulant. The grinding operation removes a portion of encapsulant material down to back surface 128 of semiconductor die 124. A chemical etch can also be used to remove and planarize encapsulant 282. Because surface 228 of PWB units 166 is vertically offset with respect to back surface 128 of semiconductor die 124 by distance D3, the removal of encapsulant 282 can be achieved without removing, and incidentally transferring, material from vertical interconnect structures 158, such as Cu, to semiconductor die 124, such as Si. Preventing the transfer of conductive material from vertical interconnect structures 158 to semiconductor die 124 reduces a risk of contaminating a material of the semiconductor die.

In FIG. 6m, an insulating or passivation layer 296 is conformally applied over encapsulant 282 and semiconductor die 124 using PVD, CVD, screen printing, spin coating, or spray coating. The insulating layer 296 contains one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, or other material having similar insulating and structural properties. The insulating layer 296 uniformly covers encapsulant 282 and semiconductor die 124 and is formed over PWB units 164-166. The insulating layer 296 is formed after the removal of a first portion of encapsulant 282 and contacts the exposed back surface 128 of semiconductor die 128. The insulating layer 296 is formed before a second portion of encapsulant 282 is removed to expose PWB units 164-166. In one embodiment, properties of insulating layer 296 are selected to help control warping of the subsequently formed Fo-PoP.

In FIG. 6n, a portion of insulating layer 296 and

encapsulant 282 is removed to form openings 298 and expose vertical interconnect structures 158. Openings 298 are formed by etching, laser, or other suitable process. In one embodiment, openings 298 are formed by LDA using laser 300. Material from vertical interconnect structures 158 is prevented from contacting semiconductor die 124 during removal of encapsulant 282 because openings 298 are formed over vertical interconnect structures 158 around or in a peripheral region around semiconductor die 124, such that vertical interconnect structures 158 are offset with respect to semiconductor die 124 and do not extend to back surface 128. Furthermore, openings 298 are not formed at a time when encapsulant 282 is being removed from over back surface 128 and at a time when semiconductor die 124 is exposed and susceptible to contamination. Because openings 298 are formed after insulating layer 296 is disposed over semiconductor die 124, the insulating layer acts as a barrier to material from vertical interconnect structures 158 being transferred to semiconductor die 124.

In FIG. 6o, carrier 220 and interface layer 224 are removed from reconstituted wafer 227 by chemical etching, mechanical peeling, CMP, mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping to facilitate the formation of an interconnect structure over active surface 130 of semiconductor die 124 and vertical interconnect structures 158 of PWB units 164-166.

FIG. 6o also shows a first portion of an interconnect or RDL is formed by the deposition and patterning of insulating or passivation layer 304. The insulating layer 304 is conformally applied to, and has a first surface that follows the contours of, encapsulant 282, PWB units 164-166, and semiconductor die 124. The insulating layer 304 has a second

planar surface opposite the first surface. The insulating layer 304 contains one or more layers of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other material having similar insulating and structural properties. The insulating layer 304 is deposited using PVD, CVD, printing, spin coating, spray coating, or other suitable process. A portion of insulating layer 304 is removed by LDA using laser 305, etching, or other suitable process to form openings 306 over vertical interconnect structures 158. Openings 306 expose conductive layer 164 of vertical interconnect structures 158 for subsequent electrical connection according to the configuration and design of semiconductor die 124.

In FIG. 6p, an electrically conductive layer 308 is patterned and deposited over insulating layer 304, over semiconductor die 124, and disposed within openings 306 to fill the openings and contact conductive layer 164 of vertical interconnect structures 158 as well as contact conductive layer 132. Conductive layer 308 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. The deposition of conductive layer 308 uses PVD, CVD, electrolytic plating, electroless plating, or other suitable process. Conductive layer 308 operates as an RDL to extend electrical connection from semiconductor die 124 to points external to semiconductor die 124.

FIG. 6p also shows an insulating or passivation layer 310 is conformally applied to, and follows the contours of, insulating layer 304 and conductive layer 308. The insulating layer 310 contains one or more layers of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other material having similar insulating and structural properties. The insulating layer 310 is deposited using PVD, CVD, printing, spin coating, spray coating, or other

suitable process. A portion of insulating layer 310 is removed by LDA using laser 311, etching, or other suitable process to form openings 312, which expose portions of conductive layer 308 for subsequent electrical interconnection.

In FIG. 6q, an electrically conductive layer 316 is patterned and deposited over insulating layer 310, over conductive layer 308, and is disposed within openings 312 to fill the openings and contact conductive layer 308. Conductive layer 316 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. The deposition of conductive layer 316 uses PVD, CVD, electrolytic plating, electroless plating, or other suitable process. Conductive layer 316 operates as an RDL to extend electrical connection from semiconductor die 124 to points external to semiconductor die 124.

FIG. 6q also shows an insulating or passivation layer 318 is conformally applied to, and follows the contours of, insulating layer 310 and conductive layer 316. The insulating layer 318 contains one or more layers of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other material having similar insulating and structural properties. The insulating layer 318 is deposited using PVD, CVD, printing, spin coating, spray coating, or other suitable process. A portion of insulating layer 318 is removed by LDA, etching, or other suitable process to form openings 320, which expose portions of conductive layer 316 for subsequent electrical interconnection.

In FIG. 6r, an electrically conductive bump material is deposited over conductive layer 316 and within openings 320 of insulating layer 318 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi,

Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 316 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form spherical balls or bumps 322. In some applications, bumps 322 are reflowed a second time to improve electrical contact to conductive layer 316. In one embodiment, bumps 322 are formed over a UBM having a wetting layer, barrier layer, and adhesive layer. The bumps can also be compression bonded to conductive layer 316. Bumps 322 represent one type of interconnect structure that can be formed over conductive layer 316. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

Taken together, insulating layers 304, 310, and 318 as well as conductive layers 308, 316, and conductive bumps 322 form build-up interconnect structure 324. The number of insulating and conductive layers included within build-up interconnect structure 324 depends on, and varies with, the complexity of the circuit routing design. Accordingly, build-up interconnect structure 324 can include any number of insulating and conductive layers to facilitate electrical interconnect with respect to semiconductor die 124. Similarly, PWB units 164-166 may include additional metal layers to facilitate design integration and increased routing flexibility before build-up interconnect structure 324 is formed over the PWB units. Furthermore, elements that would otherwise be included in a backside interconnect structure or RDL can be integrated as part of build-up interconnect structure 324 to simplify manufacturing and reduce fabrication costs with respect to a package including

both front side and backside interconnects or RDLs.

FIG. 6r further shows that reconstituted wafer 227 with build-up interconnect structure 324 is singulated using a saw blade or laser cutting tool 326 to form individual Fo-PoP 328. In one embodiment, Fo-PoP 328 has a height in a range of less than 1 mm. PWB modular units 164-166 within Fo-PoP 328 provide a cost effective alternative to using standard laser drilling processes for vertical interconnection in Fo-PoP for a number of reasons. First, PWB units 164-166 can be made with low cost manufacturing technology such as substrate manufacturing technology rather than standard laser drilling that includes high equipment cost and requires drilling through an entire package thickness which increases cycle time and decrease manufacturing throughput. Furthermore, the use of PWB units 164-166 for Fo-PoP vertical interconnection provides an advantage of improved control for vertical interconnection with respect to vertical interconnections formed exclusively by a laser drilling process.

PWB modular units 164-166 contain one or multiple rows of vertical interconnect structures 158 that provide through vertical interconnection between opposing sides of the PWB units and are configured to be integrated into subsequently formed Fo-PoP. Vertical interconnect structures 158 include vias 150 that are left void or alternatively is filled with filler material 154, e.g. conductive material or insulating material. Filler material 154 is specially selected to be softer or more compliant than conductive layer 152. Filler material 154 reduces the incidence of cracking or delamination by allowing vertical interconnect structures 158 to deform or change shape under stress. In one embodiment, vertical interconnect structures 158 include conductive layer 162 that is a copper

protection layer for preventing oxidation of the conductive via, thereby reducing yield loss in SMT applications.

PWB modular units 164-166 are disposed within Fo-PoP 328 such that surface 228 of PWB units 166 and a corresponding surface of PWB units 164 are vertically offset with respect to back surface 128 of semiconductor die 124 by a distance D3. The separation of D3 prevents material from vertical interconnect structures 158, such as Cu, from incidentally transferring to, and contaminating a material of, semiconductor die 124, such as Si. Preventing contamination of semiconductor die 124 from material of vertical interconnect structures 158 is further facilitated by exposing conductive layer 162 by LDA or another removal process separate from the grinding operation of shown in FIG. 6l. Furthermore, the presence of insulating layer 296 over back surface 128 of semiconductor die 124 before the formation of openings 298 serves as a barrier to material from vertical interconnect structures 158 reaching the semiconductor die.

PWB modular units 164-166 disposed within Fo-PoP 328 can differ in size and shape one from another while still providing through vertical interconnect for the Fo-PoP. PWB units 164-166 include interlocking footprints having square and rectangular shapes, a cross-shape (+), an angled or “L-shape,” a circular or oval shape, a hexagonal shape, an octagonal shape, a star shape, or any other geometric shape. At the wafer level, and before singulation, PWB units 164-166 are disposed around semiconductor die 124 in an interlocking pattern such that different sides of the semiconductor die are aligned with, and correspond to, a number of different sides of the PWB units in a repeating pattern. PWB units 164-166 may also include additional metal layers to facilitate design integration and increased routing flexibility before build-up interconnect

structure 324 is formed over the PWB units.

PWB modular units 164-166 provide a cost effective alternative to using standard laser drilling processes for vertical interconnection in Fo-PoP for a number of reasons. First, PWB units 164-166 can be made with low cost manufacturing technology such as substrate manufacturing technology. Second, standard laser drilling includes high equipment cost and requires drilling through an entire package thickness, which increases cycle time and decrease manufacturing throughput. Furthermore, the use of PWB units 164-166 for vertical interconnection provides an advantage of improved control for vertical interconnection with respect to vertical interconnections formed exclusively by a laser drilling process.

FIG. 7a shows an embodiment of conductive pillar or conductive vertical interconnect structure 340 with laminate core 342, conductive layers 344 and 346, and filler material 348. Filler material 348 can be conductive material or insulating material. Conductive layer 344 overlaps laminate core 342 by 0-200 μm. A Cu protective layer 350 is formed over conductive layer 346. An insulating layer 352 is formed over one surface of laminate core 342. A portion of insulating layer 352 is removed to expose Cu protective layer 350.

FIG. 7b shows an embodiment of conductive pillar or conductive vertical interconnect structure 360 with laminate core 362, conductive layers 364 and 366, and filler material 368. Filler material 368 can be conductive material or insulating material. Conductive layer 364 overlaps laminate core 362 by 0-200 μm. A Cu protective layer 370 is formed over conductive layer 366.

FIG. 7c shows an embodiment of conductive pillar or conductive vertical interconnect structure 380 with laminate

core 382, conductive layers 384 and 386, and filler material 388. Filler material 388 can be conductive material or insulating material. Conductive layer 384 overlaps laminate core 382 by 0-200 μm. A Cu protective layer 390 is formed over conductive layer 346. An insulating layer 392 is formed over one surface of laminate core 382. An insulating layer 394 is formed over an opposite surface of laminate core 382. A portion of insulating layer 394 is removed to expose Cu protective layer 386.

FIG. 7d shows an embodiment of conductive pillar or conductive vertical interconnect structure 400 with laminate core 402, conductive layers 404 and 406, and filler material 408. Filler material 408 can be conductive material or insulating material. Conductive layer 404 overlaps laminate core 402 by 0-200 μm.

FIG. 7e shows an embodiment of conductive pillar or conductive vertical interconnect structure 410 with laminate core 412, conductive layer 414, and filler material 416. Filler material 416 can be conductive material or insulating material. Conductive layer 414 overlaps laminate core 412 by 0-200 μm. An insulating layer 418 is formed over one surface of laminate core 412. A portion of insulating layer 418 is removed to expose conductive layer 414. A conductive layer 420 is formed over the expose conductive layer 414. A Cu protective layer 422 is formed over conductive layer 420. An insulating layer 424 is formed over an opposite surface of laminate core 412. A conductive layer 426 is formed over the expose conductive layer 414.

FIG. 7f shows an embodiment of conductive pillar or conductive vertical interconnect structure 430 with laminate core 432, conductive layer 434, and filler material 436. Filler

material 436 can be conductive material or insulating material. Conductive layer 434 overlaps laminate core 432 by 0-200 μm. An insulating layer 438 is formed over one surface of laminate core 432. A portion of insulating layer 438 is removed to expose conductive layer 434. A conductive layer 440 is formed over the expose conductive layer 434. A Cu protective layer 442 is formed over conductive layer 420. An insulating layer 444 is formed over an opposite surface of laminate core 432. A conductive layer 446 is formed over the expose conductive layer 434. A Cu protective layer 446 is formed over conductive layer 446.

FIG. 7g shows an embodiment of conductive pillar or conductive vertical interconnect structure 450 with laminate core 452, conductive layers 454 and 456, and filler material 458. Filler material 458 can be conductive material or insulating material. Conductive layer 454 overlaps laminate core 452 by 0-200 μm. A Cu protective layer 460 is formed over conductive layer 456. An insulating layer 462 is formed over one surface of laminate core 452. A portion of insulating layer 462 is removed to expose Cu protective layer 460. An insulating layer 464 is formed over an opposite surface of laminate core 452. A portion of insulating layer 464 is removed to expose Cu protective layer 460.

FIG. 7h shows an embodiment of conductive pillar or conductive vertical interconnect structure 470 with laminate core 472, conductive layers 474 and 476, and filler material 478. Filler material 478 can be conductive material or insulating material. Conductive layer 474 overlaps laminate core 472 by 0-200 μm. A Cu protective layer 480 is formed over conductive layer 476. An insulating layer 482 is formed over one surface of laminate core 472. An insulating layer 484 is

formed over an opposite surface of laminate core 472. A portion of insulating layer 484 is removed to expose Cu protective layer 480.

FIG. 7i shows an embodiment of conductive pillar or conductive vertical interconnect structure 490 with laminate core 492, conductive layers 494 and 496, and filler material 498. Filler material 498 can be conductive material or insulating material. Conductive layer 494 overlaps laminate core 492 by 0-200 μm. A Cu protective layer 500 is formed over conductive layer 496. An insulating layer 502 is formed over an opposite surface of laminate core 492. A portion of insulating layer 502 is removed to expose Cu protective layer 480. A Cu protective layer 504 is formed over the exposed conductive layer 496.

In FIG. 8a, a plurality of bumps 510 is formed over Cu foil 512, or other foil or carrier with thin patterned Cu or other wetting material layer. The foil or supporting layer can be evenly bonded to temporary carrier with thermal releasing tape which can stand reflow temperature. In FIG. 8b, an encapsulant 514 is formed over bumps 510 and Cu foil 512. In FIG. 8c, Cu foil 512 is removed and bumps 510 embedded in encapsulant 514 is singulated with saw blade or laser cutting tool 516 into PWB vertical interconnect units 518.

FIG. 9 shows a Fo-PoP 520 including semiconductor die 522, which is similar to semiconductor die 124 from FIG. 3c. Semiconductor die 522 has a back surface 524 and active surface 526 opposite back surface 524 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. An electrically conductive

layer 528 is formed over active surface 526 and operates as contact pads that are electrically connected to the circuits on active surface 526. An insulating or passivation layer 530 is conformally applied over active surface 526.

FIG. 9 also shows PWB modular units 518 from FIGs. 8a-8c laterally offset from, and disposed around or in a peripheral region around semiconductor die 522. Back surface 524 of semiconductor die 522 is offset from PWB modular units 518 by at least 1 μm, similar to FIG. 5b. Encapsulant 532 is deposited around PWB units 518. A build-up interconnect structure 534, similar to build-up interconnect structure 180 in FIG. 5e, is formed over encapsulant 532, PWB units 518, and semiconductor die 522. An insulating or passivation layer 536 is formed over encapsulant 532, PWB units 518, and semiconductor die 522. A portion of encapsulant 514 and insulating layer 536 is removed to expose bumps 510. Bumps 510 are offset from back surface 524 of semiconductor die 522 by at least 1 μm.

FIG. 10 shows an embodiment of Fo-PoP 540, similar to FIG. 5h, with encapsulant 542 disposed around PWB units 164-166.

In FIG. 11a, semiconductor die 550 has a back surface 552 and active surface 554 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. An electrically conductive layer 556 is formed over active surface 554 and operates as contact pads that are electrically connected to the circuits on active surface 554.

Semiconductor die 550 is mounted back surface 552 oriented to substrate 560. Substrate 560 can be a PCB. A plurality of bond wires 562 is formed between conductive layer

556 and trace lines or contact pads 564 formed on substrate 560. An encapsulant 566 is deposited over semiconductor die 550, substrate 560, and bond wires 562. Bumps 568 are formed over contact pads 570 on substrate 560.

FIG. 11b shows Fo-PoP 540 from FIG. 10 with PWB modular units 164-166 laterally offset and disposed around or in a peripheral region around semiconductor die 124. Substrate 560 with semiconductor die 550 is mounted to Fo-PoP 540 with bumps 568 metallically and electrically connected to PWB modular units 164-166. Semiconductor die 124 of Fo-PoP 540 is electrically connected through bond wires 562, substrate 560, bumps 556, and PWB modular unites 164-166 to build-up interconnect structure 180 for vertical interconnect.

FIGs. 12a-12b illustrate a process of forming modular units from an encapsulant panel with fine filler. FIG. 12a shows a cross-sectional view of a portion of encapsulant panel 578. Encapsulant panel 578 includes a polymer composite material, such as epoxy resin, epoxy acrylate, or polymer, with a suitable fine filler material (i.e., less than 45 μm) deposited within the polymer composite material. The fine filler material enables the CTE of encapsulant panel 578 to be adjusted such that the CTE of encapsulant panel 578 is greater than subsequently deposited package encapsulant material. Encapsulant panel 578 has a plurality of saw streets 579 for singulating encapsulant panel 578 into individual modular units.

In FIG. 12b, encapsulant panel 578 is singulated through saw streets 579 into individual modular units 580 using saw blade or laser cutting tool 582. Modular units 580 have a shape or footprint similar to PWB modular units 164-166 shown in FIGs. 6e-6i, but do not have embedded conductive pillars or conductive bumps. The CTE of modular units 580 is greater than

the CTE of subsequently deposited encapsulant material to reduce the incidence of warpage under thermal stress. The fine filler within the encapsulant material of modular units 580 also enables improved laser drilling for subsequently formed openings, which are formed through modular units 580.

FIGs. 13a-13i illustrate another process of forming a Fo-PoP with a modular unit formed from an encapsulant panel without embedded conductive pillars or bumps. Continuing from FIG. 6b, modular units 580 from FIG. 12b are mounted to interface layer 224 over carrier 220 using a pick and place operation. In another embodiment, encapsulant panel 578 from FIG. 12a is mounted to interface layer 224, prior to mounting semiconductor die 124, as a 300-325 mm round panel or 470 mm x 370 mm rectangular panel, and openings are punched through encapsulant panel 578 to accommodate semiconductor die 124, and encapsulant panel 578 is singulated into individual modular units 580, similar to FIG. 6i.

When modular units 580 are mounted to interface layer 224, surface 583 of modular units 580 is coplanar with exposed surface 584 of interface layer 224, such that surface 583 is not embedded within interface layer 224. Thus, surface 583 of modular units 580 is vertically offset with respect to surface 225 of insulating layer 134.

FIG. 13b shows semiconductor die 124 and modular units 580 mounted over carrier 220 as a reconstituted wafer 590. A surface 592 of modular units 580 is vertically offset with respect to back surface 128 of semiconductor die 124. Reconstituted wafer 590 is partially singulated through modular units 580 between semiconductor die 124 using a saw blade or laser cutting tool 596 to form channel or opening 598. Channel 598 extends through modular units 580, and additionally may

extend through interface layer 224 and partially but not completely through carrier 220. Channel 598 forms a separation among modular units 580 and semiconductor die 124.

In FIG. 13c, an encapsulant or molding compound 600 is deposited over semiconductor die 124, modular units 580, and carrier 220 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 600 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 600 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. Encapsulant 600 has a lower CTE than modular units 580. In FIG. 13d, carrier 220 and interface layer 224 are removed from reconstituted wafer by chemical etching, mechanical peeling, CMP, mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping to facilitate the formation of an interconnect structure over active surface 130 of semiconductor die 124 and modular units 580.

In FIG. 13e, an insulating or passivation layer 602 is formed over encapsulant 600, modular units 580, and semiconductor die 124. Insulating layer 602 contains one or more layers of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other material having similar insulating and structural properties. Insulating layer 602 is deposited using PVD, CVD, printing, spin coating, spray coating, or other suitable process. A portion of insulating layer 602 is removed by LDA, etching, or other suitable process to expose conductive layer 132 and surface 182 of modular units 580.

An electrically conductive layer 603 is patterned and deposited over insulating layer 602, over semiconductor die 124,

and within the openings formed through insulating layer 602. Conductive layer 603 is electrically connected to conductive layer 132 of semiconductor die 124. Conductive layer 603 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. In one embodiment, conductive layer 603 contains Ti/Cu, TiW/Cu, or Ti/NiV/Cu. The deposition of conductive layer 603 uses PVD, CVD, electrolytic plating, electroless plating, or other suitable process. Conductive layer 603 operates as an RDL to extend electrical connection from semiconductor die 124 to points external to semiconductor die 124 to laterally redistribute the electrical signals of semiconductor die 124 across the package. Portions of conductive layer 603 can be electrically common or electrically isolated according to the design and function of semiconductor die 124.

An insulating or passivation layer 604 is formed over conductive layer 603 and insulating layer 602. Insulating layer 604 contains one or more layers of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other material having similar insulating and structural properties. Insulating layer 604 is deposited using PVD, CVD, printing, spin coating, spray coating, or other suitable process. A portion of insulating layer 604 is removed by LDA, etching, or other suitable process to expose portions of conductive layer 603 for subsequent electrical interconnection.

An electrically conductive layer 605 is patterned and deposited over insulating layer 604, within the openings formed through insulating layer 604, and is electrically connected to conductive layers 603 and 132. Conductive layer 605 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. In one embodiment, conductive layer 605 contains Ti/Cu, TiW/Cu, or Ti/NiV/Cu. The deposition

of conductive layer 605 uses PVD, CVD, electrolytic plating, electroless plating, or other suitable process. Conductive layer 605 operates as an RDL to extend electrical connection from semiconductor die 124 to points external to semiconductor die 124 to laterally redistribute the electrical signals of semiconductor die 124 across the package. Portions of conductive layer 605 can be electrically common or electrically isolated according to the design and function of semiconductor die 124.

An insulating layer 606 is formed over insulating layer 604 and conductive layer 605. Insulating layer 606 contains one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, or other material having similar insulating and structural properties. Insulating layer 606 is deposited using PVD, CVD, printing, spin coating, spray coating, or other suitable process. A portion of insulating layer 606 is removed by LDA, etching, or other suitable process to form openings to expose portions of conductive layer 605 for subsequent electrical interconnection.

An electrically conductive bump material is deposited over the exposed portion of conductive layer 605 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 605 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form spherical balls or bumps 607. In some applications, bumps 607 are reflowed a second time to improve

electrical contact to conductive layer 605. In one embodiment, bumps 607 are formed over a UBM having a wetting layer, barrier layer, and adhesive layer. The bumps can also be compression bonded to conductive layer 605. Bumps 607 represent one type of interconnect structure that can be formed over conductive layer 605. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

Collectively, insulating layers 602, 604, and 606, conductive layers 603, 605, and conductive bumps 607 constitute a build-up interconnect structure 610. The number of insulating and conductive layers included within build-up interconnect structure 610 depends on, and varies with, the complexity of the circuit routing design. Accordingly, build-up interconnect structure 610 can include any number of insulating and conductive layers to facilitate electrical interconnect with respect to semiconductor die 124. Furthermore, elements that would otherwise be included in a backside interconnect structure or RDL can be integrated as part of build-up interconnect structure 610 to simplify manufacturing and reduce fabrication costs with respect to a package including both front side and backside interconnects or RDLs.

In FIG. 13f, back grinding tape 614 is applied over build-up interconnect structure 610 using lamination or other suitable application process. Back grinding tape 614 contacts insulating layer 606 and bumps 607 of build-up interconnect structure 610. Back grinding tape 614 follows the contours of a surface of bumps 607. Back grinding tape 614 includes tapes with thermal resistance up to 270 °C. Back grinding tape 614 also includes tapes with a thermal release function. Examples of back grinding tape 614 include UV tape HT 440 and non-UV tape

MY-595. Back grinding tape 614 provides structural support for subsequent back grinding and removal of a portion of encapsulant 600 from a backside surface 624 of encapsulant 600, opposite build-up interconnect structure 610.

Backside surface 624 of encapsulant 600 undergoes a grinding operation with grinder 628 to planarize and reduce a thickness of encapsulant 600 and semiconductor die 124. A chemical etch can also be used to planarize and remove a portion of encapsulant 600 and semiconductor die 124. After the grinding operation is completed, exposed back surface 630 of semiconductor die 124 is coplanar with surface 592 of modular units 580 and exposed surface 632 of encapsulant 600.

In FIG. 13g, a backside balance layer 640 is applied over encapsulant 600, modular units 580, and semiconductor die 124 with back grinding tape 614 providing structural support to reconstituted wafer 590. In another embodiment, back grinding tape 614 is removed prior to forming backside balance layer 640. The CTE of backside balance layer 640 can be adjusted to balance the CTE of build-up interconnect structure 610 in order to reduce warpage of the package. In one embodiment, backside balance layer 640 balances the CTE, e.g. 30-150ppm/K, of build-up interconnect structure 610 and reduces warpage in the package. Backside balance layer 640 also provides structural support to the package. In one embodiment, backside balance layer 640 has a thickness of 10-100 μm. Backside balance layer 640 can also act as a heat sink to enhance thermal dissipation from semiconductor die 124. Backside balance layer 640 can be any suitable balance layer with suitable thermal and structural properties, such as RCC tape.

In FIG. 13h, a portion of backside balance layer 640 and modular units 580 is removed to form vias or openings 644

and expose conductive layer 603 of build-up interconnect structure 610 through modular units 580. Openings 644 are formed by etching, laser, or other suitable process, using proper clamping or a vacuum foam chuck with supporting tape for structural support. In one embodiment, openings 644 are formed by LDA using laser 650. The fine filler of modular units 580 enables improved laser drilling to form openings 644. Openings 644 can have vertical, sloped, or stepped sidewalls, and extend through insulating layer 640 and surface 583 of modular units 580 to expose conductive layer 603. After forming openings 644, openings 644 undergo a desmearing or cleaning process, including a particle and organic residue wet clean, such as a single wafer pressure jetting clean with a suitable solvent, or alkali and carbon dioxide bubbled deionized water, in order to remove any particles or residue from the drilling process. A plasma clean is also performed to clean any contaminants from the exposed conductive layer 603, using reactive ion etching (RIE) or downstream/microwave plasma with O2 and one or more of tetrafluoromethane (CF4), nitrogen (N2), or hydrogen peroxide (H2O2). In embodiments where conductive layer 603 includes a TiW or Ti adhesive layer, the adhesive layer of conductive layer 603 is etched with a wet etchant in either a single wafer or batch process, and followed by a copper oxide clean.

In FIG. 13i, an electrically conductive bump material is deposited over the exposed conductive layer 603 of build-up interconnect structure 610 within openings 644 using an evaporation, electrolytic plating, electroless plating, ball drop, screen printing, jetting, or other suitable process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead

solder, or lead-free solder. The bump material is bonded to conductive layer 603 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form spherical balls or bumps 654. In some applications, bumps 654 are reflowed a second time to improve electrical contact to conductive layer 603. A UBM layer can be formed under bumps 654. The bumps can also be compression bonded to conductive layer 603. Bumps 654 represent one type of conductive interconnect structure that can be formed over conductive layer 603. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. The assembly is singulated using a saw blade or laser cutting tool 656 to form individual Fo-PoP 660, and back grinding tape 614 is removed.

In FIG. 14 shows Fo-PoP 660 after singulation. Modular units 580 are embedded within encapsulant 600 around semiconductor die 124 to provide vertical interconnection in Fo-PoP 660. Modular units 580 are formed from an encapsulant panel with a fine filler, and modular units 580 have a higher CTE than encapsulant 600, which provides flexibility to adjust the overall CTE of Fo-PoP 660. Modular units 580 can have a shape or footprint similar to the modular units shown in FIGs. 6e-6i. After depositing encapsulant 600 over modular units 580 and semiconductor die 124, the package undergoes a back grinding process to remove a portion of encapsulant 600 and semiconductor die 124, such that modular units 580 have a thickness substantially equal to the thickness of semiconductor die 124. A backside balance layer 640 is formed over modular units 580, encapsulant 600, and semiconductor die 124 to provide additional structural support, and prevent warpage of Fo-PoP 660. Openings

644 are formed through backside balance layer 640 and modular units 580 to expose conductive layer 603 of build-up interconnect structure 610. Bumps 654 are formed within openings 644 to form a three-dimensional (3-D) vertical electrical interconnect structure through Fo-PoP 660. Thus, modular units 580 do not have embedded conductive pillars or bump material for vertical electrical interconnect. Forming openings 644 and bumps 654 through modular units 580 reduces the number of manufacturing steps, while still providing modular units for vertical electrical interconnect.

FIGs. 15a-15b illustrate a process of forming modular units from a PCB panel. FIG. 15a shows a cross-sectional view of a portion of PCB panel 670. PCB panel 670 includes one or more laminated layers of polytetrafluoroethylene pre-impregnated (prepreg), FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. PCB panel 670 has a plurality of saw streets 672 for singulating PCB panel 670 into individual modular units. In FIG. 15b, PCB panel 670 is singulated through saw streets 672 using saw blade or laser cutting tool 674 into individual modular units 676. Modular units 676 have a shape or footprint similar to PWB modular units 164-166 shown in FIGs. 6e-6i, but do not have embedded conductive pillars or conductive bumps. The CTE of modular units 676 is greater than the CTE of subsequently deposited encapsulant material to reduce the incidence of warpage under thermal stress.

FIG. 16 shows an embodiment of Fo-PoP 660, similar to FIG. 14, with modular units 676 embedded within encapsulant 600 instead of modular units 580. Modular units 676 are embedded within encapsulant 600 around semiconductor die 124 to provide

vertical interconnection in Fo-PoP 660. Modular units 676 are formed from a PCB panel, and modular units 676 have a higher CTE than encapsulant 600, which provides flexibility to adjust the overall CTE of Fo-PoP 660. Modular units 676 can have a shape or footprint similar to the PWB modular units shown in FIGs. 6e-6i. After depositing encapsulant 600 over modular units 676 and semiconductor die 124, the package undergoes a back grinding process to remove a portion of encapsulant 600 and semiconductor die 124, such that modular units 676 have a thickness substantially equal to the thickness of semiconductor die 124. A backside balance layer 640 is formed over modular units 676, encapsulant 600, and semiconductor die 124 to provide additional structural support, and prevent warpage of Fo-PoP 660. Openings 644 are formed through backside balance layer 640 and modular units 580 to expose conductive layer 603 of build-up interconnect structure 610. Bumps 654 are formed within openings 644 to form a 3-D vertical electrical interconnect structure through Fo-PoP 660. Thus, modular units 676 do not have embedded conductive pillars or bump material for vertical electrical interconnect. Forming openings 644 and bumps 654 through modular units 676 reduces the number of manufacturing steps, while still providing modular units for vertical electrical interconnect.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a carrier;

mounting a modular interconnect unit over the carrier in a peripheral region of the semiconductor die;

mounting a semiconductor die to the carrier;

depositing an encapsulant over the carrier, semiconductor die, and modular interconnect unit; and

removing a portion of the encapsulant to expose the modular interconnect unit and the semiconductor die.

2. The method of claim 1, wherein the modular interconnect unit includes a core with a vertical interconnect structure formed through the core.

3. The method of claim 1, further including forming an insulating layer over a back surface of the semiconductor die prior to exposing the modular interconnect unit with respect to the encapsulant.

4. The method of claim 1, wherein removing the portion of encapsulant further includes:

removing a first portion of the encapsulant from over the semiconductor die to expose a back surface of the semiconductor die while leaving a second portion of the encapsulant over the modular interconnect unit; and

removing the second portion of the encapsulant to expose the modular interconnect unit.

5. The method of claim 1, wherein the modular interconnect unit forms part of an interlocking pattern around the semiconductor die and a height of the modular interconnect unit is less than a height of the semiconductor die.

6. A method of making a semiconductor device, comprising:

providing a semiconductor die;

disposing a modular interconnect unit in a peripheral region around the semiconductor die; and

depositing an encapsulant over the semiconductor die and modular interconnect unit.

7. The method of claim 6, wherein the modular interconnect unit includes a core with a conductive interconnect structure formed through the core.

8. The method of claim 7, wherein the conductive interconnect structure includes a metal cap and a protection layer formed over the metal cap.

9. The method of claim 7, wherein the modular interconnect unit includes multiple rows of vertical interconnect structures or bumps.

10. The method of claim 6, further including forming a vertical interconnect structure through the modular interconnect unit after depositing the encapsulant over the semiconductor die and modular interconnect unit.

11. A semiconductor device, comprising:

a semiconductor die;

a modular interconnect unit disposed in a peripheral region around the semiconductor die; and

an encapsulant deposited around the semiconductor die and modular interconnect unit.

12. The semiconductor device of claim 11, wherein the modular interconnect unit includes a core with a vertical interconnect structure formed through the core.

13. The semiconductor device of claim 11, wherein the modular interconnect unit has a square shape, rectangular shape, cross-shape, angled or L-shape, circular shape, or oval shape.

14. The semiconductor device of claim 11, wherein the modular interconnect unit forms part of an interlocking pattern around the semiconductor die and a height of the modular interconnect unit is less than a height of the semiconductor die.

15. The semiconductor device of claim 11, further including an insulating layer formed over the semiconductor device to reduce warpage.