CONTROLLING ELECTROMECHANICAL BEHAVIOR OF STRUCTURES WITHIN A MICROELECTROMECHANICAL SYSTEMS DEVICE

Background of the Invention

Field of the Invention

[0001] This invention relates to microelectromechanical systems devices. In particular it relates to thin film structures in microelectromechanical systems devices and to electromechanical and optical responses of such thin film structures.

Description of the Related Art

[0002] Today a wide variety of microelectromechanical systems (MEMS) devices may be fabricated using microfabrication techniques. Examples of these MEMS devices include motors, pumps, valves, switches, sensors, pixels, etc.

[0003] Often these MEMS devices harness principles and phenomena from different domains such as the optical, electrical and mechanical domains. Such principles and phenomena, while seemingly difficult to harness in the macroscopic world, can become extremely useful in the microscopic world of MEMS devices, where such phenomena become magnified. For example, electrostatic forces which are generally considered to be too weak in the macroscopic world to be harnessed, are strong enough in the microscopic world of MEMS devices to activate these devices, often at high speeds and with low power consumption.

[0004] Materials used in MEMS devices are generally selected based on their inherent properties in the optical, electrical, and mechanical domains and the characteristic response to input, such as for example, a driving or actuation voltage.

[0005] One problem affecting the fabrication of MEMS devices is that in some cases, a material having a highly desirable response to input, for example an optical response to incident light, may also have an undesirable response to input, for example, an electromechanical response to an actuation or driving voltage. To overcome, or at least reduce, the undesirable response, new materials have to be found or developed often at great expense.

[0006] Another problem with the fabrication of MEMS devices is that sometimes, a material selected for its characteristic response may become damaged due to exposure to chemical agents used during a particular microfabrication process. This causes the material to demonstrate less of the characteristic response to the input.

Summary of the Invention

In one embodiment, a MEMS device having a substrate is provided, the MEMS device including an electrode layer formed over the substrate, a dielectric layer formed over the electrode layer, a first etch barrier layer formed over the dielectric layer, a second etch barrier layer formed over the first etch barrier layer, a cavity located above the second etch barrier, and a moving layer located above the cavity.

In another embodiment, a MEMS device is provided, the MEMS device including conducting means for conducting an electrical signal, supporting means for supporting the conducting means, insulating means for electrically insulating the conducting means, first protecting means for protecting the insulating means, second protecting means for protecting the first protecting means, and defining means for defining a cavity having a variable size.

In another embodiment, a method of manufacturing a MEMS device is provided, the method including depositing an electrode layer on a substrate, depositing a dielectric layer over the electrode layer, depositing an etch stop layer over the dielectric layer, and depositing a protective layer over the etch stop layer.

In another embodiment, a method of manufacturing a MEMS device is provided, the method including depositing an electrode layer on a substrate, depositing a first dielectric layer over the electrode layer, depositing second dielectric layer over the first dielectric layer, depositing a third dielectric layer over the second dielectric layer, depositing a first sacrificial layer over the third dielectric layer, performing a preliminary etch to remove a portion of the first sacrificial layer, thereby exposing at least a portion of the third dielectric layer, and depositing a second sacrificial layer over the remaining portion of the first sacrificial layer and the exposed portion of the third dielectric layer.

In another embodiment, a MEMS device is provided, the MEMS device including a substrate, an electrode layer located over a substrate. a charge-trapping layer located over the

electrode layer, wherein the charge-trapping layer is configured to trap both positive and negative charge, and a first etch barrer layer located over the charge-trapping layer.

In another embodiment, a method of manufacturing a MEMS device is provided, including depositing an electrode layer on a substrate, depositing a charge-trapping layer over the electrode layer, wherein the charge-trapping layer is configured to trap both positive and negative charge, and depositing a first etch barrier layer over the charge-trapping layer.

In another embodiment, a MEMS device is provided, the MEMS device including a substrate, an electrode layer formed over the substrate, a layer of silicon nitride formed over the electrode layer, and a layer of aluminum oxide formed over the layer of silicon nitride.

[0007] In another embodiment, a MEMS device is provided, the MEMS device including means for conducting an electrical signal, means for supporting said conducting means, means for trapping both positive and negative charge, and means for protecting said means for trapping charge.

Brief Description of the Drawings

[0008] Figures 1 and 2 show schematic cross-sections of a MEMS device in an unactuated, and an actuated state respectively;

[0009] Figure 3 shows a chart of the actuation and release voltages for the MEMS device of Figures 1 and 2;

[0010] Figure 4 shows one a thin film stack for a MEMS device, in accordance with one embodiment of the invention;

[0011] Figure 5 shows a thin film stack for a MEMS device, in accordance with another embodiment of the invention.

[0012] Figure 6 shows a hysteresis curve for a MEMS device including the thin film stack shown in Figure 5 of the drawings;

[0013] Figure 7 shows another embodiment of a thin film stack for a MEMS device;

[0014] Figure 8 shows a hysteresis curve for a MEMS device including the thin film stack of Figure 7 of the drawings;

[0015] Figures 9A-9D show embodiments of a thin film stack for a MEMS device;

[0016] Figures 10A-10H illustrate an exemplary process for manufacturing a MEMS device;

[0017] Figures 11A and 11B show embodiments of a thin film stack for a MEMS device;

[0018] Figure 11C is a cross section of two interferometric modulators which include a thin film stack in accordance with an embodiment of the invention;

[0019] Figure 11D shows another embodiment of a thin film stack for a MEMS device;

[0020] Figure 12A shows a block diagram of an electrostatic fluid flow system within a MEMS device in accordance with one embodiment of the invention;

[0021] Figure 12B is a schematic, isometric view of the fluid flow system of Figure 8a illustrating its principle of operation; and

[0022] Figure 13 schematically shows another embodiment of a MEMS device in accordance with the invention.

[0023] Figures 14A and 14B are system block diagrams illustrating an embodiment of a visual display device comprising a plurality of interferometric modulators.

Detailed Description of the Preferred Embodiment

[0024] A particular structure or layer within a microelectromechanical systems (MEMS) device may be desirable for its optical response to input in the form of incident light, but may at the same time have an undesirable electromechanical response to input in the form of an actuation or driving voltage. Techniques are disclosed herein to manipulate or control the electromechanical response of the structure or layer, thus at least reducing the undesirable electomechanical response.

[0025] As an illustrative, but a non-limiting example of a MEMS device, consider the interference modulator (IMOD) device 10 shown in Figure 1 of the drawings. Referring to Figure 1, it will be seen that IMOD device 10 has been greatly simplified for illustrative purposes so as not to obscure aspects of the present invention.

[0026] The IMOD device 10 includes a transparent layer 12 and a reflective layer 14 which is spaced from the transparent layer 12 by an air gap 16. The reflective layer 14 is supported on posts 18 and is electrostatically displaceable towards the transparent layer 12

thereby to close the air gap 16. An electrode 20 which is connected to a driving mechanism 22 is used to cause the electrostatic displacement of reflective layer 14. Figure 1 shows the reflective layer 14 in an undriven or undisplaced condition, whereas Figure 2 shows the reflective layer 14 in a driven or displaced condition. The reflective layer 14 is generally selected to produce a desired optical response to incident light when it is brought into contact with the transparent layer 12. In one IMOD design, the transparent layer 12 may comprise SiO_2. The electrode 20 and the transparent layer 12 are formed on a substrate 24. The substrate 24, the electrode 20, and the transparent layer 12 thereon will be referred to as a "thin film stack."

[0027] Typically, a plurality of IMOD devices 10 are fabricated in a large array so as to form pixels within a reflective display. Within such a reflective display, each IMOD device 10 essentially defines a pixel which has a characteristic optical response when in the undriven state, and a characteristic optical response when in the driven state. The transparent layer 12 and the size of the air gap 16 may be selected so that an IMOD within the reflective display may reflect red, blue, or green light when in the undriven state and may absorb light when in the driven state, as described in more detail with respect to Figures 10A-10H.

[0028] It will be appreciated that during operation of the reflective display, the IMOD devices 10 are rapidly energized, and de-energized in order to convey information. When energized, the reflective layer 14 of an IMOD 10 device is electrostatically driven towards the transparent layer 12, and when the IMOD 10 is de-energized, the reflective layer 14 is allowed to return to its undriven state. In order to keep the reflective layer 14 in its driven condition, a bias voltage is applied to each IMOD device 10.

[0029] If an actuation voltage, $V_{actuation}$, defined as a voltage required to electrostatically drive the reflective layer 14 of an IMOD device to its driven condition, as shown in Figure 2 of the drawings, is equal to a release voltage, $V_{release}$, defined as the voltage at which the reflective layer 14 returns to its undisplaced condition, as is shown in Figure 1 of the drawings, then it becomes extremely difficult to select an appropriate bias voltage, V_{bias}, that can be applied to all of the IMOD's 10 within the reflective display to keep the reflective layers 14 of each respective IMOD device 10 within the reflective display in its driven condition. The reason for this is that each IMOD 10 within the reflective display may have slight variations, for example, variations in a thickness of the layers 12, 14, etc.,

which, in practice, result in a different release voltage, $V_{release}$, for each IMOD 10. Further, due to line resistance, there will be variations in the actual voltage applied to each IMOD 10, based on its position within the display. This makes it very difficult, if not impossible, to select a value for V_{bias} that will keep the reflective layer 14 of each respective IMOD 10 within the reflective display in its driven condition. This is explained with reference to Figure 3 of the drawings, which shows the observed hysteresis behavior of the reflective layer 14 of an IMOD 10, in which the transparent layer 12 comprised SiO_2.

[0030] Referring to Figure 3, a curve, 30 is shown, which plots applied voltage (in volts) on the X-axis, against optical response measured in the volts on the Y-axis for an IMOD 10 comprising a transparent layer of SiO_2. As can be seen, actuation of the reflective layer 14 occurs at about 12.5 volts, i.e., $V_{actuation}$ equals 12.5 volts, and the reflective layer 14 returns to its undriven condition when the applied voltage falls to below 12.5 volts, i.e., $V_{release}$, equals 12.5 volts. Thus, the reflective layer 14 in an IMOD device 10 in which the transparent layer comprises only SiO_2 can sometimes demonstrate no hysteresis. Therefore, if the reflective display is fabricated using IMOD devices 10, each comprising a transparent layer 12 and the hysteresis behavior of Figure 3, it would be impossible to select a value for V_{bias}. For example, if V_{bias} is selected to be 12.5 volts, because of variations within the IMOD devices 10 in the reflective display, for at least some of the IMOD devices 10, a V_{bias} of 12.5 volts would fail to keep the reflective layer 14 of those IMOD devices 10 in the driven condition.

[0031] In order to select a V_{bias} that is sufficient to keep the reflective layer 14 of a respective IMOD device 10 within a reflective display in its driven condition, it is necessary for each reflective layer 14 of a respective IMOD device 10 within the reflective display to demonstrate some degree of hysteresis, defined as a non-zero difference between the $V_{actuation}$ and $V_{release}$.

[0032] It will be appreciated, in view of the disclosure herein, that the electromechanical response of the reflective layer 14 of each IMOD device 10 is determined by the electromechanical properties of the reflective layer 14 as well as the electrical properties of the transparent layer 12. In one particular IMOD device design, the transparent layer 12 comprises SiO_2 which gives a desired optical response when the reflective layer 14 is brought into contact therewith. However, the transparent layer 12 comprising SiO_2 has a

certain electrical characteristic or property (the SiO_2 traps negative charge) that affects the hysteresis behavior of the reflective layer 14. Thus, the transparent layer 12 has a desired optical response but an undesirable electromechanical response to a driving or actuation voltage which affects the hysteresis behavior of the reflective layer 14.

[0033] In accordance with embodiments of the present invention, the electromechanical behavior of the transparent layer 12 is altered by adding a further layer or layers, replacing SiO_2, in the thin film stack. This further layer at least minimizes or compensates for the effect of transparent layer 12 on the hysteresis behavior of the reflective layer 14.

[0034] Figure 4 illustrates an exemplary thin film stack which can be used to modify the electromechanical response of the device, namely by shifting or otherwise modifying the hysteresis curve. Specifically, Figure 4 illustrates the formation of a composite layer 35 on a substrate 32 and an electrode 34 by deposition, preferably by CVD. The composite layer 35 comprises a lower layer 36, which may be molybdenum, a silicon-containing material (e.g. silicon, silicon nitride, silicon oxide, etc.), tungsten, or titanium, preferably silicon oxide, which is a dielectric material. In certain embodiments, portions of the lower layer 36 may be removed in a later etching step. The upper, or "stop" layer 38 is preferably a material that is more resistant to a later etching step than the lower layer 36, and may also be a metal (e.g. titanium, aluminum, silver, chromium) or a dielectric material, preferably a metal oxide, e.g. an aluminum oxide. Aluminum oxide may be deposited directly or by deposition of an aluminum layer followed by oxidation. The upper and lower layers 38, 36 may be composed of the same material, but are preferably different materials. In any particular composite layer 35, at least one of the portions 36, 38 is an electrical insulator to avoid shorting the lower electrode 20 to the moving electrode 14 (see Figures 1 and 2). The stop layer 38 may be thinner or thicker than the lower layer 36. For example, in an embodiment the stop layer 38 may have a thickness in the range of about 50 angstroms to about 500 angstroms, and the lower layer 36 may have a thickness in the range of about 500 angstroms to about 3000 angstroms. The stop layer 38 serves as the etch stop, preventing removal or other damage to the lower layer 36 located underneath the etch stop 38. The stop layer 38 is more resistant to removal (e.g. etching) than the lower layer 36. In a particular

embodiment, discussed in greater detail with respect to Figure 5, the stop layer 38 is aluminum oxide and the dielectric layer 38 is silicon oxide.

[0035] In further embodiments as discussed in greater detail below, a stop layer 38 which is suitable for protecting the lower layer 36 from a given etch process may itself require protection, either from a prior or subsequent etch process or from environmental conditions. In such a case, the deposition of a secondary protective layer 39, shown in phantom in Figure 4, may advantageously be used to protect the stop layer 38. In certain embodiments, layers 36 and 38 may be deposited, and an etch process may be used during which the stop layer 38 protects dielectric layer 36. The protective layer 39 can then be deposited above the stop layer 38, and may protect it from a subsequent etching process or from environmental conditions. In alternate embodiments, the protective layer 39 can be deposited on the stop layer 38 prior to etching, and protect it from a first etching process which would otherwise have an undesirable effect on the stop layer 38. The protective layer 39 could then be removed by a subsequent etch process, during which the stop layer 38 protects dielectric layer 36. In an exemplary stack, the protective layer 39 comprises SiO_2, the stop layer 38 comprises Al_2O_3, and the lower layer 36 comprises SiO_2. The terms "etch stop," "protective," and "etch barrier" are alternately used herein to describe layers that shield underlying materials from harm during at least one process step, such as an etch step.

[0036] As previously discussed, in one embodiment of the invention, the further layer comprises Al_2O_3 which is deposited, in accordance with known deposition techniques, over the transparent layer 12. This results in a thin film stack 40 as shown in Figure 5 of the drawings, comprising a substrate 42, an electrode 44, an SiO_2 reflective layer 46 and an Al_2O_3 layer 48.

[0037] Figure 6 of the drawings shows a hysteresis curve 50 for an IMOD device 10 comprising the thin film stack 40. As with the hysteresis curve 30 (Figure 3), the X-axis plots applied voltage in Volts, whereas the Y-axis plots optical response in Volts. The hysteresis curve 50 shows a hysteresis window of 2.8 volts defined as the difference between $V_{actuation}$ (7.8 volts) and $V_{release}$ (5.0 volts). When the individual IMOD's 10 within a reflective display each have a respective reflective layer 14 which demonstrates hysteresis in accordance with the hysteresis curve 50, it will be seen that it is possible to choose a value for the V_{bias} between 5 volts and 7.8 volts which will effectively perform the function of

keeping the reflective layer 14 of each respective IMOD device 10 within the reflective display in its driven condition. In a further embodiment of the invention, the thin film stack may be further modified to include an Al_2O_3 layer above, as well as below, the transparent layer 12. This embodiment is shown in Figure 7 of the drawings, where it will be seen that the thin film stack 60 includes a substrate 62, an electrode 64, a first Al_2O_3 layer 66, an SiO_2 transparent layer 68 and a second Al_2O_3 layer 70.

[0038] Figure 8 of the drawings shows a hysteresis curve 80 for a reflective layer 14 of an IMOD device 10 having the thin film stack 60 shown in Figure 7 of the drawings. As will be seen, the hysteresis window is now wider, i.e., 4.5 volts, being the difference between $V_{actuation}$ (9 volts) and $V_{release}$ (4.5 volts).

[0039] However, other materials that have a high charge trapping density may be used, some of which were discussed above with respect to Figure 5. These materials include AlO_x, which is the off-stoichiometric version of Al_2O_3, silicon nitride (Si_3N_4), its off-stoichiometric version (SiN_x), and tantalum pentoxide (Ta_2O_5) and its off-stoichiometric version (TaO_x). All of these materials have several orders of magnitude higher charge trapping densities than SiO_2 and tend to trap charge of either polarity. Because these materials have a high charge trapping density, it is relatively easy to get charge into and out of these materials, as compared to SiO_2, which has a low charge trapping density and has an affinity for trapping negative charge only.

[0040] Other examples of materials that have a high charge trapping density include the rare earth metal oxides (e.g., hafinium oxide), and polymeric materials. Further, semiconductor materials doped to trap either negative or positive charge may be used to form the further layer above, and optionally below the SiO_2 transparent layer 12.

[0041] Thus far, a technique for manipulating the electromechanical behavior of a MEMS device has been described, wherein charge buildup within the MEMS device is controlled by the use of a charge trapping layer which has a high charge trapping density. However, it is to be understood that the invention covers the use of any charge trapping layer to alter or control the electromechanical behavior of a MEMS device regardless of the charge trapping density thereof. Naturally, the choice of a charge trapping layer whether it be of a high, low, or medium charge trapping density will be dictated by what electromechanical behavior for a MEMS device is being sought.

[0042] In some embodiments the incorporation of metals, in the form of thin layers or aggregates, provide yet another mechanism for manipulating the charge trapping density of a host film in a MEMS device. Structuring the host film by producing voids or creating a variation or periodicity in its material characteristics may also be used to alter the charge trapping characteristics.

[0043] According to another embodiment of the invention, as discussed with respect to Figures 4 and 5 above, an IMOD device 10 includes a chemical barrier layer deposited over the transparent layer 12 in order to protect the transparent layer 12 from damage or degradation due to exposure to chemical etchants in the microfabrication process. For example, in one embodiment, the transparent layer 12 which comprises SiO_2, is protected by an overlying layer comprising Al_2O_3, which acts as a chemical barrier to etchants, for example, XeF_2. In such embodiments, it has been found that when the transparent SiO_2 layer 12 is protected from the etchants, nonuniformities in the SiO_2 are eliminated along with attendant nonuniformities in electromechanical behavior, thus causing the reflective layer 14 within each IMOD device 10 to display hysteresis.

[0044] As discussed, silicon nitride (stoichiometric or non-stochiometric) may be used as the charge trapping layer. Figure 9A depicts a thin film stack 140a in which a dielectric layer 146 comprising silicon nitride is formed above an electrode 144 and a substrate 142. Above the layer 146 of silicon nitride, a stop layer 148 of aluminum oxide is formed to protect the silicon nitride during an etching process. Because silicon nitride has a high charge trapping density and is capable of trapping both positive and negative charge, the use of silicon nitride layer 146 will have a different effect on the electromechanical properties of thin film stack 140, namely on the width of the hysteresis curve, than the use of a silicon oxide layer.

[0045] In alternate embodiments, the thin film stack 140a of Figure 9A can be modified to include a protective layer above the etch stop layer 148. Figure 9B depicts a thin film stack 140b which includes a protective or second etch barrier layer 150a, which in this embodiment comprises an additional layer of silicon nitride. The protective layer 150a is preferably deposited immediately after the deposition of the first etch stop layer 148, as discussed above. In another embodiment, shown in Figure 9C, a thin film stack 140c includes a protective or second etch barrier layer 150b, which comprises silicon oxide.

[0046] The protective layers 150a or 150b are preferably removed by the same etching process which would be used to remove the sacrificial material to form the cavity. Alternatively, the sacrificial material may be removed by a first etch, and the protective layers 150a or 150b may be removed by a second etch. Protective layers such as layers 150a or 150b may comprise silicon oxide or silicon nitride, as previously discussed, but may also comprise, in alternate embodiments, molybdenum, titanium, amorphous silicon, or any other appropriate material. In certain manufacturing processes, the protective layer 150a or 150b may serve to protect aluminum oxide during patterning of the bulk sacrificial layer, as will be better understood from the discussion below of Figures 10A-10H. Because the protective layer 150a,b is preferably removed at the same time as the sacrificial material, the protective layer can also be considered a lower or thin sacrificial layer under an upper or bulk sacrificial material of a different composition.

[0047] The first or patterning etch may be selected such that the bulk sacrificial material (e.g., Mo) is etched at a significantly greater rate than the protective layer 150a,b, (e.g., silicon oxide, silicon nitride, amorphous silicon or titanium) and the second or release etch may be selected such that the protective layer 150a,b is etched at a significantly greater rate than the first etch stop layer 148. In addition, the first etch stop layer 148 (e.g., Al_2O_3) may be further protected if some portion of the protective layer 150a,b remains above the first etch stop layer 148, minimizing the exposure of the etch stop layer to the etchants.

[0048] The additional layer of protection provided by the protective layer 150a,b of Figures 9B and 9C may advantageously minimize both exposure of the etch stop layer 148 to etchants and variations in the amount of exposure of the etch stop layer 148 to a different etch process. It will be understood that, in many manufacturing processes (such as the sacrificial material patterning process described with respect to Figures 10A-10H, below), the protective layer 150a,b, can shield the etch stop layer 148 from the etchants. The etch stop layer 148 can then protect the underlying dielectric layer 146 during a subsequent etch when the second etch barrier layer 150a,b is partially or completely removed, such as the release etch described below with respect to Figures 10F-10G.

[0049] As discussed with respect to Figure 7, an additional layer of aluminum oxide may be provided beneath the dielectric layer 146. Figure 9D depicts such an embodiment, in which a thin film stack 140d includes a layer 152 of aluminum oxide beneath

the dielectric layer 146, in addition to the etch stop layer 148 above the dielectric layer 146. Such an arrangement may modify the electromechanical characteristics of the device, namely by widening the hysteresis curve. While not illustrated, it will be understood that an additional second etch barrier layer or protective layer can also be provided over the first etch stop layer 148 in the arrangement of Figure 9D.

[0050] Figures 10A-10C are cross-sectional views illustrating the initial steps in a process for manufacturing an array of unreleased interferometric modulators (release by removal of the sacrificial material to form interferometric modulators is discussed below with reference to Figures 10F-10H). In Figures 10A-10H, the formation of an array of three interferometric modulators 200 (red subpixel), 210 (green subpixel) and 220 (blue subpixel) will be illustrated, each of the interferometric modulators 200, 210, 220 having a different distance between the lower electrode/mirror 234 and the upper metal mirror layer 238a, 238b, 238c, as indicated in Figure 10H, which shows final configurations. Color displays may be formed by using three (or more) modulator elements to form each pixel in the resulting image. The dimensions of each interferometric modulator cavity (e.g., the cavities 275, 280, 285 in Figure 10H) determine the nature of the interference and the resulting color. One method of forming color pixels is to construct arrays of interferometric modulators, each having cavities of differing sizes, e.g., three different sizes corresponding to red, green and blue as shown in this embodiment. The interference properties of the cavities are directly affected by their dimensions. In order to create these varying cavity dimensions, multiple sacrificial layers may be fabricated and patterned as described below so that the resulting pixels reflect light corresponding to each of the three primary colors. Other color combinations are also possible, as well as the use of black and white pixels.

[0051] Figure 10A illustrates an optical stack 235 similar to those previously discussed (e.g. the optical stack 140b of Figure 9B) formed by first creating an electrode/mirror layer 234 by depositing an indium tin oxide electrode layer on a transparent substrate 231, then depositing a first mirror layer on the indium tin oxide electrode layer, forming a composite layer which will be referred to as the lower electrode layer 234. In the illustrated embodiment, the first mirror layer comprises chrome. Other reflective metals such as molybdenum and titanium may also be used to form the first mirror layer. In Figure 10, although the indium tin oxide electrode layer and the first mirror layer are indicated as a

single layer 234, it will be understood that the electrode layer 234 comprises a first mirror layer which is formed on the indium tin oxide electrode layer. Such a composite structure may be used in electrode layers elsewhere in the application, as well. The viewing surface 231a of the transparent substrate 231 is on the opposite side of the substrate 231 from the lower electrode layer 234. In a process not shown here, the lower electrode layer 234 is patterned and etched to form electrode columns, rows or other useful shapes as required by the display design. As indicated in Figure 10A, the optical stack 235 also includes a dielectric layer 237, which may comprise, for example, silicon oxide or a charge trapping layer, such as silicon nitride or other examples listed above, over the lower electrode layer 234, typically formed after the electrode layer 235 has been patterned and etched. In addition, the optical stack 235 includes a first etch barrier layer 236 over the dielectric or charge trapping layer 237. As noted above, the first etch layer 236 preferably comprises aluminum oxide. A protective or second etch stop barrier layer 244 is deposited over the first etch stop layer 236. In various embodiments, the second etch stop or barrier layer 244 comprises silicon oxide, silicon nitride, molybdenum, titanium, or amorphous silicon.

[0052] Figure 10A further illustrates a first pixel sacrificial layer 246a formed by depositing molybdenum (in the illustrated embodiment) over the optical stack 235 (and thus over the first and second etch barriers 236, 244, the dielectric layer 237, and the lower electrode layer 234). In other arrangements, the sacrificial material can be, e.g., titanium or amorphous silicon, but in any event is selected to be different from and selectively etchable relative to the second etch barrier layer 244. The molybdenum of the illustrated embodiment is etched to form the first pixel sacrificial layer 246a, thereby exposing a portion 244a of the second etch barrier, which overlies a corresponding portion of stop layer 236 that will ultimately be included in the resulting green and blue interferometric modulators 210, 220 (Figure 10H). The thickness of the first sacrificial layer 246a (along with the thicknesses of subsequently deposited layers as described below) influences the size of the corresponding cavity 275 (Figure 10H) in the resulting interferometric modulator 200. The etchant used to remove a portion of first sacrificial layer 246a is preferably chosen so as to not etch the second etch barrier layer 244, or to etch it at a much lower rate than the sacrificial layer 246a. Thus, although the portion 244a of the second etch barrier is exposed, it is preferably as unaffected by these etchants as is possible. An exemplary etchant is a

phosphoric/acetic/nitric acid or "PAN" etchant, which selectively removes Mo relative to the material of the second etch barrier 244 (e.g., silicon oxide, silicon nitride, titanium or amorphous silicon).

[0053] Figures 10B-10C illustrate forming a second pixel sacrificial layer 246b by deposition, masking and patterning over the exposed portion 244a of the second etch barrier layer 244 and the first pixel sacrificial layer 246a. The second pixel sacrificial layer 246b preferably comprises the same sacrificial material as the first pixel sacrificial layer 246a (molybdenum in this embodiment). Accordingly, the same selective etch chemistry can be employed. The second pixel sacrificial layer 246b is patterned and etched as illustrated in Figure 10C to expose a portion 244b of the second etch barrier 244 which overlies a corresponding portion of the first etch barrier 236 that will ultimately be included in the resulting blue interferometric modulator 220 (Figure 10H).

[0054] A third pixel sacrificial layer 246c is then deposited over the exposed portion 236b of the stop layer 236 and the second pixel sacrificial layer 246b as illustrated in Figure 10D. The third pixel sacrificial layer 246c need not be patterned or etched in this embodiment, since its thickness will influence the sizes of all three cavities 275, 280, 285 in the resulting interferometric modulators 200, 210 220 (Figure 10H). The three deposited pixel sacrificial layers 246a, 246b, 246c do not necessarily have the same thickness.

[0055] Figure 10E illustrates forming a second mirror layer 238 by depositing a layer of aluminum-containing metal over the third pixel sacrificial layer. In the illustrated embodiment, the second mirror layer 238 also serves as an electrode. Although the foregoing description refers to certain exemplary materials for the fabrication of the various layers illustrated in Figures 10, it will be understood that other materials may also be used, e.g., as described elsewhere in this application.

[0056] Figure 10F illustrates an intermediate stage of the fabrication process, wherein the mirror layer 238 has been etched to form upper mirror portions 238a,b,c, and an additional layer 246d of sacrificial material has been deposited above the mirror portions 238a,b,c. Thus, pockets of sacrificial material 246a,b,c,d exist between and around the optical stack 235 and the upper mirror portions 238a, 238b, 238c. These pockets are separated by support posts 240a,b,c,d. Figure 10G illustrates removing the sacrificial layers 246a,b,c,d to form the cavities 275, 280, 285, thereby exposing the second etch stop layer

244 underlying the portions 238a,b,c of the mirror layer. In the illustrated embodiment, gaseous or vaporous XeF_2 is used as an etchant to remove the molybdenum sacrificial layers 246a,b,c,d. It will be understood that XeF_2 may serve as a source of fluorine-containing gases such as F_2 and HF, and thus F_2 or HF may be used in place of or in addition to XeF_2 as an etchant for the preferred sacrificial materials.

[0057] The exposed portions 244 of the second etch stop barrier layer 244 and the sacrificial layers 246a,b,c,d will typically be at least partially removed by the release etch. For example, a very thin SiO_2 etch stop layer such as 244 may be removed by an XeF_2 etchant used to removed a molybdenum sacrificial layer. The same is true of silicon nitride, titanium, and amorphous silicon. Typically, all of the second etch barrier layer 244 is removed from over the first etch barrier layer 236 in the cavity regions 275, 280, 285, as shown in Figure 10H. The second etch barrier layer 244 located outside of the cavities, underneath the support posts 240a,b,c,d, has not been removed by the etch, as can be seen in Figure 10H. However, some of the second etch barrier 244 may remain even in the cavity areas after the release etching process (not shown in Figure 10H). Any remaining second etch barrier 244 is transparent and so thin as to not affect optical properties of the device. Additionally, any remaining second etch barrier 244 will typically have a non-uniform thickness, due to differential exposure to the etchants during removal of differential thicknesses of sacrificial material. In a further embodiment, a second etchant is used to remove the second etch barrier layer 244.

[0058] A comparison of Figures 10H and 10E illustrates that the size of the cavity 275 (Figure 10H) corresponds to the combined thicknesses of the three sacrificial layers 246a,b,c. Likewise, the size of the cavity 280 corresponds to the combined thickness of two sacrificial layers 246b,c, and the size of the cavity 285 corresponds to the thickness of the third sacrificial layer 246c. Thus, the dimensions of the cavities 275, 280, 285 vary according to the various combined thicknesses of the three layers 246a,b,c, resulting in an array of interferometric modulators 200, 210, 220 capable of displaying three different colors such as red, green and blue.

[0059] As discussed above, portions of the second etch barrier 244 will be exposed to a greater amount of etchant than other portions of barrier 244. This is due to the repeated deposition and etching of bulk sacrificial layer, as discussed above and depicted in

Figures 10A-10E. While the etchant used in the pattern etching of sacrificial layers 246a and 246b is preferably selected to have as minimal an effect as possible on the second etch barrier layer 244, the etchant may have some undesirable effects on the layer 244. Thus, by the stage of the process depicted in Figure 10G, immediately prior to removal of the bulk sacrificial material through an etching process, the second barrier layer 244 may have varying properties or height in different locations as a result of variations in etchant exposure. However, because the second barrier layer 244 is thin and transparent or completely removed from the cavities during the subsequent release etch, these variations will have a minimal effect on the optical or electromechanical behavior of the finished MEMS device. Because of the protection provided by this second barrier layer 244, the first barrier layer 236, which in certain embodiments is intended to form a part of the finished MEMS device, will be exposed to only a single etching process (the release etch), which typically is highly selective and will not attack Al_2O_3, and variations in the properties of layer 236 can be minimized.

[0060] Importantly, the first etch stop layer 236 protects the underlying dielectric (e.g., SiO_2) or charge trapping layer (e.g., Si_3N_4) during the release etch. The release etch is a prolonged and harmful etch, whose by-products take a long time to diffuse out of the cavities 275, 280, 285. Accordingly, underlying functional layers in the optical stack 235 are protected by the preferred Al_2O_3 etch stop layer 236.

[0061] Figures 11A and 11B depict thin film stacks in which a silicon dioxide dielectric layer is used, and in which a protective layer is formed above the etch stop layer. With respect to Figure 11A, a thin film stack 160a includes a dielectric layer 166 of silicon oxide located above an electrode layer 164 and a substrate 162. Above the dielectric layer 166 is located an etch stop layer 168, which preferably comprises aluminum oxide. A protective or second etch barrier layer 170a of silicon oxide is deposited above the first etch stop layer 168. In another embodiment, shown in Figure 11B, a thin film stack 160b includes a protective or second etch barrier layer 170b, which comprises silicon nitride.

[0062] In certain embodiments, one or more portions of the thin film stack 160a,b layer may be selectively removed. In further embodiments, a protective layer may be provided above the remainder of the etch stop layer, such that a thin film structure similar to

that discussed with respect to Figures 11A and 11B exists over at least part of the electrode. Such an embodiment is described with respect to Figure 11C.

[0063] Figure 11C depicts a pair of interferometric modulators 172 similar to the modulators 10 of Figures 1 and 2, including a thin film stack 160c. The stack 160c comprises a patterened electrode layer 164, a dielectric layer which has been etched to form dielectric portions 166a, 166b, 166b, and an etch stop layer which has been etched to form etch stop portions 168a, 168b, and 168c. The formation of etch stop portions 168a,b,c may be done through the use of a photomask, a first etch to remove the selected portions of the etch stop layer 168, and a subsequent etch to remove the portions of the dielectric layer 166 uncovered by the removal of the etch stop layer 168. A displaceable reflective layer 174 is supported by posts 176, forming interferometric cavities 178.

[0064] Those skilled in the art will also appreciate that, in the illustrated embodiment, portions of the cavity may contain a dielectric constant material, e.g., some or all of the interior walls of the cavity 178 may optionally be coated or covered with a dielectric material. Preferably, this dielectric material is a low dielectric constant material. For example, after etching to form the interferometric modulator illustrated in Figure 11C, a layer of dielectric material may be formed on the bottom electrode 164 over the exposed top surface of the bottom electrode 164. Preferably, any such layer of dielectric material is relatively thin, such that an air gap remains between the top electrode 174 and the dielectric material during both the driven and undriven states. Other interior walls of the cavity 178 that may be coated with a dielectric material include the top electrode 174 and the thin film stack 160c. If the thin film stack 160c includes a top layer of dielectric material, a thin film stack similar to stacks 160a and 160b (of Figures 11A and 11B, respectively) will be created. In embodiments in which a low dielectric constant material is used, preferred materials include porous dielectric materials (e.g. aerogels) and modified silicon oxides. U.S. Patent Nos. 6,171,945 and 6,660,656 describe low dielectric constant materials and methods for making them. Preferred low dielectric constant materials have a dielectric constant of about 3.3 or less, more preferably about 3.0 or less.

[0065] As discussed with respect to Figure 9D, an additional layer of aluminum oxide may be provided beneath the dielectric layer. Figure 11D depicts an embodiment, similar to that depicted in Figure 9D, in which a thin film stack 160d includes a layer 172 of

aluminum oxide beneath the silicon oxide dielectric layer 166, in addition to the etch stop layer 168 above the dielectric layer. As previously discussed, the inclusion of this additional layer may modify the electromechanical characteristics of the device, such as by widening the hysteresis curve.

[0066] As discussed with respect to Figure 10, the deposition of a charge-trapping layer is preferably done after the patterning of the electrode layer. For simplicity, many of the stacks depicted and discussed in the present application depict a continuous electrode layer. However, it will be understood that these are figures are merely schematics, which are not to scale, and which represent those portions of particular thin film stacks which are located over electrodes. The formation of thin film stacks which include patterned electrodes will also result in areas of the stack in which no electrode layer exists between a portion of another layer (such as a silicon oxide layer or a charge trapping layer, e.g. silicon nitride) and the substrate.

[0067] Figures 12A and 12B show another application within a MEMS device wherein a charged trapping layer is used to control the electromagnetic behavior of a structure within the MEMS device.

[0068] Referring to Figure 12A, reference numeral 90 generally indicates a portion of an electrostatic fluid flow system. The electrostatic fluid flow system includes a substrate 92 within which is formed a generally U-shaped channel 94. The channel 94 includes an inner layer 96 of a first material which is selected, for example, because of its chemical and mechanical properties, for example, the material may be particularly wear-resistant, and may demonstrate little degradation due to the flow a fluid within the channel. The channel 94 also includes an outer layer 98 which is selected for its charge-trapping properties, as will be explained in greater detail below.

[0069] The electrostatic fluid flow system 90 also includes pairs of electrodes 100 and 102 which are selectively energized to cause displacement of charge particles within a fluid in the channel 94 in the direction indicated by the arrow 104 in Figure 8b of the drawings. In one embodiment, the outer layer 98 traps charge in the fluid thereby to provide greater control of fluid flow within the system 101. In another embodiment, the layer 98 may trap charge in order to eliminate or to reduce hysteresis effects.

[0070] Referring now to Figure 13 of the drawings, another application of using a charge-trapping layer to alter the electromechanical behavior of a structure within a MEMS device is shown. In Figure 13, reference numeral 120 generally indicates a motor comprising a rotor 122 which is axially aligned and spaced from a stator of 124. As can be seen, the stator 124 is formed on a substrate 126 and includes electrodes 128, which, in use, are energized by a driving mechanism (not shown). The rotor 122 includes a cylindrical portion 130 which is fast with a spindle 132. The rotor 122 may be of a material that may be selected for its mechanical properties, including resistance to wear, but may have undesirable electrical properties in response to input, such as when the electrodes 128 are energized in order to cause rotation of the rotor 122. In order to compensate for these undesirable electrical properties, layers 134 and 136 are deposited on the rotor 122 in order to effectively act as a charge trapping layer to alter the electromechanical behavior of the rotor 122.

[0071] Figures 14A and 14B are system block diagrams illustrating an embodiment of a display device 2040. The display device 2040 can be, for example, a cellular or mobile telephone. However, the same components of display device 2040 or slight variations thereof are also illustrative of various types of display devices such as televisions and portable media players.

[0072] The display device 2040 includes a housing 2041, a display 2030, an antenna 2043, a speaker 2045, an input device 2048, and a microphone 2046. The housing 2041 is generally formed from any of a variety of manufacturing processes as are well known to those of skill in the art, including injection molding, and vacuum forming. In addition, the housing 2041 may be made from any of a variety of materials, including but not limited to plastic, metal, glass, rubber, and ceramic, or a combination thereof. In one embodiment the housing 2041 includes removable portions (not shown) that may be interchanged with other removable portions of different color, or containing different logos, pictures, or symbols.

[0073] The display 2030 of exemplary display device 2040 may be any of a variety of displays, including a bi-stable display, as described herein. In other embodiments, the display 2030 includes a flat-panel display, such as plasma, EL, OLED, STN LCD, or TFT LCD as described above, or a non-flat-panel display, such as a CRT or other tube device, as is well known to those of skill in the art. However, for purposes of describing the present

embodiment, the display 2030 includes an interferometric modulator display, as described herein.

[0074] The components of one embodiment of exemplary display device 2040 are schematically illustrated in Figure 14B. The illustrated exemplary display device 2040 includes a housing 2041 and can include additional components at least partially enclosed therein. For example, in one embodiment, the exemplary display device 2040 includes a network interface 2027 that includes an antenna 2043 which is coupled to a transceiver 2047. The transceiver 2047 is connected to the processor 2021, which is connected to conditioning hardware 2052. The conditioning hardware 2052 may be configured to condition a signal (e.g. filter a signal). The conditioning hardware 2052 is connected to a speaker 2045 and a microphone 2046. The processor 2021 is also connected to an input device 2048 and a driver controller 2029. The driver controller 2029 is coupled to a frame buffer 2028 and to the array driver 2022, which in turn is coupled to a display array 2030. A power supply 2050 provides power to all components as required by the particular exemplary display device 2040 design.

[0075] The network interface 2027 includes the antenna 2043 and the transceiver 2047 so that the exemplary display device 2040 can communicate with one or more devices over a network. In one embodiment the network interface 2027 may also have some processing capabilities to relieve requirements of the processor 2021. The antenna 2043 is any antenna known to those of skill in the art for transmitting and receiving signals. In one embodiment, the antenna transmits and receives RF signals according to the IEEE 802.11 standard, including IEEE 802.11(a), (b), or (g). In another embodiment, the antenna transmits and receives RF signals according to the BLUETOOTH standard. In the case of a cellular telephone, the antenna is designed to receive CDMA, GSM, AMPS or other known signals that are used to communicate within a wireless cell phone network. The transceiver 2047 pre-processes the signals received from the antenna 2043 so that they may be received by and further manipulated by the processor 2021. The transceiver 2047 also processes signals received from the processor 2021 so that they may be transmitted from the exemplary display device 2040 via the antenna 2043.

[0076] In an alternative embodiment, the transceiver 2047 can be replaced by a receiver. In yet another alternative embodiment, network interface 2027 can be replaced by

an image source, which can store or generate image data to be sent to the processor 2021. For example, the image source can be a digital video disc (DVD) or a hard-disc drive that contains image data, or a software module that generates image data.

[0077] Processor 2021 generally controls the overall operation of the exemplary display device 2040. The processor 2021 receives data, such as compressed image data from the network interface 2027 or an image source, and processes the data into raw image data or into a format that is readily processed into raw image data. The processor 2021 then sends the processed data to the driver controller 2029 or to frame buffer 2028 for storage. Raw data typically refers to the information that identifies the image characteristics at each location within an image. For example, such image characteristics can include color, saturation, and gray-scale level.

[0078] In one embodiment, the processor 2021 includes a microcontroller, CPU, or logic unit to control operation of the exemplary display device 2040. Conditioning hardware 2052 generally includes amplifiers and filters for transmitting signals to the speaker 2045, and for receiving signals from the microphone 2046. Conditioning hardware 2052 may be discrete components within the exemplary display device 2040, or may be incorporated within the processor 2021 or other components.

[0079] The driver controller 2029 takes the raw image data generated by the processor 2021 either directly from the processor 2021 or from the frame buffer 2028 and reformats the raw image data appropriately for high speed transmission to the array driver 2022. Specifically, the driver controller 2029 reformats the raw image data into a data flow having a raster-like format, such that it has a time order suitable for scanning across the display array 2030. Then the driver controller 2029 sends the formatted information to the array driver 2022. Although a driver controller 2029, such as a LCD controller, is often associated with the system processor 2021 as a stand-alone Integrated Circuit (IC), such controllers may be implemented in many ways. They may be embedded in the processor 2021 as hardware, embedded in the processor 2021 as software, or fully integrated in hardware with the array driver 2022.

[0080] Typically, the array driver 2022 receives the formatted information from the driver controller 2029 and reformats the video data into a parallel set of waveforms that

are applied many times per second to the hundreds and sometimes thousands of leads coming from the display's x-y matrix of pixels.

[0081] In one embodiment, the driver controller 2029, array driver 2022, and display array 2030 are appropriate for any of the types of displays described herein. For example, in one embodiment, driver controller 2029 is a conventional display controller or a bi-stable display controller (e.g., an interferometric modulator controller). In another embodiment, array driver 2022 is a conventional driver or a bi-stable display driver (e.g., an interferometric modulator display). In one embodiment, a driver controller 2029 is integrated with the array driver 2022. Such an embodiment is common in highly integrated systems such as cellular phones, watches, and other small area displays. In yet another embodiment, display array 2030 is a typical display array or a bi-stable display array (e.g., a display including an array of interferometric modulators).

[0082] The input device 2048 allows a user to control the operation of the exemplary display device 2040. In one embodiment, input device 2048 includes a keypad, such as a QWERTY keyboard or a telephone keypad, a button, a switch, a touch-sensitive screen, a pressure- or heat-sensitive membrane. In one embodiment, the microphone 2046 is an input device for the exemplary display device 2040. When the microphone 2046 is used to input data to the device, voice commands may be provided by a user for controlling operations of the exemplary display device 2040.

[0083] Power supply 2050 can include a variety of energy storage devices as are well known in the art. For example, in one embodiment, power supply 2050 is a rechargeable battery, such as a nickel-cadmium battery or a lithium ion battery. In another embodiment, power supply 2050 is a renewable energy source, a capacitor, or a solar cell, including a plastic solar cell, and solar-cell paint. In another embodiment, power supply 2050 is configured to receive power from a wall outlet.

[0084] In some implementations control programmability resides, as described above, in a driver controller which can be located in several places in the electronic display system. In some cases control programmability resides in the array driver 2022. Those of skill in the art will recognize that the above-described optimization may be implemented in any number of hardware and/or software components and in various configurations.

[0085] Although the present invention has been described with reference to specific exemplary embodiments, it will be evident that the various modification and changes can be made to these embodiments without departing from the broader spirit of the invention as set forth in the claims. Accordingly, the specification and drawings are to be regarded in an illustrative sense rather than in a restrictive sense.

WHAT IS CLAIMED IS:

1. A MEMS device having a substrate comprising:

an electrode layer formed over the substrate;

a dielectric layer formed over the electrode layer;

a first etch barrier layer formed over the dielectric layer;

a second etch barrier layer formed over the first etch barrier layer; and

a moving layer located above the second etch barrier.

2. The device of Claim 1, additionally comprising a cavity located between the second etch barrier layer and the moving layer.

3. A method of operating the device of Claim 2, the method comprising applying a first signal to the electrode layer and applying a second signal to the movable layer, causing the movable layer to move within the cavity.

4. The device of Claim 1, additionally comprising a sacrificial layer located between the second etch barrier layer and the moving layer.

5. The device of Claim 4, wherein the second etch barrier layer comprises a material resistant to an etch used to pattern the sacrificial layer.

6. The device of Claim 4, wherein the first etch barrier layer comprises a material resistant to an etch used to remove the sacrificial layer.

7. The device of Claim 1, wherein the second etch barrier layer comprises a material substantially resistant to a phosphoric/acetic/nitric acid etch.

8. The device of Claim 1, wherein the first etch barrier layer comprises a material substantially resistant to a XeF_2 etch.

9. The device of Claim 1, wherein the second etch barrier layer comprises silicon oxide.

10. The device of Claim 9, wherein the dielectric layer comprises silicon oxide and the first etch barrier layer comprises aluminum oxide.

11. The device of Claim 9, wherein the dielectric layer comprises a charge trapping layer.

12. The device of Claim 1, wherein the second etch barrier layer comprises silicon nitride.

13. The device of Claim 12, wherein the first etch barrier layer comprises aluminum oxide, and wherein the dielectric layer comprises a material selected from the group of: silicon oxide and silicon nitride.

14. The device of Claim 1, wherein the second etch barrier layer comprises a material selected from the group of titanium, molybdenum, and amorphous silicon.

15. The device of Claim 1, wherein the second etch barrier layer has a varying thickness over the surface of the first etch barrier layer.

16. The device of Claim 15, wherein the second etch barrier covers only a portion of the first etch barrier layer.

17. The device of Claim 1, additionally comprising:

a processor that is in electrical communication with at least one of said electrode layer and said movable layer, said processor being configured to process image data; and

a memory device in electrical communication with said processor.

18. The device of Claim 17, additionally comprising a driver circuit configured to send at least one signal to at least one of said electrode layer and said movable layer.

19. The device of Claim 18, additionally comprising a controller configured to send at least a portion of said image data to said driver circuit.

20. The device of Claim 17, further comprising an image source module configured to send said image data to said processor.

21. The device of Claim 20, wherein said image source module comprises at least one of a receiver, transceiver, and transmitter.

22. The device of Claim 17, further comprising an input device configured to receive input data and to communicate said input data to said processor.

23. A MEMS device, comprising:

means for conducting an electrical signal;

means for supporting said conducting means;

means for electrically insulating said conducting means;

first protecting means for protecting said insulating means;

second protecting means for protecting said first protecting means; and

means for defining a cavity having a variable size.

24. The device of Claim 23 wherein:

the supporting means comprises a transparent substrate;

the conducting means comprises an electrode layer formed over the transparent substrate; and

the means for defining a cavity comprises a movable layer spaced apart from the second protecting means.

25. The device of Claim 23 or 24, wherein the insulating means comprises a dielectric layer formed over the conducting means.

26. The device of Claim 23, 24, or 25, wherein the first protecting means comprises a first etch barrier layer formed over the insulating means.

27. The device of Claim 23, 24, 25, or 26, wherein the second protecting means comprises a second etch barrier layer formed over said first protecting means.

28. A method of manufacturing a MEMS device, comprising:

depositing an electrode layer on a substrate;

depositing a dielectric layer over the electrode layer;

depositing an etch stop layer over the dielectric layer; and

depositing a protective layer over the etch stop layer.

29. The method of Claim 28, wherein the etch stop layer comprises aluminum oxide, and wherein the dielectric layer comprises a material selected from the group of silicon nitride and silicon oxide.

30. The method of Claim 28, wherein the etch stop layer comprises aluminum oxide, additionally comprising depositing a second layer of aluminum oxide over the electrode layer, wherein the dielectric layer is deposited over the second layer of aluminum oxide.

31. The method of Claim 28, wherein the etch stop layer comprises aluminum oxide, the method additionally comprising:

depositing at least a first sacrificial layer over the protective layer;

depositing a reflective layer over the sacrificial layer; and

performing a release etch to remove the first sacrificial layer, thereby creating an interferometric cavity.

32. The method of Claim 31, wherein performing the release etch comprises etching both the first sacrificial layer and the protective layer relative to the etch barrier layer.

33. The method of Claim 31, wherein performing the release etch comprises etching the first sacrificial layer relative to the protective layer.

34. The method of Claim 33, additionally comprising selectively etching the protective layer relative to the etch barrier layer, wherein etching the protective layer is done after performing the release etch.

35. The method of Claim 31, additionally comprising:

performing a preliminary etch to remove a portion of the first sacrificial layer, thereby exposing a portion of the protective layer; and

depositing at least a second sacrificial layer over the first sacrificial layer; wherein performing a release etch comprises removing the second sacrificial layer.

36. The method of Claim 35, wherein the protective layer comprises a material selected from the group of: silicon oxide, silicon nitride, amorphous silicon, molybdenum, and titanium.

37. The method of Claim 35, wherein performing the preliminary etch removes at least a portion of the protective layer.

38. The method of Claim 35, wherein performing the preliminary etch comprises selectively etching the first sacrificial layer relative to the protective layer.

39. A MEMS device manufactured by the process of Claim 28.

40. A method of manufacturing a MEMS device, comprising:

depositing an electrode layer on a substrate;

depositing a first dielectric layer over the electrode layer;

depositing second dielectric layer on the first dielectric layer;

depositing a third dielectric layer on the second dielectric layer;

depositing a first sacrificial layer on the third dielectric layer;

performing a preliminary etch to remove a portion of said first sacrificial layer, thereby exposing at least a portion of the third dielectric layer; and

depositing a second sacrificial layer on the remaining portion of the first sacrificial layer and the exposed portion of the third dielectric layer.

41. The method of Claim 40, wherein the first dielectric layer comprises at least one of silicon oxide and silicon nitride, and wherein the second dielectric layer comprises aluminum oxide.

42. The method of Claim 40, wherein the third dielectric layer comprises a protective layer.

43. The method of Claim 42, wherein the protective layer comprises at least one of silicon oxide, silicon nitride, amorphous silicon, molybdenum, and titanium.

44. The method of Claim 40, wherein the preliminary etch selectively etches the first sacrificial layer relative to the third dielectric layer.

45. The method of Claim 40, additionally comprising:

forming a reflective layer over the second sacrificial layer;

patterning the reflective layer to form at least two movable layers; and

etching the first and second sacrificial layers, thereby forming at least a first cavity and a second cavity, wherein a height of the first cavity is different from a height of the second cavity.

46. The method of Claim 45, wherein etching the first and second sacrificial layers comprises etching said first and second layers relative to the second dielectric layer.

47. The method of Claim 46, wherein etching the first and second sacrificial materials removes at least a portion of the third dielectric layer.

48. A MEMS device formed by the method of Claim 40.

49. A MEMS device, comprising:

a substrate;

an electrode layer located over a substrate;

a charge-trapping layer located over the electrode layer, wherein the charge-trapping layer is configured to trap both positive and negative charge; and

a first etch barrier layer located over the charge-trapping layer.

50. The device of Claim 49, wherein the first etch barrier layer comprises aluminum oxide.

51. The device of Claim 49, wherein the charge-trapping layer comprises at least one of silicon nitride and tantalum pentoxide.

52. The device of Claim 49, additionally comprising a second etch barrier layer located over the first etch barrier layer.

53. The device of Claim 52, wherein the second etch barrier layer comprises a material selected from the group of: silicon oxide, silicon nitride, amorphous silicon, molybdenum, and titanium.

54. The method of Claim 52, wherein the second etch barrier layer comprises a material which is substantially resistant to a to a phosphoric/acetic/nitric acid etch

55. The method of Claim 49, wherein the first etch barrier layer comprises a material which is substantially resistant to a XeF_2 etch.

56. A method of manufacturing a MEMS device, comprising:

depositing an electrode layer on a substrate;

depositing a charge-trapping layer over the electrode layer, wherein the charge-trapping layer is configured to trap both positive and negative charge; and

depositing a first etch barrier layer over the charge-trapping layer.

57. The method of Claim 56, wherein the first etch barrier layer comprises aluminum oxide, and wherein the charge-trapping layer comprises a material selected from a group of silicon nitride and tantalum pentoxide.

58. The method of Claim 56, additionally comprising:

depositing a second etch barrier layer on the first etch barrier layer;

depositing a first layer of sacrificial material on the second etch barrier layer;

performing a first etch to remove a portion of the first layer of sacrificial material, thereby exposing a portion of the second etch barrier layer;

depositing at least a second layer of sacrificial material on the first layer of sacrificial material and over the exposed portion of the second etch barrier layer;

depositing an electrode over the first and second layers of sacrificial material; and

performing a second etch to remove the first and second layers of the sacrificial material, thereby forming an interferometric cavity.

59. The method of Claim 58, wherein the first etch selectively etches the first layer of sacrificial material relative to the second etch barrier layer.

60. The method of Claim 58, wherein the second etch selectively etches the first and second layers of sacrificial material relative to the first etch barrier layer.

61. The method of Claim 58, wherein the second etch barrier layer comprises a material selected from the group of: silicon oxide, silicon nitride, amorphous silicon, molybdenum, and titanium.

62. The method of Claim 58, wherein the first etch is performed using an etchant to which the second etch barrier layer is more resistant than the first sacrificial layer.

63. The method of Claim 58, wherein the second etch barrier is at least partially removed during the second etch and the first etch barrier layer is resistant to the second etch.

64. A MEMS device manufactured by the method of Claim 56.

65. A MEMS device, comprising:

a substrate;

an electrode layer formed over the substrate;

a layer of silicon nitride formed on the electrode layer; and

a layer of aluminum oxide formed on the layer of silicon nitride.

66. The device of Claim 65, additionally comprising a movable layer formed over the layer of aluminum oxide.

67. The device of Claim 66, additionally comprising a layer of sacrificial material located between the movable layer and the layer of aluminum oxide.

68. The device of Claim 66, additionally comprising a cavity located between the movable layer and the layer of aluminum oxide.

69. A method of operating the device of Claim 68, the method comprising applying a first signal to the electrode layer and applying a second signal to the movable layer, causing the movable layer to move within the cavity.

70. The device of Claim 66, wherein the device is an interferometric modulator.

71. The device of Claim 70, additionally comprising an additional layer formed on the layer of aluminum oxide, wherein the additional layer comprises a material selected from the group of: silicon oxide and silicon nitride.

72. The device of Claim 71, wherein the additional layer is over the layer of aluminum oxide and under posts that support the moveable layer above the cavity.

73. The device of Claim 65, additionally comprising a second layer of aluminum oxide, wherein the second layer of aluminum oxide is formed over the electrode layer, and wherein the silicon nitride layer is formed on the second layer of aluminum oxide.

74. A MEMS device, comprising:

means for conducting an electrical signal;

means for supporting said conducting means;

means for trapping both positive and negative charge; and

means for protecting said means for trapping charge.

75. The device of Claim 74, wherein the supporting means comprises a transparent substrate.

76. The device of Claim 74 or 75, wherein the means for conducting an electrical signal comprises an electrode layer formed over the supporting means.

77. The device of Claim 74, 75, or 76, wherein the charge trapping means comprises a layer of charge-trapping material formed over the conducting means, the charge-trapping material configured to trap both positive and negative charge.

78. The device of Claim 74, 75, 76, or 77, wherein the protecting means comprises an etch barrier layer formed over the charge trapping means.