

DEDICATED MECHANISM FOR PAGE-MAPPING IN A GPU

ABSTRACT

Circuits, methods, and apparatus that reduce or eliminate system memory accesses to retrieve address translation information. In one example, these accesses are reduced or eliminated by pre-populating a graphics TLB with entries that are used to translate virtual addresses used by a GPU to physical addresses used by a system memory. Translation information is maintained by locking or restricting entries in the graphics TLB that are needed for display access. This may be done by limiting access to certain locations in the graphics TLB, by storing flags or other identifying information in the graphics TLB, or by other appropriate methods. In another example, memory space is allocated by a system BIOS for a GPU, which stores a base address and address range. Virtual addresses in the address range are translated by adding them to the base address.

Figure 1