

Description

The invention relates to an amplifier arrangement comprising

- a first and a second output transistor each having a first main terminal, a second main terminal and a control terminal, whose main current paths are arranged in series between two power supply terminals and are further coupled to an output connecting a load,
- drive means for driving the first and the second transistor, said drive means having a first input for applying an input signal, a second input, a first output which is coupled to the control terminal of the first transistor and a second output which is coupled to the control terminal of the second transistor,
- quiescent current means for causing a quiescent current to flow through the first and the second output transistor, said quiescent current means having first and second current measuring means for generating a first and a second measuring current which are a measure of the current flowing through the first and the second output transistor, respectively, and having feedback means for controlling the quiescent current flowing through the first and the second output transistor by way of the first and the second measuring current.

In the description and the appendant Claims the first main terminal, the second main terminal and the control terminal are identical to the drain, the source and the gate, respectively, in the case of unipolar transistors, and to the collector, the emitter and the base, respectively, in the case of bipolar transistors.

An amplifier arrangement of this type can be generally used as a power amplifier arrangement and is particularly suitable as an output amplifier in audio circuits.

Such an amplifier arrangement is known from European Patent Application EP-A-0,217,431.

The first and the second output transistor are push-pull driven by the non-inverting and the inverting output, respectively, of a voltage-to-current converter which has a non-inverting input to which the input voltage is applied and an inverting input which is connected to the output of the amplifier arrangement.

The amplifier arrangement is of the class AB type because a given quiescent current flows through the two output transistors. The means for adjusting the value of this quiescent current comprise a measuring circuit for each of the two output transistors for measuring the current through the relevant output transistor. This measuring current is converted across a first diode into a voltage which is applied to the inverting input of an amplifier. A reference voltage generated across a second diode is applied to the non-inverting input thereof. In the absence of an input signal to drive the output transistors, the output of the amplifier controls the relevant output transistor in such a way that the voltage at the inverting input of this amplifier will become equal to the reference voltage. When driving one of the two output transistors, the current through the driven transistor increases and the quiescent current through the non-driven transistor decreases. The known arrangement is, however, adapted in such a way that the non-driven transistor is fully turned off. If the relevant transistor is subsequently driven, it should first be turned on, which causes cross-over distortion.

It is therefore an object of the invention to provide an amplifier arrangement having an improved quiescent current control. According to the invention, an amplifier arrangement of a type described in the opening paragraph is characterized in that the feedback means comprise

- a first differential amplifier having a third and a fourth transistor each having a control terminal, a first main terminal and a second main terminal, the second main terminals being coupled to a common point which is coupled to a first current source, the control terminal of the third transistor being coupled to a first point for conveying a voltage which is proportional to the first measuring current and the control terminal of the fourth transistor being coupled to a second point for conveying a voltage which is proportional to the second measuring current,
- a reference circuit comprising a second current source and a fifth transistor having a first main terminal, a second main terminal and a control terminal which is coupled to the first main terminal, and
- a second differential amplifier having a sixth and a seventh transistor each having at least one first main terminal, at least one second main terminal and a control terminal, the control terminal of the sixth transistor being coupled to the second main terminal of the fifth transistor, the control terminal of the seventh transistor being coupled to the common point of the first differential amplifier, and two of the first main terminals of the sixth and the seventh transistor being coupled to the first and the second output of the drive means.

The structure of the negative feedback means according to the invention causes the quiescent current through the non-driven output transistor to be controlled to a substantially constant value, which keeps this transistor conducting independent of the extent to which the other output transistor is driven. This prevents the one output transistor from being turned off when the other output transistor is fully turned on.

Consequently, the cross-over distortion caused thereby is considerably reduced.

The further structure of the negative feedback means is determined by the conductivity type of the first and the second output transistor. If the first and the second output transistor are of the same conductivity type, an embodiment of the amplifier arrangement may be further characterized in that

- the sixth and the seventh transistor each have two first main terminals, and in that
- the one first main terminal of the sixth transistor is coupled to the first output of the drive means and the other first main terminal of the sixth transistor is coupled to the second output of the drive means.

A further embodiment of such an amplifier arrangement may be characterized in that the first current measuring means include an eighth transistor having a first main terminal, a second main terminal and a control terminal, the control terminal and the second main terminal being coupled to the control terminal and the second main terminal, respectively, of the first output transistor and in that the second current measuring means include a ninth transistor having a first main terminal, a second main terminal and a control terminal, the control terminal and the second main terminal being coupled to the control terminal and the second main terminal, respectively, of the second output transistor. This embodiment may be further characterized in that the second main terminal of the eighth transistor is coupled to the second main terminal of the first output transistor by means of a first resistor and in that the second main terminal of the ninth transistor is coupled to the second main terminal of the second output transistor by means of a second resistor. The first and the second resistor limit the maximum current through the eighth and the ninth transistor, which prevents these transistors from damage when the output transistors are fully turned on.

Another embodiment of such an amplifier arrangement may be characterized in that

- the first main terminal of the eighth transistor is coupled to a first power supply terminal by means of a tenth transistor having a first main terminal, a second main terminal and a control terminal, the first main terminal of the tenth transistor being coupled to its control terminal and the second main terminal constituting the first point for conveying a voltage which is proportional to the first measuring current,
- the first main terminal of the ninth transistor is coupled to the first power supply terminal by means for an eleventh transistor having a first main terminal, a second main terminal and a control terminal, the first main terminal of the eleventh transistor being coupled to its control terminal and the second main terminal constituting the second point for conveying a voltage which is proportional to the second measuring current, and in that
- the first main terminal of the fifth transistor is coupled to the first power supply terminal by means of a twelfth transistor having a first main terminal and a second main terminal and a control terminal, the first main terminal being coupled to its control terminal. The currents generated by the first and second current measuring means across the tenth and the eleventh transistor are converted into voltages which are proportional thereto and which are applied to the control terminals of the third and the fourth transistor.

Yet a further embodiment of such an amplifier arrangement may be characterized in that the drive means include a third differential amplifier having a thirteenth and a fourteenth transistor each having a first main terminal, a second main terminal and a control terminal, the control terminal and the first main terminal of the thirteenth transistor being coupled to the first input and the first output, respectively, of the drive means and the control terminal and the second main terminal of the fourteenth transistor being coupled to the second input and the second output, respectively, of the drive means. This embodiment may be further characterized in that a first capacitor is arranged between the first input and the first output of the drive means and in that the first input of the drive means is coupled to an input of a fifteenth transistor arranged as a voltage follower, an output of which is coupled to the second output of the drive means by means of a second capacitor. The first capacitor ensures a frequency compensation for obtaining a stable gain and the second capacitor ensures a direct signal transmission to the control terminal of the second output transistor in the case of high frequencies. This results in the phase shifting being reduced, thus improving the stability of the amplifier arrangement.

Yet another embodiment of such an amplifier arrangement may be characterized in that the first output of the drive means is coupled to a non-inverting input of an amplifier, an inverting input of which is coupled to the output of the amplifier arrangement and an output of which is coupled to the control terminal of the first output transistor. This amplifier constitutes a negative feedback from the output to the control terminal of the first output transistor so that the non-linearities caused by this transistor are reduced. This negative feedback is effective at all drive conditions because it is ensured that the first output transistor remains conducting in the amplifier arrangement according to the invention.

In another embodiment this amplifier may be characterized in that it is constituted by a fourth differential amplifier having a sixteenth and a seventeenth transistor each having a control terminal and a

first and a second main terminal, the control terminal of the sixteenth transistor being coupled to the non-inverting input and the control terminal of the seventeenth transistor being coupled to the inverting input, the first main terminal of the seventeenth transistor being coupled to the output of the amplifier and to a current source.

5 yet another embodiment may be characterized in that the first output of the drive means is coupled to an input of a voltage follower circuit, an output of which is coupled to the control terminal of the first output transistor by means of a third capacitor. At high frequencies the third capacitor ensures a direct signal transmission from the drive means to the control terminal of the first output transistor and thereby eliminates the phase shift occurring in the amplifier at high frequencies. This improves the stability of the amplifier
10 arrangement.

The amplifier arrangement according to the invention may be suitably formed with bipolar transistors. In that case the negative feedback means control the current through the first and the second output transistor in such a way that the harmonic means value of these currents is maintained substantially constant. The amplifier arrangement may, however, also be formed with field-effect transistors. The negative feedback
15 means then control the currents through the first and the second output transistor in such a way that a relationship which complies with the equation for a circle is present between these currents.

In an amplifier arrangement according to the invention, the first and the second output transistor may be alternatively of the opposite conductivity type instead of the same conductivity type. The amplifier arrangement may then be further characterized in that

- the sixth and the seventh transistor each have a first main terminal and in that
- the first main terminal of the sixth transistor is coupled to the first output of the drive means and the first main terminal of the seventh transistor is coupled to the second output of the drive means.

This embodiment is very suitable for low power supply voltages. A further embodiment of such an amplifier arrangement may be characterized in that

- 25 - the first current measuring means include an eighth transistor having a first main terminal, a second main terminal and a control terminal, the control terminal being coupled to the control terminal of the first output transistor and the second main terminal being coupled to the second main terminal of the first output transistor by means of a first resistor, said second main terminal of the eighth transistor constituting the first point for conveying a voltage which is proportional to the first measuring current,
- 30 - the second current measuring means include a ninth transistor having a first main terminal, a second main terminal and a control terminal, the control terminal being coupled to the control terminal of the second output transistor and the second main terminal being coupled to the second main terminal of the second output transistor by means of a second resistor,
- the first main terminal of the ninth transistor is coupled to a first power supply terminal by means of a
35 third resistor, said first main terminal of the ninth transistor constituting the second point for conveying a voltage which is proportional to the second measuring current, and in that
- the first main terminal of the fifth transistor is coupled to the first power supply terminal by means of a fourth resistor.

The first measuring current flows through the first resistor and the voltage across this resistor is directly applied to the control terminal of the third transistor. The second measuring current is converted across the third resistor into a voltage which is proportional thereto and which is applied to the control terminal of the fourth transistor.

Yet another embodiment of such an amplifier arrangement may be characterized in that

- 45 - the drive means include a third differential amplifier with a tenth transistor having a first main terminal, a second main terminal and a control terminal and an eleventh transistor having two first main terminals, two second main terminals and a control terminal, the control terminal of the tenth transistor being coupled to the first input of the drive means and the control terminal and the two first main terminals being coupled to the second input and the first and the second output, respectively, of the drive means. This embodiment may be further characterized in that a first capacitor is arranged
50 between the first input and the first main terminal of the tenth transistor and in that
- a second capacitor is arranged between the control terminal of the first output transistor and the output, and in that
- a third capacitor is arranged between the control terminal of the second output transistor and the output. These capacitors enhance the stability of the amplifier arrangement.

55 This amplifier arrangement may be suitably formed with bipolar transistors. The negative feedback means then control the currents through the first and the second output transistor in such a way that the harmonic mean value of these currents is maintained substantially constant. This amplifier arranged can of course also be formed with field-effect transistors instead of bipolar transistors.

The invention will now be described in greater detail, by way of example, with reference to the accompanying drawings in which

Fig. 1 shows a first embodiment of an amplifier arrangement according to the invention,

Fig. 2a shows the relationship between the currents through the output transistors,

Fig. 2b shows the waveforms of the currents through the output transistors as a function of the output voltage of the amplifier,

Fig. 3 shows a second embodiment of an amplifier arrangement according to the invention,

Fig. 4 shows a third embodiment of an amplifier arrangement according to the invention,

Fig. 5 shows a fourth embodiment of an amplifier arrangement according to the invention,

Fig. 6a shows the relationship between the measuring currents in the circuit arrangement of Fig. 5,

Fig. 6b shows the waveforms of the quiescent currents as a function of the output voltage for the amplifier arrangement of Fig. 5,

Fig. 7 shows a fifth embodiment of an amplifier arrangement according to the invention, and

Fig. 8 shows the waveforms of the currents through the output transistors as a function of the output voltage for the amplifier arrangement of Fig. 7.

Fig. 1 shows a first embodiment of an amplifier arrangement according to the invention. The arrangement comprises a first output transistor T_1 and a second output transistor T_2 whose collector-emitter paths are arranged in series between a first power supply terminal 1 and a second power supply terminal 2. The emitter of transistor T_1 and the collector of transistor T_2 are connected to an output 3 of the amplifier arrangement to which a load Z_1 is connected.

The amplifier arrangement also comprises drive means 10 for push-pull driving of the first and the second output transistor T_1 , T_2 . The drive means 10 comprise a differential amplifier having two transistors T_{11} and T_{12} whose emitters are connected to a common point which is connected to the power supply terminal 2 by means of a current source $I_1 = I$. The base of transistor T_{11} is connected to a first input 4 to which an input voltage V_{in} is applied. This signal originates from an input stage which may have a conventional structure such as that of a $\mu A741$ -input stage. The base of transistor T_{12} is connected to a second input 5 conveying a reference voltage V_{ref} . The collector of transistor T_{11} is connected to a first output 6 which is coupled to the base of transistor T_1 and to the collector of transistor T_{13} constituting a variable current source I_5 . Similarly, the collector of transistor T_{12} is connected to a second output 7 which is coupled to the base of transistor T_2 and is connected to the collector of a transistor T_{14} constituting a variable current source I_6 .

The current sources I_5 and I_6 form part of quiescent current means for causing a quiescent current to flow through the output transistors T_1 and T_2 in order to obtain a class AB adjustment of the amplifier arrangement. These quiescent current means have first current measuring means 20 which are constituted by a transistor T_3 whose base-emitter junction is arranged in series with a first resistor R_1 parallel to the base-emitter junction of transistor T_1 . The collector current of transistor T_3 is a measure of the collector current of transistor T_1 and is determined by the ratio of the emitter surfaces of the transistors T_1 and T_3 and the resistance of resistor R_1 . In order to minimize the dissipation of the arrangement, the emitter surface of transistor T_3 is preferably chosen to be much smaller than that of transistor T_1 . The resistor R_1 limits the maximum current through transistor T_3 to a safe value so as to prevent this transistor from being damaged when transistor T_1 is fully turned on. It is to be noted that the resistor R_1 may in principle be dispensed with. The quiescent current means also have second current measuring means 30 which are similarly provided with a transistor T_4 whose base-emitter junction in series with a resistor R_2 is arranged parallel to the base-emitter junction of transistor T_2 . The collector current of transistor T_4 is a measure of the current flowing through transistor T_2 . The quiescent current means also comprise negative feedback means 40 which keep the harmonic mean value of the measuring currents supplied by the first and second measuring means 20 and 30 and hence the currents through the first and the second output transistor T_1 and T_2 substantially equal to a reference value. The negative feedback means 40 comprise a first differential amplifier having two transistors T_5 and T_6 whose emitters are connected to a common point 8 which is connected to the second power supply terminal 2 by means of a current source $I_2 = 2I_0$. The base 11 of transistor T_5 is connected to the first power supply terminal via a transistor T_7 arranged as a diode and to the collector of transistor T_3 . Similarly, the base 12 of transistor T_6 is connected to the first power supply terminal 1 via a transistor T_8 arranged as a diode and to the collector of transistor T_4 . The negative feedback means 40 also comprise a reference circuit which is constituted by a current source $I_3 = I_0$ whose output 9 is connected to the first power supply terminal 1 via two series-arranged transistors T_9 and T_{10} arranged as diodes. The negative feedback means 40 also comprise a second differential amplifier having two transistors T_{13} and T_{14} whose base-emitter junctions are arranged in parallel and two transistors T_{15} and T_{16} whose base-emitter junctions are also arranged in parallel. The emitters of the transistors T_{13} -

T₁₅ are connected to a common point which is connected to the positive power supply terminal 1 by means of a current source I₄ = 2I. The common base of the transistors T₁₅ and T₁₆ is connected to the point 8 of the differential amplifier T₅, T₆. The collectors of the transistors T₁₅ and T₁₆ are connected to the second power supply terminal 2. The common base of the transistors T₁₃ and T₁₄ is connected to the output 9 of current source I₃. The collector of transistor T₁₃ is connected to the first output 6 and the collector of transistor T₁₄ is connected to the second output 7 of the drive means 10. Transistor T₁₃ constitutes a variable current source I₅ and transistor T₁₄ constitutes a variable current source I₆.

It is to be noted that the transistors T₁₃ and T₁₄ as well as the transistors T₁₅ and T₁₆ may be replaced by one single transistor having a double collector.

The operation of the arrangement may be explained as follows. The class AB adjustment affects the bases of the output transistors T₁ and T₂ as a common mode signal, whilst the signal to be amplified affects the bases of these transistors as a difference mode signal. In the means 40 a first translinear loop can be distinguished which is constituted by the transistors T₅-T₈. The following relation holds for this loop:

$$V_{BE7} + V_{BE5} = V_{BE8} + V_{BE6} \quad (1)$$

in which V_{BE} is the base-emitter voltage of the relevant transistor. By means of the known exponential relation between the base-emitter voltage and the collector current of a transistor and the assumption that the transistors T₅-T₈ have identical emitter surfaces, this equation results in :

$$I_{S1} \cdot I_0(1+a) = I_{S2} \cdot I_0(1-a) \quad (2)$$

in which I_{S1} = the first measuring current flowing through transistor T₇ and being supplied by the first measuring means 20,

I₂ = the second measuring current flowing through transistor T₈ and being supplied by the second measuring means 30 and

a₀ = the signal current through the transistors T₅ and T₆ determined by a difference in the first and the second measuring current I_{S1} and I_{S2}.

It follows from this equation that

$$\frac{I_{S2}}{I_{S1}} = \frac{1+a}{1-a} \quad \text{or} \quad a = \frac{I_{S2} - I_{S1}}{I_{S2} + I_{S1}} \quad (3)$$

In the means 40 a second translinear loop may also be distinguished which is constituted by the transistors T₈, T₆, T₁₆, T₁₃, T₁₀ and T₉. The following equation holds for this loop:

$$V_{BE8} + V_{BE6} + V_{BE13} = V_{BE9} + V_{BE10} + V_{BE16} \quad (4)$$

By means of the known exponential transistor equation and again assuming that the transistors have identical emitter surfaces, this equation results in

$$I_{S2} \cdot I_0(1-a) \cdot \frac{I(1+Z)}{2} = I_0^2 \cdot \frac{I(1-Z)}{2} \quad (5)$$

in which ZI = the signal current through the transistors T₁₃ and T₁₆ determined by a voltage difference between the bases 8 and 9. It follows that

$$I_0 \cdot \frac{1-Z}{1+Z} = I_{S2}(1-a) \quad (6)$$

Filling in equation 3, this results in

$$I_0 \cdot \frac{1-Z}{1+Z} = \frac{2I_{S1} \cdot I_{S2}}{I_{S1} + I_{S2}} \quad (7)$$

or

$$Z = \frac{I_0(I_{S1} + I_{S2}) - 2I_{S1} \cdot I_{S2}}{I_0 \cdot (I_{S1} + I_{S2}) + 2I_{S1} \cdot I_{S2}} \quad (8)$$

The collector current of transistor T_{13} is equal to

$$I_5 = I \left(\frac{1+Z}{2} \right).$$

Since transistor T_{14} is arranged in parallel with transistor T_{13} , the collector current of transistor T_{14} is also equal to

$$I_6 = I \left(\frac{1+Z}{2} \right).$$

In the absence of an input voltage V_{in} at the input 4 of the drive means 10 the current I of current source I_1 will be evenly distributed over the transistors T_{11} and T_{12} so that a direct current $\frac{I}{2}$ flows through each of these transistors. These direct currents are compensated by the direct currents $\frac{I}{2}$ which flow through the transistors T_{13} and T_{14} . Consequently, a current $\frac{ZI}{2}$ flows via output 6 to the base of transistor T_1 and an equally large current $\frac{ZI}{2}$ flows via output 7 to the base of transistor T_2 . A quiescent current resulting in a first and an equal second measuring current I_{S1} and I_{S2} will therefore flow through transistors T_1 and T_2 . The transistors T_1 and T_2 are now driven in such a way that the voltage at the point 8 determined by these measuring currents is equal to the reference voltage at the point 9. For the value of the quiescent current flowing through transistors T_1 and T_2 the following applies. The current gain factors of the transistors T_1 and T_2 are very large. This means that the base currents $\frac{ZI}{2}$ are very small and may be assumed to be approximately zero. With $I_{S1} = I_{S2}$ it follows from equation 7 or 8 for the measuring currents flowing in the absence of an input voltage V_1 that:

$$I_{S1} = I_{S2} = I_0 \quad (9)$$

For relatively small currents the voltage across the resistors R_1 and R_2 is small with respect to the base-emitter voltages of the transistors T_3 and T_4 . For a ratio of base-emitter surfaces of the transistors T_1 , T_3 and T_2 , T_4 which is equal to N it holds for the value of the quiescent currents flowing through the transistors T_1 and T_2 that;

$$I_1 = I_2 = N I_0 \quad (10)$$

In the case of an input voltage V_{in} at the input 4 which is, for example, smaller than the reference voltage V_{ref} at the input 5, the current through transistor T_{12} increases and the current through transistor T_{11} decreases. Consequently, the base current of transistor T_1 increases and that of transistor T_2 decreases so that transistor T_1 is further turned on and transistor T_2 is further turned off. As a result, the measuring current I_{S1} through transistor T_3 increases and the measuring current I_{S2} through transistor T_4 decreases. Consequently, the voltage across the base-emitter junction of transistor T_7 increases and the voltage across the base-emitter junction of transistor T_8 decreases. At already relatively small currents transistor T_5 will therefore be turned off so that transistor T_6 will start behaving as an emitter follower. The voltage at the

common point 8 thus increases so that transistors T_{15} and T_{16} will convey less current and transistors T_{13} and T_{14} will convey more current. The base current of both transistor T_1 and of transistor T_2 consequently increases. In this way the measuring current I_{s2} and consequently the quiescent current through transistor T_2 is controlled to a well-defined residual value independent of the extent to which transistor T_1 is turned on. When driving transistor T_2 , the quiescent current through transistor T_1 is similarly controlled to the same residual value.

When ignoring the base currents of the transistors T_1 and T_2 it follows from equation 7 that the currents I_1 and I_2 are determined by the following equation:

$$\frac{2I_1 \cdot I_2}{I_1 + I_2} = N \cdot I_0 \quad (11)$$

It is apparent from the equation above that the circuit 40 controls the harmonic mean value of the currents through the transistors T_1 and T_2 to a value which is equal to a reference value. In Fig. 2a the relationship between the currents I_1 and I_2 determined by means of equation 11 is shown graphically. Fig. 2b shows the waveforms of the currents I_1 and I_2 through the transistors T_1 and T_2 as a function of the voltage V_{out} at the output 3 of the amplifier arrangement. For the sake of comparison the waveforms of these currents in the known circuit arrangement are shown in broken lines in this Figure. As is apparent from this Figure, the residual current of the non-driven output transistor is each time controlled to a constant value. It follows from equation 11 that this residual current is given by:

$$I_r = \frac{N I_0}{2} \quad (12)$$

In this embodiment the residual current is thus equal to half the quiescent current in the absence of an input signal. Due to this residual current the non-driven transistor is each time partly turned on and is prevented from being turned off. Consequently, the cross-over distortion is reduced. Since the base-emitter voltage variations of the output transistors are small, the distortion caused thereby is also small. Since the first output transistor T_1 is always turned on, the variation of the output impedance of this transistor and hence of the total amplifier arrangement is small so that the distortion of the output signal caused thereby is also small. Moreover, the dissipation in the non-driven output transistor is substantially constant because the residual current flowing therethrough is accurately fixed and is substantially constant. It is to be noted that the harmonic mean value of the currents through the output transistors and hence the residual current can be controlled to a different value in the case of a different choice of the ratio of the emitter surfaces and/or bias currents. Furthermore, the factor $1/2$ in equation (12) can be modified by giving the transistors in the described translinear loops different emitter surfaces.

Fig. 3 shows a second embodiment of an amplifier arrangement according to the invention in which the same components have the same reference numerals as in Fig. 1. The output transistor T_1 is arranged in a Darlington configuration with a transistor T_{20} , whilst the collector is connected to the collector of transistor T_1 and the emitter is connected to the base of transistor T_1 and to the second power supply terminal 2 by means of a current source I_7 . The base of transistor T_{20} is connected to the first output 6 of the drive means 10. Similarly, transistor T_2 is arranged in a Darlington configuration with a transistor T_{22} , whilst the emitter of transistor T_{22} is connected to the second power supply terminal 2 by means of a current source I_9 . The base of transistor T_{22} is driven by a voltage follower with a transistor T_{23} and a current source I_{10} . The base of transistor T_{23} is connected to the second output 7 of the drive means 10.

The Darlington configurations T_1 , T_{20} and T_2 , T_{22} ensure a very large current gain and consequently very small base currents in the transistors T_{20} and T_{23} .

In the embodiment of Fig. 3 the first output 6 of the drive means is connected to the non-inverting input of an amplifier 50 whose inverting output is connected to the output 3 of the amplifier arrangement. The output of the amplifier 50 is connected to the base of transistor T_{20} . The amplifier 50 ensures a negative feedback around the Darlington configuration T_1 , T_{20} . This results in the distortion of the output voltage due to non-linearities of the output transistor T_1 being eliminated, so that the voltage V_0 at the output 3

accurately follows the voltage at the output 6 of the drive means 10. Since transistor T_1 is always turned on as a result of the quiescent current control according to the invention, it is ensured that this negative feedback continues to function correctly under all circumstances.

Fig. 4 shows a third embodiment of an amplifier arrangement according to the invention in which the same components have the same reference numerals as in Fig. 3. A frequency compensation capacitor C_1 which, as is known, stabilizes the gain if the amplifier arrangement is driven by a conventional input amplifier, is arranged between the input 4 of the amplifier arrangement and the first output 6 of the drive means 10. The input 4 is also connected to the base of a transistor T_{30} whose collector is connected to the power supply terminal 1 and whose emitter is connected to the power supply terminal 2 by means of a current source I_{11} and to the second output 7 of the drive means 10 by means of a capacitor C_2 . The capacitor C_2 ensures that the input voltage V_{in} is directly applied to the base of transistor T_{23} via voltage-follower transistor T_{30} in the case of high frequencies. This enhances the phase margin and hence the stability of the amplifier arrangement. The capacitors C_1 and C_2 also stabilize the control loop which controls the quiescent current because they provide a dominant-pole in this loop.

In this embodiment the amplifier 50 is constituted by a differential amplifier having two transistors T_{40} , T_{41} whose emitters are connected to a common point which is connected to the power supply terminal 2 via a current source I_{12} . The base of transistor T_{40} is connected to the first output 6 of the drive means 10 and the base of the transistor T_{41} is connected to the output 3 of the amplifier arrangement. The collector of transistor T_{40} is directly connected to the power supply terminal 1 and the collector of transistor T_{41} is connected to the positive power supply terminal 1 by means of a current source I_{13} and to an output 15 of the amplifier 30. This output 15 is connected to the base of transistor T_{20} . The first output 6 of the drive means 10 is also connected to the base of a transistor T_{42} whose collector is connected to the first power supply terminal 1 and whose emitter is connected to the second power supply terminal 2 by means of a current source I_{14} and to the output 15 of amplifier 30 by means of a capacitor C_3 . In the region where amplifier 50 exhibits a large phase shift, capacitor C_3 ensures that the signal at the first output 6 is directly applied to the base of transistor T_{20} . A first diode D_1 is arranged between the base and the emitter of transistor T_{40} and a second diode D_2 is arranged parallel to capacitor C_3 . These diodes prevent the amplifier T_{40} , T_{41} from being overdriven in the case of fast, step-wise signals (transients).

Fig. 5 shows a fourth embodiment of an amplifier arrangement according to the invention in which the same components have the same reference numerals as in Fig. 1. The arrangement now comprises MOS field-effect transistors instead of bipolar transistors.

In the negative feedback means 40 two translinear loops can be distinguished again. For the first loop with transistors T_5 - T_{10} the following equation holds:

$$V_{GST7} + V_{GST5} = V_{GST6} + V_{GST8} \quad (13)$$

in which V_{GS} is the gate-source voltage of the relevant transistor. For the second loop with transistors T_3 , T_6 , T_{16} , T_{13} , T_{10} and T_9 the following equation holds:

$$V_{GST8} + V_{GST6} + V_{GST13} = V_{GST9} + V_{GST10} + V_{GST16} \quad (14)$$

Due to the strong negative feedback in the negative feedback loop it can be assumed that the second differential amplifier T_{13} - T_{16} is always balanced, so that it holds that:

$$V_{GST13} = V_{GST14} = V_{GST15} = V_{GST16} \quad (14A)$$

For the second translinear loop it thus holds that:

$$V_{GST9} + V_{GST10} = V_{GST8} + V_{GST6} \quad (15)$$

For identical transistors and using the quadratic relationship between the drain source current I_D and the gate source voltage V_{GS} of a MOS transistor:

$$I_D = 1/2\beta(V_{GS}-V_T)^2 \quad (16)$$

in which

β = a geometry factor and
 V_T = the threshold voltage of the transistor,

equations (13) and (15) can be written as follows

$$2\sqrt{I_0} = \sqrt{I_{S1}} + \sqrt{I_0(1+a)} = \sqrt{I_{S2}} + \sqrt{I_0(1-a)} \quad (17)$$

in which

$I_0(1+a)$ = the current through transistor T_5 and

$I_0(1-a)$ = the current through transistor T_6 .

Equation (17) can be rewritten as

$$I_0(1+a) = (2\sqrt{I_0} - \sqrt{I_{S1}})^2 \quad (18)$$

$$I_0(1-a) = (2\sqrt{I_0} - \sqrt{I_{S2}})^2 \quad (19)$$

By addition of these equations and rewriting, it holds for the relationship between the measuring currents I_{S1} and I_{S2} that:

$$(\sqrt{I_{S1}} - 2\sqrt{I_0})^2 + (\sqrt{I_{S2}} - 2\sqrt{I_0})^2 = 2I_0 \quad (20)$$

This equation describes a locus of a circle a quarter of which is valid. Fig. 6a shows this relationship between the measuring currents I_{S1} and I_{S2} .

With $I_{S1} = I_{S2}$ it follows from equation 20 for the measuring currents flowing in the absence of an input voltage that:

$$I_{S1} = I_{S2} = I_0 \quad (21)$$

For relatively small currents the voltage across resistors R_1 and R_2 is small with respect to the gate-source voltage of the transistors T_3 and T_4 . In the case of a ratio of the length-width ratio of the transistors T_1 and T_3 and of the transistors T_2 and T_4 equal to N it holds for the quiescent currents flowing through transistors T_1 and T_2 that

$$I_1 = I_2 = N I_0 \quad (22)$$

It follows from equation (20) that when driving, for example, transistor T_1 the quiescent current through transistor T_2 is controlled to a residual value which is given by

$$I_r = N I_{S2\text{rest}} = N(2 - \sqrt{2})^2 I_0 \approx 0.35 N I_0 \quad (23)$$

When driving transistor T_1 , the quiescent current through transistor T_2 is controlled in the same manner to the same residual value. The waveforms of the quiescent currents through the output transistors as a function of the output voltage of the amplifier is shown diagrammatically in Fig. 6b. The residual current in this embodiment is thus approximately equal to 0.35 times the quiescent current in the absence of an input signal. In the same way as in the bipolar embodiment, this prevents the non-driven output transistor from being turned off and thereby causing distortion.

Fig. 7 shows a fifth embodiment of an amplifier arrangement according to the invention. Unlike the previous embodiments, the arrangement comprises output transistors of the opposite conductivity type instead of the same type. The arrangement comprises a PNP output transistor T_1 and an NPN output transistor T_2 whose collector-emitter paths are arranged in series between a first power supply terminal 1 and a second power supply terminal 2. The collectors of transistor T_1 and of transistor T_2 are connected to the output 3 of the amplifier arrangement.

The transistors T_1 and T_2 are driven in phase by drive means 10. These means are provided with a differential amplifier having a transistor T_{11} and two transistors T_{12} and T_{13} whose base-emitter junctions are arranged in parallel and whose emitters are connected to a common point which is connected to power supply terminal 2 by means of a current source $I_1 = I$. The base of transistor T_1 is connected to the input 5 to which an input voltage is applied which may originate from an input stage of the conventional type. The common base of the transistors T_{12} and T_{13} is connected to a second input 5 which conveys a reference voltage V_{ref} . The collector of transistor T_{12} is connected to a first output 6 of the drive means to which the base of transistor T_1 is connected and the collector of transistor T_{13} is connected to a second output 7 to which the base of transistor T_2 is connected.

The amplifier arrangement is provided with quiescent current means for controlling the quiescent

currents through the transistors T_1 and T_2 . These means comprise first current measuring means 20 which are constituted by a PNP transistor T_3 whose base-emitter junction in series with a resistor $R_1 = R$ is arranged parallel to the base-emitter junction of transistor T_1 . The current through transistor T_3 and resistor R_1 is a measure of the current through transistor T_1 . To minimize the dissipation, the emitter surface of transistor T_3 is chosen to be much smaller than that of transistor T_1 . The resistor R_1 also limits the maximum value of the current through transistor T_3 to prevent damage when transistor T_1 is fully turned on. The quiescent current means further comprise second current measuring means having a transistor T_4 whose base-emitter junction in series with a resistor $R_2 = R$ is arranged parallel to the base-emitter junction of transistor T_2 . The collector current of transistor T_4 is a measure of the current flowing through transistor T_2 . This current is converted across a resistor $R_3 = R$ into a voltage which is proportional thereto.

The quiescent current means also comprise negative feedback means 40 which are provided with a first differential amplifier having two transistors T_5 and T_6 whose emitters are connected to a common point 8 which is connected to the second power supply terminal 2 by means of a current source $I_2 = I_0$. The base 11 of transistor T_5 is connected to the emitter of transistor T_3 and the base 12 of transistor T_6 is connected to the collector of transistor T_4 . The negative feedback means also comprise a reference circuit which is constituted by the series arrangement of a transistor T_{10} arranged as a diode and a resistor $R_4 = R$ to which a current source $I_3 = I_0$ is connected. The negative feedback means 40 also comprise a second differential amplifier having two transistors T_{15} and T_{16} whose emitters are connected to a common point which is connected to the positive power supply terminal 2 by means of a current source $I_4 = 2I$. The base of transistor T_{15} is connected to the common point 8 of the differential amplifier T_5 , T_6 and the base of the transistor T_{16} is connected to the emitter of transistor T_{10} .

The operation of the arrangement may be explained as follows. Two loops can be distinguished in the means 40. For the loop with resistors R_1 , R_4 and transistors T_5 , T_{10} , T_{15} and T_{16} and for the loop with resistors R_3 , R_4 , T_6 , T_{10} , T_{15} and T_{16} the following equations hold, assuming that the differential amplifier T_{15} , T_{16} will be balanced due to the negative feedback:

$$I_{S1} \cdot R + V_{BET5} = I_0 \cdot R + V_{BET10} \quad (24)$$

$$I_{S2} \cdot R + V_{BET6} = I_0 \cdot R + V_{BET10} \quad (25)$$

in which

I_{S1} = the current through resistor R_1
and

I_{S2} = the current through resistor R_3 .

The relationship between the currents I_1 and I_2 through transistors T_1 and T_2 and the measuring currents I_{S1} and I_{S2} is given by

$$I_1 = N I_{S1} \cdot e^{RI_{S1}/VT} \quad (26)$$

and

$$I_2 = N I_{S2} \cdot e^{RI_{S2}/VT} \quad (27)$$

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With the known relationship between the base-emitter voltage and the collector current of a transistor the following can be written for the equations 24 and 25

$$I_{S1} \cdot R + V_T \ln \frac{I_{T6}}{I_{SP}} = I_0 R + V_T \ln \frac{I}{I_{SP}} \quad (28)$$

$$I_{S2} \cdot R + V_T \ln \frac{I_{T5}}{I_{SP}} = I_0 R + V_T \ln \frac{I}{I_{SP}} \quad (29)$$

With these equations the following relations can be obtained by means of solution for the currents through transistors T_5 and T_6

$$I_{T5} = [I_0 \cdot e^{I_0 R / V_T}] \cdot e^{-I_{S2} \cdot R / V_T} \quad (30)$$

en

$$I_{T6} = [I_0 \cdot e^{I_0 R / V_T}] \cdot e^{-I_{S1} \cdot R / V_T} \quad (31)$$

Furthermore it holds that

$$I_{T5} + I_{T6} = I_0 \quad (32)$$

If equation (32) is combined with equations (30) and (31) the equation indicating the relationship between the measuring currents I_{S1} and I_{S2} is obtained:

$$e^{-I_{S1} \cdot R / V_T} + e^{-I_{S2} \cdot R / V_T} = e^{-I_0 \cdot R / V_T} \quad (32)$$

By filling in the equations (26) and (27) in this equation, the relationship between the output currents I_1 and I_2 is obtained. However, this equation does not give a simple analytic relationship. The waveform of the output currents as a function of the output voltage V_o of the amplifier arrangement is shown in Fig. 8.

In the absence of an input voltage the quiescent currents of transistors T_1 and T_2 will be equally large, so that it also holds that $I_{S1} = I_{S2}$. It follows from equation (32) that:

$$I_{S1} = I_{S2} = I_0 + V_T / R \cdot \ln 2 \quad (33)$$

With the aid of equation (26) or (27) it follows for the value of the quiescent current of transistors T_1 and T_2 that:

$$I_1 = I_2 = 2NI_0 e^{I_0 R / V_T} \left(1 + \frac{V_T}{I_0 R} \cdot \ln 2 \right) \quad (34)$$

For calculating the residual current of an output transistor when the other output transistor is driven, the measuring current of the driven output transistor, for example, I_{S2} is assumed to be very large in equation (32). It follows for the measuring current that

$$I_{S1} = I \quad (35)$$

With equation (26) it follows for the residual current through output transistor T_1 that

$$I_r = NI_0 \cdot e^{I_0 R / V_T} \quad (36)$$

If equation (36) is compared with equation (34), it appears that the residual current is substantially twice as large as the quiescent current in the absence of an input voltage if it holds that $I_0 R > V_T$. The control behaviour of the arrangement is then substantially equal to that of the arrangement of Fig. 1. In the arrangement of Fig. 7 a capacitor C_1 is arranged between the base and the collector of transistor T_1 , a capacitor C_2 is arranged between the base and the collector of transistor T_2 and a capacitor C_3 is arranged between the base and the collector of transistor T_1 . These capacitors fulfill the same functions as the

capacitors C_1 , C_2 and C_3 in the embodiment of Fig. 4. Also in this embodiment the quiescent current of the non-driven output transistor is controlled to a constant residual value, thus preventing the occurrence of harmonic distortion.

It is evident that the arrangement of Fig. 7 may also comprise field-effect transistors instead of bipolar transistors.

The invention is not limited to the embodiments shown. The first and the second current measuring means may be constituted in any other way, provided that they generate a current which is a measure of the current flowing through the first and the second output transistor. The drive means may also be constituted in any other way, provided that they drive the first and the second output transistor in the push-pull mode. The embodiments of the amplifier arrangement according to the invention are either completely built up with bipolar transistors or they are completely built up with unipolar transistors. It is of course also possible to build up the amplifier arrangement with both unipolar and bipolar transistors.

Claims

1. An amplifier arrangement comprising

- a first (T1) and second (T2) output transistor each having a first main terminal, a second main terminal and a control terminal, whose main current paths are arranged in series between two power supply terminals (1, 2) and are further coupled to an output (3) for connecting a load (ZL),
- drive means (10) for driving the first and the second transistor, said drive means having a first input (4) for applying an input signal, a second input (5), a first output (6) which is coupled to the control terminal of the first transistor and a second output (7) which is coupled to the control terminal of the second transistor,
- quiescent current means (20, 30) for causing a quiescent current to flow through the first and the second output transistor, said quiescent current means having first and second current measuring means for generating a first (IS1) and a second (IS2) measuring current which are a measure of the current flowing through the first and the second output transistor, respectively, and having feedback means (40) for controlling the quiescent current flowing through the first and the second output transistor by way of the first and the second measuring current, characterized in that the feedback means comprise
- a first differential amplifier having a third (T5) and a fourth (T6) transistor each having a control terminal, a first main terminal and a second main terminal, the second main terminals being coupled to a common point (8) which is coupled to a first current source (I2), the control terminal of the third transistor being coupled to a first point (11) for conveying a voltage which is proportional to the first measuring current and the control terminal of the fourth transistor being coupled to a second point (12) for conveying a voltage which is proportional to the second measuring current,
- a reference circuit comprising a second current source (I3) and a fifth transistor (T10) having a first main terminal, a second main terminal and a control terminal which is coupled to the first main terminal, and
- a second differential amplifier having a sixth (T13, T14) and a seventh (T15, T16) transistor each having at least one first main terminal, at least one second main terminal and a control terminal, the control terminal of the sixth transistor being coupled to the second main terminal of the fifth transistor, the control terminal of the seventh transistor being coupled to the common point (8) of the first differential amplifier, and two of the first main terminals of the sixth and the seventh transistor being coupled to the first and the second output of the drive means.

2. An amplifier arrangement as claimed in Claim 1, characterized in that

- the first (T1) and the second (T2) output transistor are of the same conductivity type,
- the sixth (T13, T14) and the seventh (T15, T16) transistor each have two first main terminals, and in that
- the one first main terminal of the sixth transistor is coupled to the first output (6) of the drive means and the other first main terminal of the sixth transistor is coupled to the second output (7) of the drive means.

3. An amplifier arrangement as claimed in Claim 1 or 2, characterized in that the first current measuring means include an eighth transistor (T3) having a first main terminal, a second main terminal and a control terminal, the control terminal and the second main terminal being coupled to the control

capacitors C_1 , C_2 and C_3 in the embodiment of Fig. 4. Also in this embodiment the quiescent current of the non-driven output transistor is controlled to a constant residual value, thus preventing the occurrence of harmonic distortion.

It is evident that the arrangement of Fig. 7 may also comprise field-effect transistors instead of bipolar transistors.

The invention is not limited to the embodiments shown. The first and the second current measuring means may be constituted in any other way, provided that they generate a current which is a measure of the current flowing through the first and the second output transistor. The drive means may also be constituted in any other way, provided that they drive the first and the second output transistor in the push-pull mode. The embodiments of the amplifier arrangement according to the invention are either completely built up with bipolar transistors or they are completely built up with unipolar transistors. It is of course also possible to build up the amplifier arrangement with both unipolar and bipolar transistors.

Claims

1. An amplifier arrangement comprising

- a first (T1) and second (T2) output transistor each having a first main terminal, a second main terminal and a control terminal, whose main current paths are arranged in series between two power supply terminals (1, 2) and are further coupled to an output (3) for connecting a load (ZL),
- drive means (10) for driving the first and the second transistor, said drive means having a first input (4) for applying an input signal, a second input (5), a first output (6) which is coupled to the control terminal of the first transistor and a second output (7) which is coupled to the control terminal of the second transistor,
- quiescent current means (20, 30) for causing a quiescent current to flow through the first and the second output transistor, said quiescent current means having first and second current measuring means for generating a first (IS1) and a second (IS2) measuring current which are a measure of the current flowing through the first and the second output transistor, respectively, and having feedback means (40) for controlling the quiescent current flowing through the first and the second output transistor by way of the first and the second measuring current, characterized in that the feedback means comprise
- a first differential amplifier having a third (T5) and a fourth (T6) transistor each having a control terminal, a first main terminal, and a second main terminal, the second main terminals being coupled to a common point (8) which is coupled to a first current source (I2), the control terminal of the third transistor being coupled to a first point (11) for conveying a voltage which is proportional to the first measuring current and the control terminal of the fourth transistor being coupled to a second point (12) for conveying a voltage which is proportional to the second measuring current,
- a reference circuit comprising a second current source (I3) and a fifth transistor (T10) having a first main terminal, a second main terminal and a control terminal which is coupled to the first main terminal, and
- a second differential amplifier having a sixth (T13, T14) and a seventh (T15, T16) transistor each having at least one first main terminal, at least one second main terminal and a control terminal, the control terminal of the sixth transistor being coupled to the second main terminal of the fifth transistor, the control terminal of the seventh transistor being coupled to the common point (8) of the first differential amplifier, and two of the first main terminals of the sixth and the seventh transistor being coupled to the first and the second output of the drive means.

2. An amplifier arrangement as claimed in Claim 1, characterized in that

- the first (T1) and the second (T2) output transistor are of the same conductivity type,
- the sixth (T13, T14) and the seventh (T15, T16) transistor each have two first main terminals, and in that
- the one first main terminal of the sixth transistor is coupled to the first output (6) of the drive means and the other first main terminal of the sixth transistor is coupled to the second output (7) of the drive means.

3. An amplifier arrangement as claimed in Claim 1 or 2, characterized in that the first current measuring means include an eighth transistor (T3) having a first main terminal, a second main terminal and a control terminal, the control terminal and the second main terminal being coupled to the control



terminal and the second main terminal, respectively, of the first output transistor and in that the second current measuring means include a ninth transistor (T4) having a first main terminal, a second main terminal and a control terminal, the control terminal and the second main terminal being coupled to the control terminal and the second main terminal, respectively, of the second output transistor.

4. An amplifier arrangement as claimed in Claim 3, characterized in that the second main terminal of the eighth transistor (T3) is coupled to the second main terminal of the first output transistor by means of a first resistor (R1) and in that the second main terminal of the ninth (T4) transistor is coupled to the second main terminal of the second output transistor by means of a second resistor (R2).
5. An amplifier arrangement as claimed in Claim 3 or 4, characterized in that
 - the first main terminal of the eighth transistor is coupled to a first power supply terminal by means of a tenth transistor (T7) having a first main terminal, a second main terminal and a control terminal, the first main terminal of the tenth transistor being coupled to its control terminal and the second main terminal constituting the first point (11) for conveying a voltage which is proportional to the first measuring current,
 - the first main terminal of the ninth transistor is coupled to the first power supply terminal by means of an eleventh transistor (T8) having a first main terminal, a second main terminal and a control terminal, the first main terminal of the eleventh transistor being coupled to its control terminal and the second main terminal constituting the second point (12) for conveying a voltage which is proportional to the second measuring current, and in that
 - the first main terminal of the fifth transistor (T10) is coupled to the first power supply terminal by means of a twelfth (T9) transistor having a first main terminal and a second main terminal and a control terminal, the first main terminal being coupled to its control terminal.
6. An amplifier arrangement as claimed in Claim 1, 2, 3, 4 or 5, characterized in that the drive means include a third differential amplifier having a thirteenth (T11) and a fourteenth transistor (T12) each having a first main terminal, a second main terminal and a control terminal, the control terminal and the first main terminal of the thirteenth transistor being coupled to the first input (4) and the first output (6) respectively, of the drive means and the control terminal and the first main terminal of the fourteenth transistor being coupled to the second input (5) and the second output (7), respectively, of the drive means.
7. An amplifier arrangement as claimed in Claim 6, characterized in that a first capacitor (C1) is arranged between the first input (4) and the first output (6) of the drive means.
8. An amplifier arrangement as claimed in Claim 6 or 7, characterized in that the first input (6) of the drive means is coupled to an input of a fifteenth transistor (T30) arranged as a voltage follower, an output of which is coupled to the second output (7) of the drive means by means of a second capacitor (C2).
9. An amplifier arrangement as claimed in any one of Claims 2 to 8, characterized in that the first output of the drive means is coupled to a non-inverting input of an amplifier (50), an inverting input of which is coupled to the output of the amplifier arrangement and an output of which is coupled to the control terminal of the first output transistor.
10. An amplifier arrangement as claimed in Claim 9, characterized in that the amplifier is constituted by a fourth differential amplifier having a sixteenth (T40) and a seventeenth (T41) transistor each having a control terminal and a first and a second main terminal, the control terminal of the sixteenth transistor being coupled to the non-inverting input and the control terminal of the seventeenth transistor being coupled to the inverting input, the first main terminal of the seventeenth transistor being coupled to the output of the amplifier and to a current source (I13).
11. An amplifier arrangement as claimed in Claim 9 or 10, characterized in that the first output of the drive means (6) is coupled to an input of a voltage-follower circuit (T42), an output of which is coupled to the control terminal of the first output transistor by means of a third capacitor (C3).
12. An amplifier arrangement as claimed in Claim 11, characterized in that a first diode (D2) is arranged in parallel with the third capacitor (C3) and in that a second diode (D1) is arranged between the second



main terminal and the control terminal of the sixteenth transistor (T40).

13. An amplifier arrangement as claimed in any one of the preceding Claims 2 to 12, characterized in that the transistors are bipolar transistors.

14. An amplifier arrangement as claimed in any one of the preceding Claims 2 to 12, characterized in that the transistors are field-effect transistors.

15. An amplifier arrangement as claimed in Claim 1, characterized in that

- the first (T1) and the second (T2) output transistor are of the opposite conductivity type,
- the sixth and the seventh transistor each have a first main terminal and in that
- the first main terminal of the sixth transistor is coupled to the first output (6) of the drive means and the first main terminal of the seventh transistor is coupled to the second output (7) of the drive means.

16. An amplifier arrangement as claimed in Claim 15, characterized in that

- the first current measuring means include an eighth transistor (T3) having a first main terminal, a second main terminal and a control terminal, the control terminal being coupled to the control terminal of the first output transistor and the second main terminal being coupled to the second main terminal of the first output transistor by means of a first resistor (R1), said second main terminal of the eighth transistor constituting the first point for conveying a voltage which is proportional to the first measuring current,
- the second current measuring means include a ninth transistor (T4) having a first main terminal, a second main terminal and a control terminal, the control terminal being coupled to the control terminal of the second output transistor and the second main terminal being coupled to the second main terminal of the second output transistor by means of a second resistor (R2),
- the first main terminal of the ninth transistor is coupled to a first power supply terminal by means of a third resistor (R3), said first main terminal of the ninth transistor constituting the second point for conveying a voltage which is proportional to the second measuring current, and in that
- the first main terminal of the fifth transistor is coupled to the first power supply terminal by means of a fourth resistor.

17. An amplifier arrangement as claimed in Claim 1, 15 or 16, characterized in that

- the drive means include a third differential amplifier with a tenth transistor (T11) having a first main terminal, a second main terminal and a control terminal and an eleventh transistor (T12, T13) having two first main terminals, two second main terminals and a control terminal, the control terminal of the tenth transistor being coupled to the first input of the drive means and the control terminal and the two first main terminals of the eleventh transistor being coupled to the second input and the first and the second output, respectively, of the drive means.

18. An amplifier arrangement as claimed in Claim 17, characterized in that a first capacitor (C1) is arranged between the first input and the first main terminal of the tenth transistor.

19. An amplifier arrangement as claimed in Claim 16, 17 or 18, characterized in that

- a second capacitor (C3) is arranged between the control terminal of the first output transistor and the output, and in that
- a third capacitor (C2) is arranged between the control terminal of the second output transistor and the output.

20. An amplifier arrangement as claimed in anyone of the preceding Claims 15 to 19, characterized in that the transistors are bipolar transistors.

Patentansprüche

1. Verstärkeranordnung mit

- einem ersten (T1) und einem zweiten (T2) Ausgangstransistor mit je einem ersten Hauptanschluß, einem zweiten Hauptanschluß und einem Steuerungsanschluß, deren Leitungspfade zwischen zwei Stromversorgungsanschlüssen (1,2) in Reihe geschaltet und außerdem mit einem Ausgang



- (3) zum Anschluß einer Last (ZL) gekoppelt sind,
- Treibermitteln (10) zum Ansteuern des ersten und des zweiten Transistors, wobei die Treibermittel einen ersten Eingang (4) zum Zuführen eines Eingangssignals, einen zweiten Eingang (5), einen ersten, mit dem Steuerungsanschluß des ersten Transistors gekoppelten Ausgang (6) und einen zweiten, mit dem Steuerungsanschluß des zweiten Transistors gekoppelten Ausgang (7) haben,
 - Ruhestrommitteln (20, 30) zum Bewirken eines durch den ersten und den zweiten Ausgangstransistor fließenden Ruhestroms, wobei diese Ruhestrommittel erste und zweite Strommeßmittel zum Erzeugung eines ersten (IS1) und eines zweiten (IS2) Meßstroms haben, wobei die Meßströme ein Maß für den durch den ersten bzw. den zweiten Ausgangstransistor fließenden Strom sind, sowie Rückkopplungsmittel (40) zur Steuerung des durch den ersten und den zweiten Ausgangstransistor fließenden Ruhestroms anhand des ersten und des zweiten Meßstroms, dadurch gekennzeichnet, daß die Rückkopplungsmittel folgendes umfassen:
 - einen ersten Differentialverstärker mit einem dritten (T5) und einem vierten (T6) Transistor, die je einen Steuerungsanschluß, einen ersten Hauptanschluß und einen zweiten Hauptanschluß haben, wobei die zweiten Hauptanschlüsse mit einem gemeinsamen, mit einer ersten Stromquelle (I2) gekoppelten Punkt (8) verbunden sind, der Steuerungsanschluß des dritten Transistors mit einem ersten Punkt (11) zum Führen einer zu dem ersten Meßstrom proportionalen Spannung und der Steuerungsanschluß des vierten Transistors mit einem zweiten Punkt (12) zum Führen einer zu dem zweiten Meßstrom proportionalen Spannung gekoppelt ist,
 - eine Bezugsschaltung mit einer zweiten Stromquelle (I3) und einem fünften Transistor (T10), der einen ersten Hauptanschluß, einen zweiten Hauptanschluß und einen mit dem ersten Hauptanschluß gekoppelten Steuerungsanschluß hat, und
 - einen zweiten Differentialverstärker mit einem sechsten (T13, T14) und einem siebenten (T15, T16) Transistor mit je mindestens einem ersten Hauptanschluß, mindestens einem zweiten Hauptanschluß und einem Steuerungsanschluß, wobei der Steuerungsanschluß des sechsten Transistors mit dem zweiten Hauptanschluß des fünften Transistors gekoppelt ist, der Steuerungsanschluß des siebenten Transistors mit dem gemeinsamen Punkt (8) des ersten Differentialverstärkers gekoppelt ist und zwei der ersten Hauptanschlüsse des sechsten und des siebenten Transistors mit dem ersten und dem zweiten Ausgang der Treibermittel gekoppelt sind.
2. Verstärkeranordnung nach Anspruch 1, dadurch gekennzeichnet, daß
- der erste (T1) und der zweite (T2) Ausgangstransistor vom gleichen Leitfähigkeitstyp sind,
 - der sechste (T13, T14) und der siebente (T15, T16) Transistor je zwei erste Hauptanschlüsse haben, und daß
 - der eine erste Hauptanschluß des sechsten Transistors mit dem ersten Ausgang (6) der Treibermittel und der andere erste Hauptanschluß des sechsten Transistors mit dem zweiten Ausgang (7) der Treibermittel gekoppelt ist.
3. Verstärkeranordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die ersten Strommeßmittel einen achten Transistor (T3) mit einem ersten Hauptanschluß, einem zweiten Hauptanschluß und einem Steuerungsanschluß enthalten, wobei der Steuerungsanschluß und der zweite Hauptanschluß mit dem Steuerungsanschluß bzw. dem zweiten Hauptanschluß des ersten Ausgangstransistors gekoppelt sind, und daß die zweiten Strommeßmittel einen neunten Transistor (T4) mit einem ersten Hauptanschluß, einem zweiten Hauptanschluß und einem Steuerungsanschluß enthalten, wobei der Steuerungsanschluß und der zweite Hauptanschluß mit dem Steuerungsanschluß bzw. dem zweiten Hauptanschluß des zweiten Ausgangstransistors gekoppelt sind.
4. Verstärkeranordnung nach Anspruch 3, dadurch gekennzeichnet, daß der zweite Hauptanschluß des achten Transistors (T3) mit Hilfe eines ersten Widerstandes (R1) mit dem zweiten Hauptanschluß des ersten Ausgangstransistors gekoppelt ist, und daß der zweite Hauptanschluß des neunten Transistors (T4) mit Hilfe eines zweiten Widerstandes (R2) mit dem zweiten Hauptanschluß des zweiten Ausgangstransistors gekoppelt ist.
5. Verstärkeranordnung nach Anspruch 3 oder 4, dadurch gekennzeichnet, daß
- der erste Hauptanschluß des achten Transistors mit Hilfe eines zehnten Transistors (T7), der einen ersten Hauptanschluß, einen zweiten Hauptanschluß und einen Steuerungsanschluß hat, mit einem ersten Stromversorgungsanschluß gekoppelt ist, wobei der erste Hauptanschluß des



- zehnten Transistors mit dessen Steuerungsanschluß gekoppelt ist, und der zweite Hauptanschluß den ersten Punkt (11) zum Führen einer zu dem ersten Meßstrom proportionalen Spannung bildet,
- 5 - der erste Hauptanschluß des neunten Transistors mit Hilfe eines elften Transistors (T8), der einen ersten Hauptanschluß, einen zweiten Hauptanschluß und einen Steuerungsanschluß hat, mit dem ersten Stromversorgungsanschluß gekoppelt ist, wobei der erste Hauptanschluß des elften Transistors mit dessen Steuerungsanschluß gekoppelt ist, und der zweite Hauptanschluß den zweiten Punkt (12) zum Führen einer zu dem zweiten Meßstrom proportionalen Spannung bildet, und daß
- 10 - der erste Hauptanschluß des fünften Transistors (T10) mit Hilfe eines zwölften Transistors (T9), der einen ersten Hauptanschluß, einen zweiten Hauptanschluß und einen Steuerungsanschluß hat, mit dem ersten Stromversorgungsanschluß gekoppelt ist, wobei der erste Hauptanschluß des zwölften Transistors mit dessen Steuerungsanschluß gekoppelt ist.
- 15 6. Verstärkeranordnung nach Anspruch 1, 2, 3, 4 oder 5, dadurch gekennzeichnet, daß die Treibermittel einen dritten Differentialverstärker mit einem dreizehnten (T11) und einem vierzehnten (T12) Transistor enthalten, die je einen ersten Hauptanschluß, einen zweiten Hauptanschluß und einen Steuerungsanschluß haben, wobei der Steuerungsanschluß und der erste Hauptanschluß des dreizehnten Transistors mit dem ersten Eingang (4) bzw. dem ersten Ausgang (6) der Treibermittel und der Steuerungsanschluß und der erste Hauptanschluß des vierzehnten Transistors mit dem zweiten Eingang (5) bzw. dem zweiten Ausgang (7) der Treibermittel gekoppelt sind.
- 20 7. Verstärkeranordnung nach Anspruch 6, dadurch gekennzeichnet, daß ein erster Kondensator (C1) zwischen den ersten Eingang (4) und den ersten Ausgang (6) der Treibermittel geschaltet ist.
- 25 8. Verstärkeranordnung nach Anspruch 6 oder 7, dadurch gekennzeichnet, daß der erste Eingang (6) der Treibermittel mit einem Eingang eines fünfzehnten, als Spannungsfolger geschalteten Transistors (T30) gekoppelt ist, wobei ein Ausgang des Transistors mit Hilfe eines zweiten Kondensators (C2) mit dem zweiten Ausgang (7) der Treibermittel gekoppelt ist.
- 30 9. Verstärkeranordnung nach einem der Ansprüche 2 bis 8, dadurch gekennzeichnet, daß der erste Ausgang der Treibermittel mit einem nicht-invertierenden Eingang eines Verstärkers (50) gekoppelt ist, von dem ein invertierender Eingang mit dem Ausgang der Verstärkeranordnung und von dem ein Ausgang mit dem Steuerungsanschluß des ersten Ausgangstransistors gekoppelt ist.
- 35 10. Verstärkeranordnung nach Anspruch 9, dadurch gekennzeichnet, daß der Verstärker von einem vierten Differentialverstärker mit einem sechzehnten (T40) und einem siebzehnten (T41) Transistor gebildet wird, die je einen Steuerungsanschluß, einen ersten Hauptanschluß und einen zweiten Hauptanschluß haben, wobei der Steuerungsanschluß des sechzehnten Transistors mit dem nicht-invertierenden Eingang und der Steuerungsanschluß des siebzehnten Transistors mit dem invertierenden Eingang gekoppelt ist, und wobei der erste Hauptanschluß des siebzehnten Transistors mit dem Ausgang des Verstärkers und mit einer Stromquelle (I13) gekoppelt ist.
- 40 11. Verstärkeranordnung nach Anspruch 9 oder 10, dadurch gekennzeichnet, daß der erste Ausgang der Treibermittel (6) mit einem Eingang einer Spannungsfolgerschaltung (T42) gekoppelt ist, von der ein Ausgang mit Hilfe eines dritten Kondensators (C3) mit dem Steuerungsanschluß des ersten Ausgangstransistors gekoppelt ist.
- 45 12. Verstärkeranordnung nach Anspruch 11, dadurch gekennzeichnet, daß eine erste Diode (D2) parallel zu dem dritten Kondensator (C3) und eine zweite Diode (D1) zwischen den zweiten Hauptanschluß und den Steuerungsanschluß des sechzehnten Transistors (T40) geschaltet ist.
- 50 13. Verstärkeranordnung nach einem der Ansprüche 2 bis 12, dadurch gekennzeichnet, daß die Transistoren Bipolartransistoren sind.
- 55 14. Verstärkeranordnung nach einem der Ansprüche 2 bis 12, dadurch gekennzeichnet, daß die Transistoren Feldeffekttransistoren sind.
15. Verstärkeranordnung nach Anspruch 1, dadurch gekennzeichnet, daß



- der erste (T1) und der zweite (T2) Ausgangstristor vom entgegengesetzten Leitfähigkeitstyp sind,
- der sechste und der siebente Transistor je einen ersten Hauptanschluß haben und daß
- der erste Hauptanschluß des sechsten Transistors mit dem ersten Ausgang (6) der Treibermittel und der erste Hauptanschluß des siebenten Transistors mit dem zweiten Ausgang (7) der Treibermittel gekoppelt ist.

16. Verstärkernordnung nach Anspruch 15, dadurch gekennzeichnet, daß

- die ersten Strommeßmittel einen achten Transistor (T3) mit einem ersten Hauptanschluß, einem zweiten Hauptanschluß und einem Steuerungsanschluß enthalten, wobei der Steuerungsanschluß mit dem Steuerungsanschluß des ersten Ausgangstristors und der zweite Hauptanschluß mit Hilfe eines ersten Widerstandes (R1) mit dem zweiten Hauptanschluß des ersten Ausgangstristors gekoppelt sind, und wobei dieser zweite Hauptanschluß des achten Transistors den ersten Punkt zum Führen einer zu dem ersten Meßstrom proportionalen Spannung bildet,
- die zweiten Strommeßmittel einen neunten Transistor (T4) mit einem ersten Hauptanschluß, einem zweiten Hauptanschluß und einem Steuerungsanschluß enthalten, wobei der Steuerungsanschluß mit dem Steuerungsanschluß des zweiten Ausgangstristors und der zweite Hauptanschluß mit Hilfe eines zweiten Widerstandes (R2) mit dem zweiten Hauptanschluß des zweiten Ausgangstristors gekoppelt sind,
- der erste Hauptanschluß des neunten Transistors mit Hilfe eines dritten Widerstandes (R3) mit einem ersten Stromversorgungsanschluß gekoppelt ist, wobei dieser erste Hauptanschluß des neunten Transistors den zweiten Punkt zum Führen einer zu dem zweiten Meßstrom proportionalen Spannung bildet, und daß
- der erste Hauptanschluß des fünften Transistors mit Hilfe eines vierten Widerstandes mit dem ersten Stromversorgungsanschluß gekoppelt ist.

17. Verstärkeranordnung nach Anspruch 1, 15 oder 16, dadurch gekennzeichnet, daß

- die Treibermittel einen dritten Differentialverstärker enthalten, mit einem zehnten Transistor (T11), der einen ersten Hauptanschluß, einen zweiten Hauptanschluß und einen Steuerungsanschluß hat, und einem elften Transistor (T12, T13), der zwei erste Hauptanschlüsse, zwei zweite Hauptanschlüsse und einen Steuerungsanschluß hat, wobei der Steuerungsanschluß des zehnten Transistors mit dem ersten Eingang der Treibermittel verbunden ist, und der Steuerungsanschluß sowie die beiden ersten Hauptanschlüsse des elften Transistors mit dem zweiten Eingang und dem ersten bzw. dem zweiten Ausgang der Treibermittel verbunden sind.

18. Verstärkeranordnung nach Anspruch 17, dadurch gekennzeichnet, daß ein erster Kondensator (C1) zwischen den ersten Eingang und den ersten Hauptanschluß des zehnten Transistors geschaltet ist.

19. Verstärkeranordnung nach Anspruch 16, 17 oder 18, dadurch gekennzeichnet, daß

- ein zweiter Kondensator (C3) zwischen den Steuerungsanschluß des ersten Ausgangstristors und den Ausgang geschaltet ist, und daß
- ein dritter Kondensator (C2) zwischen den Steuerungsanschluß des zweiten Ausgangstristors und den Ausgang geschaltet ist.

20. Verstärkernordnung nach einem der Ansprüche 15 bis 19, dadurch gekennzeichnet, daß die Transistoren Bipolartransistoren sind.

Revendications

1. Circuit amplificateur comportant

- des premier (T1) et deuxième (T2) transistors de sortie présentant chacun une première borne principale, une deuxième borne principale et une borne de réglage, transistors dont les principaux trajets de courant sont montés en série entre deux bornes d'alimentation (1, 2) et couplés, en outre, à une sortie (3) pour relier une charge (ZL),
- des moyens d'excitation (10) pour exciter les premier et deuxième transistors, lesdits moyens d'excitation présentant une première entrée (4) pour appliquer un signal d'entrée, une deuxième entrée (5), une première sortie (6) couplée à la borne de réglage du premier transistor et une deuxième sortie (7) couplée à la borne de réglage du deuxième transistor,



- des moyens de courant de repos (20, 30) pour faire circuler un courant de repos à travers les premier et deuxième transistors de sortie, lesdits moyens de courant de repos présentant de premier et deuxième moyens de mesure de courant pour engendrer de premier (IS1) et deuxième (IS2) courants de mesure qui constituent une mesure du courant circulant respectivement à travers les premier et deuxième transistors de sortie, et présentant des moyens de rétrocouplage (40) pour régler le courant de repos circulant à travers les premier et deuxième transistors de sortie à l'aide des premier et deuxième courants de mesure, caractérisé en ce que les moyens de rétrocouplage comportent
 - un premier amplificateur différentiel ayant de troisième (T5) et quatrième (T6) transistors présentant chacun une borne de réglage, une première borne principale et une deuxième borne principale, les deuxièmes bornes principales étant couplées à un point commun (8) couplé à une première source de courant (I2), la borne de réglage du troisième transistor étant couplée à un premier point (11) destiné à porter une tension proportionnelle au premier courant de mesure et la borne de réglage du quatrième transistor étant couplée à un deuxième point (12) destiné à porter une tension proportionnelle au deuxième courant de mesure,
 - un circuit de référence comportant une deuxième source de courant (I3) et un cinquième transistor (T10) présentant une première borne principale, une deuxième borne principale et une borne de réglage couplée à la première borne principale, et
 - un deuxième amplificateur différentiel présentant des sixième (T13, T14) et septième (T15, T16) transistors ayant chacun au moins une première borne principale, au moins une deuxième borne principale et une borne de réglage, la borne de réglage du sixième transistor étant couplée à la deuxième borne principale du cinquième transistor, la borne de réglage du septième transistor étant couplée au point commun (8) du premier amplificateur différentiel, et deux des premières bornes principales des sixième et septième transistors étant couplées aux première et deuxième sorties des moyens d'excitation.

2. Circuit amplificateur selon la revendication 1, caractérisé en ce que

- les premier (T1) et deuxième (T2) transistors de sortie sont du même type de conductivité,
- les sixième (T13, T14) et septième (T15, T16) transistors présentent chacun deux premières bornes principales, et
- la première borne principale du sixième transistor est couplée à la première sortie (6) des moyens d'excitation et l'autre première borne principale du sixième transistor est couplée à la deuxième sortie (7) des moyens d'excitation.

3. Circuit amplificateur selon la revendication 1 ou 2, caractérisé en ce que les premiers moyens de mesure de courant comprennent un huitième transistor (T3) présentant une première borne principale, une deuxième borne principale et une borne de réglage, la borne de réglage et la deuxième borne principale étant couplées respectivement à la borne de réglage et à la deuxième borne principale du premier transistor de sortie et en ce que les deuxièmes moyens de mesure de courant comprennent un neuvième transistor (T4) présentant une première borne principale, une deuxième borne principale et une borne de réglage, la borne de réglage et la deuxième borne principale étant couplées respectivement à la borne de réglage et à la deuxième borne principale du deuxième transistor de sortie.

4. Circuit amplificateur selon la revendication 3, caractérisé en ce que la deuxième borne principale du huitième transistor (T3) est couplée à la deuxième borne principale du premier transistor de sortie à l'aide d'une première résistance (R1) et en ce que la deuxième borne principale du neuvième transistor (T4) est couplée à la deuxième borne principale du deuxième transistor de sortie à l'aide d'une deuxième résistance (R2).

5. Circuit amplificateur selon la revendication 3 ou 4, caractérisé en ce que

- la première borne principale du huitième transistor est couplée à une première borne d'alimentation à l'aide d'un dixième transistor (T7) présentant une première borne principale, une deuxième borne principale et une borne de réglage, la première borne principale du dixième transistor étant couplée à sa borne de réglage et la deuxième borne principale constituant le premier point (11) destiné à porter une tension proportionnelle au premier courant de mesure,
- la première borne principale du neuvième transistor est couplée à la première borne d'alimentation à l'aide d'un onzième transistor (T8) présentant une première borne principale, une deuxième borne principale et une borne de réglage, la première borne principale du onzième transistor



étant couplée à sa borne de réglage et la deuxième borne principale constituant le deuxième point (12) destiné à porter une tension proportionnelle au deuxième courant de mesure, et

- la première borne principale du cinquième transistor (T10) est couplée à la première borne d'alimentation à l'aide d'un douzième transistor (T9) présentant une première borne principale et une deuxième borne principale et une borne de réglage, la première borne principale étant couplée à sa borne de réglage.

6. Circuit amplificateur selon la revendication 1, 2, 3, 4 ou 5, caractérisé en ce que les moyens d'excitation comprennent un troisième amplificateur différentiel présentant des treizième (T11) et quatorzième (T12) transistors ayant chacun une première borne principale, une deuxième borne principale et une borne de réglage, la borne de réglage et la première borne principale du treizième transistor étant couplées respectivement à la première entrée (4) et la première sortie (6) des moyens d'excitation et la borne de réglage et la première borne principale du quatorzième transistor étant couplées respectivement à la deuxième entrée (5) et à la deuxième sortie (7) des moyens d'excitation.

7. Circuit amplificateur selon la revendication (6), caractérisé en ce qu'un premier condensateur (C1) est monté entre la première entrée (4) et la première sortie (6) des moyens d'excitation.

8. Circuit amplificateur selon la revendication 6 ou 7, caractérisé en ce que la première entrée (6) des moyens d'excitation est couplée à une entrée d'un quinzième transistor (T30) monté comme suiveur de tension dont une sortie est couplée à la deuxième sortie (7) des moyens d'excitation à l'aide d'un deuxième condensateur (C2).

9. Circuit amplificateur selon l'une quelconque des revendications 2 à 8, caractérisé en ce que la première sortie des moyens d'excitation est couplée à une entrée non inverseuse d'un amplificateur (50) dont une entrée inverseuse est couplée à la sortie du circuit amplificateur et dont une sortie est couplée à la borne de réglage du premier transistor de sortie.

10. Circuit amplificateur selon la revendication 9, caractérisé en ce que l'amplificateur est constitué d'un quatrième amplificateur différentiel présentant des seizième (T40) et dix-septième (T41) transistors ayant chacun une borne de réglage et de première et deuxième bornes principales, la borne de réglage du seizième transistor étant couplée à l'entrée non inverseuse et la borne de réglage du dix-septième transistor étant couplée à l'entrée inverseuse, la première borne principale du dix-septième transistor étant couplée à la sortie de l'amplificateur et à une source de courant (I13).

11. Circuit amplificateur selon la revendication 9 ou 10, caractérisé en ce que la première sortie des moyens d'excitation (6) est couplée à une entrée d'un circuit suiveur de tension (T42) dont une sortie est couplée à la borne de réglage du premier transistor de sortie à l'aide d'un troisième condensateur (C3).

12. Circuit amplificateur selon la revendication 11, caractérisé en ce qu'une première diode (D2) est montée en parallèle avec le troisième condensateur (C3) et en ce qu'une deuxième diode (D1) est montée entre la deuxième borne principale et la borne de réglage du seizième transistor (T40).

13. Circuit amplificateur selon l'une quelconque des revendications précédentes 2 à 12, caractérisé en ce que les transistors sont des transistors bipolaires.

14. Circuit amplificateur selon l'une quelconque des revendications précédentes 2 à 12, caractérisé en ce que les transistors sont des transistors à effet de champ.

15. Circuit amplificateur selon la revendication 1, caractérisé en ce que

- les premier (T1) et deuxième (T2) transistors de sortie sont du type de conductivité opposé
- les sixième et septième transistors présentent chacun une première borne principale et
- la première borne principale du sixième transistor est couplée à la première sortie (6) des moyens d'excitation et en ce que la première borne principale du septième transistor est couplée à la deuxième sortie (7) des moyens d'excitation.

16. Circuit amplificateur selon la revendication 15, caractérisé en ce que



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- les premiers moyens de mesure de courant comprennent un huitième transistor (T3) présentant une première borne principale, une deuxième borne principale et une borne de réglage, la borne de réglage étant couplée à la borne de réglage du premier transistor de sortie et la deuxième borne principale étant couplée à la deuxième borne principale du premier transistor de sortie à l'aide d'une première résistance (R1), ladite deuxième borne principale du huitième transistor constituant le premier point pour porter une tension proportionnelle au premier courant de mesure,
 - 10 - les deuxièmes moyens de mesure de courant comprennent un neuvième transistor (T4) présentant une première borne principale, une deuxième borne principale et une borne de réglage, la borne de réglage étant couplée à la borne de réglage du deuxième transistor de sortie et la deuxième borne principale étant couplée à la deuxième borne principale du deuxième transistor de sortie à l'aide d'une deuxième résistance (R2),
 - 15 - la première borne principale du neuvième transistor est couplée à une première borne d'alimentation à l'aide d'une troisième résistance (R3), ladite première borne principale du neuvième transistor formant le deuxième point pour porter une tension proportionnelle au deuxième courant de mesure, et
 - la première borne principale du cinquième transistor est couplée à la première borne d'alimentation à l'aide d'une quatrième résistance.
- 20 17. Circuit amplificateur selon les revendications 1, 15, 16 caractérisé en ce que
- les moyens d'excitation comprennent un troisième amplificateur différentiel muni d'un dixième transistor (T11) présentant une première borne principale, une deuxième borne principale et une borne de réglage et un onzième transistor (T12, T13) présentant deux premières bornes principales, deux deuxième bornes principales et une borne de réglage, la borne de réglage du dixième transistor étant couplée à la première entrée des moyens d'excitation et la borne de réglage et les deux premières bornes principales du onzième transistor étant couplées respectivement à la deuxième entrée et aux première et deuxième sorties des moyens d'excitation.
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18. Circuit amplificateur selon la revendication 17, caractérisé en ce qu'un premier condensateur (C1) est monté entre la première entrée et la première borne principale du dixième transistor.
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19. Circuit amplificateur selon les revendications 16, 17 ou 18, caractérisé en ce que
- un deuxième condensateur (C3) est monté entre la borne de réglage du premier transistor de sortie et la sortie, et
 - 35 - un troisième condensateur (C2) est monté entre la borne de réglage du deuxième transistor de sortie et la sortie.
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20. Circuit amplificateur selon l'une quelconque des revendications précédentes 15 à 19, caractérisé en ce que les transistors sont des transistors bipolaires.
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