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☒ Drawing(s) : paged ... to paged ...
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**Method and device for monitoring an
alternating signal**

5 The present invention relates to a method for monitoring an alternating signal in accordance with the precharacterizing clause of Claim 1 and a device in accordance with the precharacterizing clause of the first substantive claim.

10 The use of stages which output an alternating signal which is used for controlling a connected stage is generally known. Control stages of this type may contain, for example, a microprocessor which outputs an alternating signal in the form of a digital signal and thus controls a connected stage. Oscillators are also known which use a sinusoidal, rectangular or other alternating
15 signal for processing further signals by means of corresponding stages.

Various possibilities are conceivable for a signal which is of the type output by a control stage of the said type, is alternating, also called changing
20 below, to change its course. Thus, for example, a potential shift may occur in that a DC voltage is superimposed upon the changing signal. It is furthermore possible that the pulse duty ratio of the changing signal changes. Depending on the device in which the control stage is
25 used and/or depending on the operating state, changes of this type can be intentional or can point to a fault in the control stage.

30 It is the object of the present invention to monitor the state of an alternating signal in a simple way.

This object is achieved by means of a method according to the main claim and by means of a device in accordance with the first substantive claim.

35 According to the invention, an alternating signal which is generated, for example, by a control stage or by an oscillator, is conditioned in such a way that, by means of comparing the conditioned signal with reference values, signals are generated which can be evaluated in a simple way.



The conditioning of the changing signal can be effected, for example, in that the latter is essentially smoothed. The value of the smoothed signal is a measure of a possible DC component and/or of the clock ratio of
5 the changing signal.

Another possibility for conditioning is, for example, to route the changing signal via a capacitor which is connected in series between a first stage, which is generating the changing signal, and a second stage,
10 which is controlled by this signal. In this arrangement, the first side of the capacitor, which is connected to the second stage, is charged by means of a voltage source, a current source or the like in such a way that, in the event of no change or only small changes in the
15 potential at the second side, connected to the first stage, of the capacitor, the first side assumes specific voltage values in accordance with a prescribed time variation.

It should be pointed out that both the alternating
20 signals which are used for control and the signals which are derived therefrom can be conditioned.

A variation in the pulse duty ratio and/or the DC component of the alternating signal can, for example, be used for controlling a connected stage or can also point
25 to a functional disturbance. Thus, for example, in the case of a control stage of the type mentioned, an uncontrolled state may occur in which the output signal from the control stage corresponds to a DC voltage level, a positive operating voltage or earth potential. This can
30 be caused, for example, by induction peaks or the like which influence the sequence of a control program which is being used for the functioning of the control stage. It is likewise conceivable that elements of the control stage become defective, that the supply voltage of the
35 control stage fails, or the like.

In the cases mentioned, faulty functioning occurs of the stages connected to the control stage.

It is an advantage of the present invention that states of this type can be detected in a simple way and



a prescribed state of the connected stages can then be controlled.

Operational monitoring of this type can be used, for example, in the case of a device such as a video recorder which drives a tape on which information is stored and from which information can be read.

Further features, advantages and details of the invention are explained in the following exemplary embodiments, with reference to the drawing, in which:

Fig. 1: shows the block diagram of a first exemplary embodiment;

Fig. 2: shows variations of signals in the exemplary embodiment of Fig. 1

Fig. 3: shows the block diagram of a second exemplary embodiment;

Fig. 4: shows variations of signals in the exemplary embodiment of Fig. 3

Before the description of the exemplary embodiments is gone into in more detail, it should be pointed out that the blocks shown individually in the figures are merely used for improved understanding of the invention. Normally, individual blocks or a plurality of these blocks are combined into units. These blocks may be realized in integrated or hybrid technology or as program-controlled microcomputers, or as part of a program suitable for controlling it.

The elements contained in the individual stages can also be of separate design, however.

Fig. 1 shows an electronic control device 10, which routes control signals U_s via a conditioning stage, which in this exemplary embodiment is designed as a smoothing element 11, to a drive stage 12, which applies current to a motor 13. The smoothing element 11 comprises a resistor 11a, whose first terminal is connected to the output of the control device 10, and a capacitor 11b, which is connected between the second terminal of the resistor 11a and earth. The smoothing element 11 effects smoothing of the control signal U_s , as a result of which a signal U_i is formed. The latter is then fed to the



noninverting (+) inputs of a first comparator 14, a second comparator 15 and a third comparator 16. The comparators 14, 15, 16 are connected by their inverting (-) inputs to a first reference voltage Ur_1 , to a second reference voltage Ur_2 and to a third reference voltage Ur_3 . The output signals Ua_1 and Ua_3 from the comparators 14, 16 are each fed to an input of an EXCLUSIVE-OR gate 17, whose output signal So is fed to further drive means which apply current to the motor 13. These further drive means, which inter alia contain an output stage, and means which evaluate the signal So and a signal Ss of a starting stage 19 and then drive the output stage as described below, are represented symbolically in Fig. 1 by the stage 18.

The output signal Ua_2 from the comparator passes to the starting stage 19, whose output signal Ss is fed to the stage 18.

The functioning of the exemplary embodiment of Fig. 1 is explained below with the aid of Fig. 2 only to the extent that is necessary for understanding the present invention.

In order to start the motor 13 running, the control device 10 outputs the clocked control signal Us , which leads to a smoothed signal Ui , as is represented in Figures 2a and 2b in the interval between t_0 and t_1 . The signal Ui has a residual ripple which, for the purposes of better understanding, is drawn somewhat exaggerated. The values of the reference voltages Ur are likewise drawn in Figure 2b. The comparators output signals Ua , as is shown in Figures 2c) to 2e).

Normal operation, such as is present during the interval between t_0 and t_1 , will be considered first. On the basis of the signal Ui , the comparator 15 simulates the output signal Ua_2 with a variation which corresponds to the clock rate of the original output signal Us , with a clock ratio t_h/t_l during a period T . The signal Ua_1 is "low", that is to say it assumes the digital value "0", and the signal Ua_2 is "high", corresponding to the value "1". Hence, as can be seen from Fig. 2f, the output



signal S_o of the EX-OR gate 17 is high, as a result of which the operation of the output stage containing the stage 18 is not impaired.

5 In this exemplary embodiment, the signal U_s is used not only for initiating a motor start but also for operational monitoring of the control device 10. If a disturbance should occur during the operation of the control device 10, as a result of which the control device assumes an operating voltage value which, in this
10 exemplary embodiment, can be U_+ or earth, the state of the signal S_o of the gate 17 changes, and the driving of the output stage contained in stage 18 changes therewith.

Firstly, let possible disturbed operation in the interval between t_1 and t_2 be considered, in which the
15 signal U_s assumes the positive operating voltage U_+ , as a result of which U_{a2} also becomes "high". Since U_+ is greater than both U_{r1} and U_{r3} , both the signals U_{a1} , U_{a3} are "high" and the signal S_o of the gate 17 becomes "low". This has the effect that the stage 18 slows down
20 the motor 13 in a prescribed way from an instantaneous rotational speed to a standby speed. This standby speed can mean, for example, the standstill of the motor 10.

A second possible disturbed case is shown above the time t_2 . Here the signals U_s and U_i are intended to
25 assume the value of earth potential. Since this lies below both U_{r1} and U_{r3} , the signals U_{a1} and U_{a3} become "low". Hence, S_o is also "low" and standby operation is maintained.

The cases shown in Fig. 2 represent a special
30 case to the extent that the first disturbance (t_1 - t_2) occurs first and the second disturbance (after t_2) then occurs subsequently. It is of course possible that the signal U_i falls directly to earth potential after normal operation. As a result, standby operation is then accord-
35 ingly initiated, in that the motor 13 is slowed down.

In describing this exemplary embodiment it was initially assumed that the signal U_s was sampled between the two values U_+ , U_m of the operating voltages. However, it is also possible that a lower range is provided for

the signal U_s . In this case, the circuit of Fig. 1 can also be used for the purpose of determining a possible DC component of the signal U_s .

5 The block diagram of a second exemplary embodiment is shown in Fig. 3 and is explained with the aid of Fig. 4. Means and signals having an analogous function as in the case of the exemplary embodiment of Fig. 1 and Fig. 2 are designated as they were there. They will be discussed below only to the extent that is essential for
10 the understanding of the present invention.

The essential difference from the exemplary embodiment of Fig. 1 lies in the fact that another type of conditioning of the signal U_s is carried out. The latter is not routed via the smoothing element 11 but via
15 a capacitor 20, which is connected in series with a resistor 21. At the connection between the elements 20, 21 a signal U_i' is tapped off and fed to the comparators 14, 15, 16. In this case the signal U_i' passes in each case at the comparators 14 and 15 to the noninverting
20 input and at the comparator 16 to the inverting input. The resistor 21 is connected to the centre tap of a voltage divider which is formed from resistors 22, corresponding to 22a-22d, and which serves to generate the reference voltages U_{r1} , U_{r2} , U_{r3} , which are in each
25 case applied to the free inputs of the comparators 14-16. The output signals U_{a1} and U_{a3} are fed to the OR-gate, which is designated here by 17', since in this exemplary embodiment it can be designed as a "simple" OR-gate, and does not necessarily need to be an EXCLUSIVE-OR gate. In
30 the case of a preferred embodiment, the gate 17' is realized by two diodes which are in each case connected downstream of the comparators 14 and 15 in the forward direction, as is indicated inside block 17'.

Connected downstream of gate 17 is a capacitor 23
35 which has the effect that, if the signal S_0 is switched over briefly, this is not noticeable by the stage 18.

Figures 4a and 4b show the variation of the signals U_s and U_i' . In the event of a change of U_s from "low" to "high", the right-hand side of the capacitor 20



(see Fig. 3), from which the signal U_i' is taken, is recharged in a finite time, that is to say only approximately abruptly, to a voltage whose value is close to the positive supply voltage U_+ of the control device 10. As long as U_s remains "high", the right-hand capacitor side is discharged exponentially via the resistor 21 in the direction of the reference voltage U_{r2} , which is picked off at the centre tap of the voltage divider.

The values for the elements 20, 21 are selected in such a way that, within the intervals t_h and t_l , in which the signal U_s is respectively "high" and "low" in normal operation, the signal U_i' does not fall below the first reference value U_{r1} or does not exceed the third reference value U_{r3} , respectively. Hence, in normal operation, during the intervals t_h , the first output signal U_{a1} is "high" (see Fig. 2c) and the third output signal U_{a3} is "low" (see Fig. 2e).

At this point it should be noted that the vertical auxiliary lines of Fig. 4, which are drawn with dashed lines or chain-dotted lines, have the following meaning: the chain-dotted lines mark the points in time at which the signal U_s changes its state in each case. The dashed lines mark those points in time at which the signal U_i' respectively exceeds or falls below the second reference value U_{r2} and at which the signal U_{a2} accordingly respectively changes its state. In this case, gate propagation times have been neglected.

In the case of a change in the signal U_s from "high" to "low", the signal U_i' falls with a finite speed to a value which virtually corresponds to that of the earth potential U_m . The exponential voltage variation on the right-hand side of the capacitor once more tends to U_{r2} , the third reference voltage U_{r3} not being exceeded in normal operation, however.

By means of the variation of the signal U_i' , as is shown in Fig. 2b in the interval t_0 to t_1 , the effect is achieved that one of the output signals U_{a1} , U_{a2} is always "high", if it is initially neglected that in the event of a voltage jump in U_s the signal U_i' does not



follow arbitrarily quickly. Hence, the output signal S_o of the gate 17 is "high" in normal operation. However, since, as already indicated, U_i' rises or falls only at a finite speed, brief drops in the signal S_o are to be expected. However, these are smoothed by the capacitor 23 in such a way that they are not noticeable by the stage 18 and that taking account of the jumps can be omitted in Fig. 4f.

In implementing the OR-gate 17', it is to be taken into account that, during the brief drops in its output signal, discharging of the capacitor 23 is avoided. This is achieved, for example, by realizing the gate 17' by means of the two diodes, which are drawn in block 17'. It is furthermore possible to use another type of OR gate, such as is realized, for example, by a TTL gate. However, an additional diode is then possibly necessary between the output of the gate 17' and the capacitor 23.

If normal operation is left at a point in time t_1 , in that the signal U_s assumes the constant "high" value, the exponential voltage drop on the right-hand side of the capacitor leads to the voltage falling below the first reference voltage U_{r1} at the point in time t_1' . Then, apart from the third output signal U_{a3} , the first output signal U_{a1} also becomes "low" and hence also the gate output signal S_o . This situation is detected by the stage 18, which then drives the output stage contained in it in such a way that the motor 13 is slowed down to a standby speed.

In the case of an operational disturbance, in which the signal U_s constantly assumes the earth potential, as is intended to be carried out after a point in time t_2 , U_i' initially falls below the values of the two reference voltages U_{r1} , U_{r3} , as a result of which normal operation is briefly faked by the gate signal S_o . However, from a point in time t_2' the reference value U_{r3} is exceeded and an operational disturbance is detected.

The advantage of the exemplary embodiment of Fig. 2 as compared with that of Fig. 1 lies in particular



in the fact that there is reliable monitoring for the control device 10 and the drive stage 12 even in the case of different operating voltages U_+ , U_+' . In the event that the second reference voltage U_{r2} has a value of 2.5 volt and the two other reference voltages U_{r1} , U_{r3} lie symmetrically around this value, faulty functioning occurs in Fig. 1 if the operating voltage U_+ of the control device 10 is, for example, 2 volt or 10 volt and the control signal U_s is sampled between U_+ and earth. Even in the case of slight deviations in the operating voltages from each other, faulty functioning is to be expected in the case of the exemplary embodiment according to Fig. 1, but not in the case of the circuit of Fig. 3.

In the case of configuring the exemplary embodiment according to Fig. 3, the charging of the right-hand side of the capacitor can be effected by means of a controlled current source. The latter is connected, for example, directly between the right-hand side of the capacitor and an operating voltage, such as U_+' or earth, and can be controlled by a comparison signal whose value is a measure of the voltage difference between that voltage applied to the right-hand side of the capacitor and a desired voltage such as, for example, the second reference voltage U_{r2} . Depending on the current source and the said comparison signal, a desired variation of voltage with time can be set for the right-hand side of the capacitor. This can vary exponentially, linearly or in accordance with another function.

Further versions of the exemplary embodiments can have at least one of the following variations:

- the signal U_s can be divided into a first signal, which is used for driving the stage 18 and can be fed to the latter directly, and into a second signal which is used for monitoring the alternating signal U_s . In this case, a second feed line to the circuit 12 is necessary, but the comparator 15 can be dispensed with;
- by means of suitable selection of the values for the



reference voltages U_r , it is possible not only to detect when the signal U_s assumes a DC value, but also to detect exceeding or falling below prescribed pulse duty ratios;

- 5 - more than three reference voltages can be provided. As a result it is possible, for example, to detect corresponding DC components and further functions in the circuit 12 can then be controlled using only one connecting line. If the signal U_s is designed as a
- 10 pulse-width-modulated (PWM) signal, it is also possible to detect corresponding values of the clock ratio corresponding to the number of reference voltages. This can be used for monitoring the operation of a load, such as that of the motor 13.
- 15 Reference should be made at this point in particular to the previous Applications P 42 27 761.2, in which the determination is described of the value of a current with which a PWM load is driven, and to P 42 29 344.8, in which a load is controlled as a
- 20 function of a temperature;
- after a disturbance has been detected once, in the event that a normal case is detected later, the stage 18 can automatically once more control a downstream load, such as the motor 13, into normal
- 25 operation, or provision can also be made for this to be effected only after the receipt of a confirmation signal which is output by means which are not shown or by a user of the system whose functioning is being monitored;
- 30 - the exemplary embodiments can be used as part of a video recorder, a compact disk (CD) player or another device having a motor;
- instead of a device with a motor, functions of other devices or systems can be monitored in the ways
- 35 described;
- instead of functional monitoring, the manner in which control signals are converted into U_i and U_i' , respectively, and the subsequent evaluation can also be used for controlling other functions.





PATENT CLAIMS

1. Method for monitoring an alternating signal (U_s), characterized in that
 - the alternating signal (U_s) is conditioned in such a way that a conditioned signal (U_i ; U_i') is generated whose time variation is a measure of the clock ratio and/or of the possible DC component of the alternating signal, in that
 - the conditioned signal (U_i ; U_i') is compared with prescribed reference values (U_{r1} , U_{r3}), as a result of which corresponding comparison values (U_{a1} , U_{a3}) are produced, and in that
 - on the basis of the comparison values (U_{a1} , U_{a3}), conclusions are drawn about the clock ratio and/or the DC component of the alternating signal.
2. Method according to Claim 1, characterized in that the alternating signal (U_s) is conditioned in that it is smoothed, the conditioned signal (U_i) having a DC component whose value is a measure of the clock ratio and/or the DC component of the alternating signal (U_s), and being able to have an AC component with a prescribed amplitude, the alternating signal (U_s) optionally being able to be regenerated from the AC component (U_{a2}).
3. Method according to Claim 1, characterized in that the alternating signal (U_s) is conditioned in that a signal derived from it has applied to it a voltage in such a way that, following a voltage change in the alternating signal (U_s), the derived signal tends towards a prescribed voltage value (U_{r2}) with a prescribed time variation.
4. Method according to one of Claims 1 to 3, characterized in that, on the basis of the comparison signals (U_{a1} , U_{a3}), a control signal (S_o) is formed whose value is a measure of a possible operational disturbance.
5. Method according to one of Claims 1 to 4, characterized in that, on the basis of the values of the comparison signals (U_{a1} , U_{a3}), means (13), which can be controlled with the aid of the alternating signal, are controlled down into quiescent operation (standby





operation).

6. Device for monitoring an alternating signal (U_s) which is generated by generator means (10), characterized in that

- 5 - a conditioning stage (11; 20, 21) is provided which conditions the alternating signal (U_s) in such a way that a conditioned signal (U_i ; U_i') is generated whose time variation is a measure of the clock ratio and/or a possible DC component of the alternating
- 10 signal, in that
- comparison means (14, 16) are provided which compare the conditioned signal (U_i ; U_i') with prescribed reference values (U_{r1} , U_{r3}), as a result of which corresponding comparison values (U_{a1} , U_{a3}) are
 - 15 produced, and in that
 - evaluation means (17, 18) are provided which, on the basis of the comparison values (U_{a1} , U_{a3}), draw conclusions about the clock ratio and/or the DC component of the alternating signal.

20 7. Device according to Claim 6, characterized in that the conditioning stage contains smoothing means (11) which smooth the alternating signal (U_s) in such a way that the conditioned signal (U_i) has a DC component whose value is a measure of the pulse duty ratio and/or the DC

25 component of the alternating signal (U_s), and can have an AC component with a prescribed amplitude, the alternating signal (U_s) optionally being able to be regenerated from the AC component (U_{a2}).

8. Device according to Claim 6, characterized in

30 that the conditioning stage has a capacitor (20) which is connected by its first terminal to the generator (10), in that there is a voltage or current device (21, 22) which charges or discharges the second terminal with a prescribed current, as a result of which a conditioned

35 signal (U_i') is generated which, following a voltage change of the alternating signal (U_s), tends towards a prescribed voltage value (U_{r2}) with a prescribed time variation.

9. Device according to one of Claims 6 to 8, charac-





terized in that, on the basis of the comparison signals (Ua1, Ua3), evaluation means (17) form a control signal (So) whose value is a measure of a possible operational disturbance.

- 5 10. Device according to one of Claims 6 to 9, characterized in that, on the basis of the values of the comparison signals (Ua1, Ua3), means (13) which can be controlled with the aid of the alternating signal are controlled down into quiescent operation (standby
10 operation).

