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(54) Title: REDUCED TEMPERATURE ETCHING OF DOPED SILICON OXIDE

(57) Abstract: Examples are disclosed that relate to etching features in a layer of silicon oxide doped with an etch rate-modifying dopant. One example provides a method of performing a memory device fabrication process. The method comprises placing a substrate in a processing chamber of a processing tool, the substrate comprising a first structure comprising alternating layers in a mold stack for a 3D memory structure, and the substrate also comprising a second structure comprising a silicon oxide layer doped with an etch rate-modifying dopant. The method further comprises controlling the processing tool to perform an etching cycle comprising etching at least a portion of a channel hole in the first structure of the substrate and at least a portion of a hole in the second structure of the substrate.

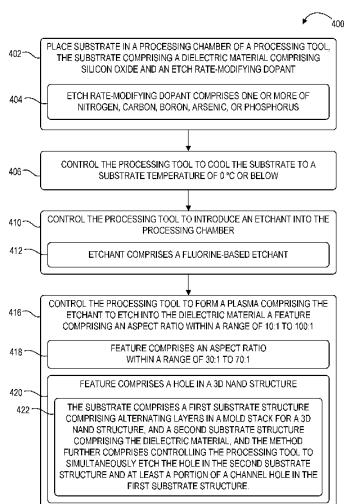


FIG. 4

SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN,
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