Description

Technical Field

This invention relates to processes for bonding conductors to bonding pads of a substrate.

Background of the Invention

Electronic circuit systems are typically made by defining complex integrated circuit structures on semiconductor chips, bonding the chips to circuit package substrates, and in turn bonding the packages to printed circuit boards. The most common bonding technique is wire bonding, in which an instrument (a thermode) thermocompression bonds wire to a bonding pad of one element, such as a chip, and then pulls the wire and makes a bond on bonding pad of a second element so as to form an arcuate self-supporting wire bridge between the two bonding pads.

An alternative to wire bonding which has found a substantial degree of commercial acceptance is tape automated (TAB) bonding, a technique described, for example, in the publication "The Basics of Tape Automated Bonding," Hybrid Circuit Technology, November 1984, Pages 15-21. In TAB bonding, a dielectric tape contains conductors to be bonded to a chip. The conductors overlap in cantilever fashion a window in the tape such as to match a row of bonding pads arranged on the periphery of the chip. Solder bumps on the ends of the conductors may be bonded by reflow soldering to the bonding pads of the chip. A dielectric tape may contain a large number of such windows which permits automated soldering of conductor arrays to successive chips. Opposite ends of the conductors may thereafter be bonded, for example, to a package substrate.

A trend that has been clear for a number of years in the integrated circuit field has been a steady increase in the density of conductors used on semiconductors chips, package substrates, and printed circuit boards. The bonding pads that must be used for making an interconnection between each conductor of one element and the circuitry of another element must typically be wider than the width of the conductors to accommodate the bonding process. Thus, there has been difficulty in arranging on the periphery of a chip, for example, all of the bonding pads needed for accommodating all of the conductors of the chip. If care is not taken in the proper organization of bonding pads, one obviously runs the risk of accidental short circuits. For example, in wire bonding, the wire interconnection may sag if designed to bridge too great a distance. TAB bonding assumes the organization of bonding pads in a peripheral array, which is inherently limiting.

The U.S patent of Ketchpel, No. 4,255,613, granted March 10, 1981, describes an interconnection method using conductors that overlap a tape. The publication, *IBM Technical Disclosure Bulletin*, Vol. 24, No. 12, May 1982, pp.6388-6389, describes a method for using multiconductor tapes for contacting parallel rows of termination sites.

According to the present invention, there is provided a process as defined in claim 1.

In accordance with one specific embodiment of the invention, a process for interconnecting in which the circuitry of two substrates comprises the step of terminating the circuitry on bonding pads that are arranged in parallel rows with the first row of each substrate being nearest an edge of the substrate. The bonding pads of the two first rows of the two substrates are joined by conductors of a dielectric tape that bridges the two substrates. The conductors overlap the edges of the dielectric tape and are organized to permit them to be bonded to corresponding bonding pads of the two substrates, for example, by soldering. The two second rows of bonding pads are joined by conductors on a second dielectric tape which is wide enough to cover two first rows of bonding pads and thereby provide electrical insulation. In like manner, successive tape layers are of progressively wider widths to provide insulation from interconnections beneath them, while permitting conductors carried by the tapes to overlap the edges and contact exposed bonding pads. In this manner, the principle of TAB bonding can be used for making connections to the bonding pads of chips without the need for arranging all of the bonding pads in a single row along the edge of the chip.

Various other embodiments and uses of the invention will be apparent from the consideration of the following detailed description taken in conjunction with the accompanying drawing.

Brief Description of the Drawing

Figures 1, 2, and 3, respectively, illustrate successive steps in a process for interconnecting the bonding pads of two adjacent substrates.

Detailed Description

Referring now to FIG. 1, there is shown two substrates 10 and 11 each containing electrical circuitry (not shown) which is to be interconnected. Substrate 10 may, for example, be a semiconductor chip while substrate 11 may be a circuit package substrate containing circuitry which one desires to connect permanently to the circuitry of the chip. Individual conductors of the circuitry of the two substrates terminate in bonding pads which are

shown on the drawing as squares. The circuits of the two substrates are interconnected by interconnecting appropriate bonding pads of the two substrates.

The circuit conductors of the two substrates can typically be made of a much smaller width than that of the individual bonding pads. The bonding pads must typically be at least 4 mils (100 micrometers) square to ensure reliable bonding; whereas the conductors may typically have a width of only 1 micrometer and still give dependable electrical conduction. Moreover, to insure against accidental short-circuits, it is customary to have a significantly greater spacing between bonding pads than between circuit conductors. Thus, as the density of the circuitry increases, it becomes increasingly difficult to arrange all of the bonding pads along the edge or the periphery of a substrate.

In accordance with the present invention, the bonding pads of each of the two substrates are organized in parallel rows A-E such that proper interconnection between the circuits of the two substrates is made when a bonding pad of one substrate is interconnected to the corresponding bonding pad of the corresponding row of the other substrate. Corresponding bonding pads of the two A rows are interconnected by parallel conductors 13 which are formed on a dielectric tape 14. The dielectric tape has a width slightly smaller than the distance between row A of substrate 10 and row A of substrate 11. The ends of conductors 13 overlap opposite edges of dielectric tape 14 and are spaced such as to make contact with corresponding bonding pads of the two A rows of the two substrates. Thus, when positioned as shown in FIG. 1, the free ends of conductors 13 may conveniently be bonded to the bonding pads of the two A rows by any convenient process, such as reflow soldering or thermocompression bonding.

Preferably, the free ends of each conductor 13 includes "bumps" of solder which, after proper registration of the conductors 13 with the bonding pads, are melted and adhere to the bonding pads A through reflow soldering. The dielectric tape 14 may, for example, be Kapton (a trademark of the DuPont Company) which is commonly used as a dielectric tape in TAB bonding. In accordance with known TAB bonding principles, the conductors 13 may be adhered to the tape 14 either through use of an appropriate adhesive, or by a deposition technique known as sputtering. Reflow soldering is conventionally effected by contacting the free ends of the conductors 13 with a hot thermode. During the soldering, a fixture holds the tape 14 in place.

Referring to FIG. 2, after the bonding pads of rows A have been interconnected, bonding pads of rows B are interconnected by conductors 16 included on a dielectric tape 17. The dielectric tape is of sufficient width so as to overlie and cover completely the bonding pads of the two A rows and the conductors 13. Thus, the conductors 16 are electrically insulated from the bonding pads of rows A and conductors 13. As before, the conductors 16 overlap the edges of dielectric tape 17 and can thus be conveniently soldered to the bonding pads of row B of substrate 10 and row B of substrate 11.

In like manner, a successive layer of dielectric tape covers the bonding pads of rows B and carries conductors for interconnecting the C rows of the two substrates. Thereafter, the D rows of bonding pads are interconnected in the same manner.

Referring to FIG. 3, there is shown the final dielectric tape 19 used to carry conductors 20 that interconnect the outer rows E of the two substrates. This final dielectric tape has a sufficient width to cover bonding pads A-D of the two substrates and associated interconnections. For purposes of completeness, conductors 21 for interconnecting the bonding pads of the D rows, conductors 22 for interconnecting the bonding pads of the C rows, conductors 16 for interconnecting the bonding pads of the B rows, and conductors 13 for interconnecting the bonding pads of A rows are all shown in phantom.

The bonding pads of each row may typically be made with a center-to-center spacing of 10 mils. The rows are preferably staggered as shown to prevent overlapping of the interconnecting conductors. Thus, the total thickness of the interconnection assembly is not significantly greater than that of conventional TAB bonding.

Another advantage of the invention is that one can easily inspect each of the bonds of the successive interconnection levels. That is, the dielectric tape doesn't obscure the conductors which are bonded at the time the bond is made; this would not be true for certain other bonding techniques in which there is no overlap by the conductors of the tape carrier.

While the invention has been shown as being used to interconnect the bonding pads of two substrates, it is to he understood that the bonding pads of substrate 10, for example, could be bonded as shown, but a completely different technique could be used for bonding the other ends of conductors to the bonding pads of substrate 11.

Claims

1. A process for interconnecting bonding pads arranged in at least first, second, third, and fourth bonding pad arrays comprising the steps of forming first conductors on a first dielectric tape such that free ends of the conductors overlap opposite edges of the first tape to have a configuration corresponding to the

shown on the drawing as squares. The circuits of the two substrates are interconnected by interconnecting appropriate bonding pads of the two substrates.

The circuit conductors of the two substrates can typically be made of a much smaller width than that of the individual bonding pads. The bonding pads must typically be at least 4 mils (100 micrometers) square to ensure reliable bonding; whereas the conductors may typically have a width of only 1 micrometer and still give dependable electrical conduction. Moreover, to insure against accidental short-circuits, it is customary to have a significantly greater spacing between bonding pads than between circuit conductors. Thus, as the density of the circuitry increases, it becomes increasingly difficult to arrange all of the bonding pads along the edge or the periphery of a substrate.

In accordance with the present invention, the bonding pads of each of the two substrates are organized in parallel rows A-E such that proper interconnection between the circuits of the two substrates is made when a bonding pad of one substrate is interconnected to the corresponding bonding pad of the corresponding row of the other substrate. Corresponding bonding pads of the two A rows are interconnected by parallel conductors 13 which are formed on a dielectric tape 14. The dielectric tape has a width slightly smaller than the distance between row A of substrate 10 and row A of substrate 11. The ends of conductors 13 overlap opposite edges of dielectric tape 14 and are spaced such as to make contact with corresponding bonding pads of the two A rows of the two substrates. Thus, when positioned as shown in FIG. 1, the free ends of conductors 13 may conveniently be bonded to the bonding pads of the two A rows by any convenient process, such as reflow soldering or thermocompression bonding.

Preferably, the free ends of each conductor 13 includes "bumps" of solder which, after proper registration of the conductors 13 with the bonding pads, are melted and adhere to the bonding pads A through reflow soldering. The dielectric tape 14 may, for example, be Kapton (a trademark of the DuPont Company) which is commonly used as a dielectric tape in TAB bonding. In accordance with known TAB bonding principles, the conductors 13 may be adhered to the tape 14 either through use of an appropriate adhesive, or by a deposition technique known as sputtering. Reflow soldering is conventionally effected by contacting the free ends of the conductors 13 with a hot thermode. During the soldering, a fixture holds the tape 14 in place.

Referring to FIG. 2, after the bonding pads of rows A have been interconnected, bonding pads of rows B are interconnected by conductors 16 included on a dielectric tape 17. The dielectric tape is of sufficient width so as to overlie and cover completely the bonding pads of the two A rows and the conductors 13. Thus, the conductors 16 are electrically insulated from the bonding pads of rows A and conductors 13. As before, the conductors 16 overlap the edges of dielectric tape 17 and can thus be conveniently soldered to the bonding pads of row B of substrate 10 and row B of substrate 11.

In like manner, a successive layer of dielectric tape covers the bonding pads of rows B and carries conductors for interconnecting the C rows of the two substrates. Thereafter, the D rows of bonding pads are interconnected in the same manner.

Referring to FIG. 3, there is shown the final dielectric tape 19 used to carry conductors 20 that interconnect the outer rows E of the two substrates. This final dielectric tape has a sufficient width to cover bonding pads A-D of the two substrates and associated interconnections. For purposes of completeness, conductors 21 for interconnecting the bonding pads of the D rows, conductors 22 for interconnecting the bonding pads of the C rows, conductors 16 for interconnecting the bonding pads of the B rows, and conductors 13 for interconnecting the bonding pads of A rows are all shown in phantom.

The bonding pads of each row may typically be made with a center-to-center spacing of 10 mils. The rows are preferably staggered as shown to prevent overlapping of the interconnecting conductors. Thus, the total thickness of the interconnection assembly is not significantly greater than that of conventional TAB bonding.

Another advantage of the invention is that one can easily inspect each of the bonds of the successive interconnection levels. That is, the dielectric tape doesn't obscure the conductors which are bonded at the time the bond is made; this would not be true for certain other bonding techniques in which there is no overlap by the conductors of the tape carrier.

While the invention has been shown as being used to interconnect the bonding pads of two substrates, it is to he understood that the bonding pads of substrate 10, for example, could be bonded as shown, but a completely different technique could be used for bonding the other ends of conductors to the bonding pads of substrate 11.

Claims

1. A process for interconnecting bonding pads arranged in at least first, second, third, and fourth bonding pad arrays comprising the steps of forming first conductors on a first dielectric tape such that free ends of the conductors overlap opposite edges of the first tape to have a configuration corresponding to the

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desired interconnections to the first and second arrays;

locating the first tape between the first and second arrays; and

bonding the free ends of the first conductors to bonding pads of the first and second arrays;

said third array of bonding pads is located adjacent the first array and said fourth array of bonding pads is located adjacent the second array such that the first and second arrays are located between the third and fourth arrays;

forming second conductors on a second dielectric tape such that free ends of the conductors overlap opposite edges of the second tape to have a configuration corresponding to the desired interconnections to the third and fourth arrays;

locating the second tape such that it covers the first tape, the first conductors and the first and second arrays of bonding pads; and

bonding the free ends of the second conductors to bonding pads of the third and fourth arrays.

2. The process of claim 1 further CHARACTERIZED IN THAT the first array of bonding pads is arranged in a first row along a first substrate;

the second array of bonding pads is arranged in a second row along a second substrate;

the third array comprises a row of bonding pads on the first substrate
parallel to the first row; and

the fourth array comprises a fourth row of bonding pads on the second substrate parallel to the second row.

3. The process of claim 2 further CHARACTERIZED IN THAT the bonding pads of the third row are staggered with respect to the bonding pads of the first row and the bonding pads of the fourth row are staggered with respect to the bonding pads of the second row.

4. The process of claim 2 further CHARACTERIZED IN THAT the first substrate contains a plurality of other rows of bonding pads parallel to the first and third rows;

the second substrate contains a plurality of other rows of bonding pads parallel to the second and fourth rows;

conductors carried on dielectric tape are bonded to corresponding bonding pads of the first and second substrates such that the dielectric tape completely covers the bonding pads of the first and second substrates that have been previously bonded.

Patentansprüche

1. Verfahren zur Verbindung von Anschlußfeldern, die in mindestens einer ersten, zweiten, dritten und vierten Anschlußfeld-Anordnung angeordnet sind, mit folgenden Schritten:

erste Leiter werden auf einem ersten dielektrischen Band derart gebildet, daß die freien Enden der Leiter die sich gegenüberstehenden Ränder des ersten Bandes überlappen und eine Gestalt entsprechend den gewünschten Verbindungen zu den ersten und zweiten Anordnungen aufweisen;

das erste Band wird zwischen der ersten und zweiten Anordnung angeordnet;

die freien Enden der ersten Leiter werden mit den Anschlußfeldern der ersten und zweiten Anordnung gebondet;

die dritte Anordnung der Anschlußfelder ist der ersten Anordnung benachbart angeordnet und die vierte Anordnung der Anschlußfelder ist benachbart der zweiten Anordnung gelegen, so daß die erste und zweite Anordnung zwischen der dritten und vierten Anordnung zu liegen kommen;

zweite Leiter werden auf einem zweiten dielektrischen Band so geformt, daß die freien Enden der Leiter gegenüberliegende Ränder des zweiten Bandes überlappen, um eine Gestalt entsprechend den gewünschten Verbindungen zwischen der dritten und vierten Anordnung einzunehmen;

das zweite Band wird so angeordnet, daß es das erste Band, die ersten Leiter und die erste und zweite Anordnung von Anschlußfeldern bedeckt;

die freien Enden der zweiten Leiter werden an die Anschlußfelder der dritten und vierten Anordnungen gebondet.

2. Verfahren nach Anspruch 1,
dadurch gekennzeichnet, daß die erste Anordnung der Anschlußfelder in einer ersten Reihe entlang eines ersten Substrats angeordnet ist, daß die zweite Anordnung der Anschlußfelder in einer zweiten Reihe entlang eines zweiten Substrats angeordnet ist, daß die dritte Anordnung eine Reihe von Anschlußfeldern auf dem ersten Substrat parallel zur ersten Reihe umfaßt und daß die vierte Anordnung eine vierte Reihe von Anschlußfeldern auf dem zweiten Substrat parallel zu der zweiten Reihe aufweist.

3. Verfahren nach Anspruch 2,
dadurch gekennzeichnet, daß die Anschlußfelder der dritten Reihe mit Bezug auf die Anschlußfelder der ersten Reihe versetzt angeordnet sind und daß die Verbindungsfelder der

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vierten Reihe mit Bezug auf die Verbindungsfelder der zweiten Reihe versetzt angeordnet sind.

4. Verfahren nach Anspruch 2, dadurch gekennzeichnet, daß das erste Substrat eine Mehrzahl von weiteren Reihen von Anschlußfeldern parallel zur ersten und dritten Reihe enthält, daß das zweite Substrat eine Mehrzahl von weiteren Reihen von Anschlußfeldern parallel zur zweiten und vierten Reihe enthält und daß die auf dem dielektrischen Band angebrachten Leiter an entsprechende Anschlußfelder des ersten und zweiten Substrats so gebondet werden, daß das dielektrische Band die Anschlußfelder der ersten und zweiten Substrate vollständig bedeckt, die zuvor gebondet worden sind.

Revendications

1. Technique d'interconnexion de plages de connexion disposées dans au moins un premier, deuxième, troisième et quatrième réseaux de plages de connexion comprenant les étapes de formation de premiers conducteurs sur une première bande diélectrique de sorte que les extrémités libres des conducteurs chevauchent des bords opposés de la première bande pour avoir une configuration correspondant aux interconnexions désirées avec les premier et deuxième réseaux;

   placement de la première bande entre les premier et deuxième réseaux; et

   connexion des extrémités libres des premiers conducteurs aux plages de connexion des premier et deuxième réseaux;

   ledit troisième réseau de plages de connexion est placé à côté du premier réseau et ledit quatrième réseau de plages de connexion est placé à côté du deuxième réseau de sorte que les premier et deuxième réseaux sont situés entre les troisième et quatrième réseaux;

   formation de deuxièmes conducteurs sur une deuxième bande diélectrique de sorte que les extrémités libres des conducteurs chevauchent des bords opposés de la deuxième bande pour avoir une configuration correspondant aux interconnexions désirées avec les troisième et quatrième réseaux;

   placement de la deuxième bande pour qu'elle couvre la première bande, les premiers conducteurs et les premier et deuxième réseaux de plages de connexion; et

   connexion des extrémités libres des seconds conducteurs aux plages de connexion des troisième et quatrième réseaux;

2. Technique selon la revendication 1, CARACTERISEE en outre EN CE QUE le premier réseau de plages de connexion est disposé en une première rangée le long d'un premier substrat;

   le deuxième réseau de plages de connexion est disposé en une deuxième rangée sur un second substrat;

   le troisième réseau comprend une rangée de plages de connexion sur le premier substrat parallèle à la première rangée; et

   le quatrième réseau comprend une quatrième rangée de plages de connexion sur le second substrat parallèle à la deuxième rangée.

3. Technique selon la revendication 2, CARACTERISEE en outre EN CE QUE les plages de connexion de la troisième rangée sont décalées par rapport aux plages de connexion de la première rangée et les plages de connexion de la quatrième rangée sont décalées par rapport aux plages de connexion de la deuxième rangée.

4. Technique selon la revendication 2, CARACTERISEE en outre EN CE QUE le premier substrat contient une pluralité d'autres rangées de plages de connexion parallèles aux première et troisième rangées;

   le second substrat contient une pluralité d'autres rangées de plages de connexion parallèles aux deuxième et quatrième rangées;

   des conducteurs portés sur la bande diélectrique sont liés aux plages de connexion correspondantes des premier et second substrats de sorte que la bande diélectrique couvre complètement les plages de connexion des premier et second substrats qui ont été précédemment connectées.