

## **A RADIO FREQUENCY IDENTIFICATION TRANSCEIVER**

### **FIELD OF THE INVENTION**

**[0001]** The invention relates to a radio frequency identification transceiver.

### **BACKGROUND OF THE INVENTION**

**[0002]** Demand for Radio Frequency Identification (RFID) is increasing rapidly with advancement in integrated circuit (IC) technologies and decreasing size and cost of RFID tags. These enable numerous applications which require very small size and low-cost RFID readers. Some of these applications include tagging items in retail stores, warehouse management, baggage tracing and tracking at the airports. This increase in demand calls for a corresponding need for small form factor and low-cost handheld RFID readers.

**[0003]** RFID frequency bands start from as low as 125 kHz. But for long read range ultra-high frequency (UHF), 860 MHz to 960 MHz band, is preferred since the size of the reader and tags are comparable to wavelength. Further, the 860 MHz to 960 MHz band falls within the approved frequency bands for UHF RFID in major countries. For USA, the minimum frequency resolution is about 50 kHz. EPC Global Class-1 Generation-2 protocol focuses on the frequency band from 860MHz to 960MHz. The European RFID standard calls for stringent spectrum mask requirement as disclosed in publication European Telecommunications Standards Institute EN 302 208-1 V1.1.2, European Standard, 2006-03.

**[0004]** There are known single-chip transceivers providing radio frequency (RF), mixed-signal, and digital baseband functionality for a physical layer of a UHF RFID reader. The RFID reader IC has a die size of 21 mm<sup>2</sup> and is realized in a 0.18  $\mu$ m silicon germanium (SiGe) BiCMOS process. The chip dissipates 1.5 W when

simultaneously transmitting a +20 dBm signal and receiving -85 dBm tag signals in the presence of a 0 dBm self jammer.

[0005] There is also a known complementary metal-oxide-semiconductor (CMOS) RF transceiver for UHF mobile RFID reader operating at 900MHz band. The transceiver is designed and fabricated in a 0.18  $\mu\text{m}$  CMOS process, where the design focus is on the linearity rather than the noise figure.

[0006] There is also a known reader front-end which allows for detection of the tag information in the presence of large in-band blockers, based on the RFID range. The proposed reader allows for amplification of the weakest desired signal by 18 dB while rejecting the TX blocker and its noise floor as well as LO phase noise by 30 dB on average, resulting in a better than 50 dB of signal-to-blocker ratio. TX blocker rejection is achieved through a combination of signals traveling in two RF paths, a linear path and a nonlinear path. In the linear path, both the desired and the blocker signals are equally amplified through a low noise amplifier (LNA) and in the nonlinear path, the desired signal limits both the blocker and the desired signals. The limiting function only preserves the frequency and phase of the stronger blocker signal. The blocker signal is then rejected by subtracting the outputs of the linear and nonlinear paths. Therefore, the blocker signal is cancelled out but the desired signal is amplified through the linear path.

[0007] There is a known RFID reader accessible through a personal computer, where the RFID reader includes a PC card interface and a controller both operating according to clock signals from a crystal oscillator. The RFID reader further includes a linearized power amplifier modulator in a transmit path, a receive chain capable of demodulating EPC global Class\_1 and Class\_0 signals from RFID tags, and an integrated switching device for selecting one of a plurality of antenna for transmitting or receiving RF signals.

**[0008]** Another RFID reader provides sensitivity enhancement for a single antenna RFID interrogating device by separately coupling a nulling signal formed using a portion of a transmit signal into a receiver. The phase and amplitude of nulling signal can be adjusted so that the nulling signal cancels that a reflected transmit signal from the antenna, resulting in the small backscattered signal from the distant RFID tag to be more easily detected, and improving the sensitivity of the RFID receiver.

**[0009]** A known receiver uses a lumped constant network approach to eliminate costly and bulky couplers, circulators and distributed delay lines. A single-pole, four-throw (sp4t) antenna switching arrangement is also provided. The receiver provides a hand-held receiver capable of operation over distances of approximately three to five meters. This allows the construction of a hand-held receiver having high performance (i.e., a long reading distance) and good discrimination (i.e., the ability to accurately read closely-spaced tags moving rapidly past a check point). When used with compatible RFID tags, the system may also be used to alter the identification or other information stored within the RFID tags.

**[0010]** It would be advantageous to have a RFID transceiver that provides the above functions on a single integrated device and yet is able to operate in one of a plurality of predefined frequency ranges. The present invention provides such a RFID transceiver that matches the performance of currently available, but more expensive and bulkier RFID transceivers.

## **SUMMARY OF THE INVENTION**

**[0011]** According to one aspect of the invention, there is provided a radio frequency identification transceiver, including: a transmitter path, including; a pulse shaper to tunably shape the pulse of a signal to be transmitted in different predefined frequency ranges; a modulator to modulate the shaped pulse to be transmitted into one of a plurality of predefined frequency ranges; a receiver path, including: a

demodulator to demodulate a received signal from a plurality of predefined frequency ranges.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

**[0012]** In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the invention are described with reference to the following drawings, in which:

**[0013]** Figure 1 shows a block level representation of a RFID (Radio Frequency Identification) system built in accordance to an embodiment of the present invention

**[0014]** Figure 2 shows a block level representation of the architecture of a RFID transceiver built in accordance to an embodiment of the present invention.

**[0015]** Figure 2A shows a block level representation of a high pass filter of a RFID transceiver built in accordance to an embodiment of the present invention.

**[0016]** Figure 2B shows the frequency characteristics of a high pass filter of a RFID transceiver built in accordance to an embodiment of the present invention.

**[0017]** Figure 2C shows testing to detect the presence of the center frequency of a pre-selected channel.

**[0018]** Figure 3 shows a block level representation of a RFID system built in accordance to an embodiment of the present invention.

**[0019]** Figure 4 shows a block level representation of a RFID system built in accordance to an embodiment of the present invention.

[0020] Figures 5 and 6 show block level representations of RFID systems used under different operating conditions.

[0021] Figure 7 shows a block level representation of the architecture of a dual-loop phase locked loop (PLL) synthesizer of a RFID transceiver built in accordance to an embodiment of the present invention.

[0022] Figure 8 shows a schematic diagram of circuitry used to implement voltage-controlled oscillators used in a PLL synthesizer of an RFID transceiver built in accordance with an embodiment of the invention.

[0023] Figure 9 shows tuning curves for all eight bands of an 8-band voltage-controlled oscillator used in a RFID transceiver built in accordance with an embodiment of the invention.

[0024] Figure 10 shows a schematic diagram of a charge-pump circuit of a phase frequency detector (PFD) and a charge pump block used in a PLL synthesizer of an RFID transceiver built in accordance with an embodiment of the invention.

[0025] Figure 11 shows a schematic diagram of a single sideband (SSB) mixer in a PLL synthesizer of an RFID transceiver built in accordance with an embodiment of the invention.

[0026] Figure 12 illustrates image rejection of a SSB mixer.

[0027] Figure 13A shows a block level representation of the architecture of a receiver path of a RFID transceiver built in accordance to an embodiment of the present invention.

[0028] Figure 13B shows a block level representation of another architecture of a receiver path of a RFID transceiver built in accordance to an embodiment of the present invention.

[0029] Figure 14 shows a block level representation of the architecture of a receiver path front-end of a RFID transceiver built in accordance to an embodiment of the present invention.

[0030] Figure 15 shows a schematic diagram of a low noise amplifier (LNA) of a RFID transceiver built in accordance to an embodiment of the present invention.

[0031] Figure 16 shows a block level representation of the structure and configuration of a LNA in a receiver path of a RFID transceiver built in accordance to an embodiment of the present invention.

[0032] Figure 17 shows a schematic diagram of a down-conversion mixer, which can be used to realize an in phase mixer (I-Mixer) and a quadrature mixer (Q-Mixer) of a RFID transceiver built in accordance to an embodiment of the present invention.

[0033] Figure 18A shows a block level representation of a channel select filter (CSF) of a RFID transceiver built in accordance to an embodiment of the present invention.

[0034] Figure 18B shows frequency characteristics of a CSF.

[0035] Figure 19 shows a schematic diagram of a channel select filter (CSF) in a receiver path of a RFID transceiver built in accordance with an embodiment of the invention.

[0036] Figure 20 shows a block level representation of a variable gain amplifier (VGA) in a receiver path of a RFID transceiver built in accordance with an embodiment of the invention.

[0037] Figure 21 shows a schematic diagram of a VGA in a receiver path of a RFID transceiver built in accordance with an embodiment of the invention.

[0038] Figure 22 shows a block level representation of a pulse-shaping filter (PSF) in a transmitter path of a RFID transceiver built in accordance with an embodiment of the invention.

[0039] Figure 23A shows a block level representation of a PSF in a transmitter path of a RFID transceiver built in accordance with an embodiment of the invention.

[0040] Figure 23B shows frequency characteristics of a PSF.

[0041] Figure 24 shows a biquad structure schematic diagram of a PSF in a receiver path of a RFID transceiver built in accordance with an embodiment of the invention.

[0042] Figure 25 shows a block level representation of a modulator in a transmitter path of a RFID transceiver built in accordance with an embodiment of the invention.

[0043] Figure 26 shows a block level representation of a single sideband amplitude shift keying (SSB-ASK) unit used by a RFID transceiver built in accordance with an embodiment of the invention.

[0044] Figure 27 shows a block level representation of a power amplifier (PA) in a transmitter path of a RFID transceiver built in accordance with an embodiment of the invention.

[0045] Figure 28 shows a schematic diagram of a PA in a transmitter path of a RFID transceiver built in accordance with an embodiment of the invention.

[0046] Figure 29 shows a block level representation of a digital application specific integrated circuit (ASIC) of a RFID transceiver built in accordance with an embodiment of the invention.

[0047] Figure 30 summarises logic control of an ASIC.

[0048] Figure 31 shows the transmit spectrum mask for a multiple interrogator environment, which meets the EPC Gen-2 standard, and an output spectrum of a RFID transceiver built in accordance with an embodiment of the invention.

[0049] Figure 32 shows measured pulse-shaping filter characteristics of a RFID transceiver built in accordance with an embodiment of the invention.

[0050] Figure 33 shows measured carrier phase-noise at 860MHz and 960MHz of a RFID transceiver built in accordance with an embodiment of the invention.

[0051] Figure 34A shows DSB-ASK modulation of a RFID transceiver built in accordance with an embodiment of the invention.

[0052] Figure 34B shows PR-ASK modulation of a RFID transceiver built in accordance with an embodiment of the invention.

[0053] Figure 34C shows SSB-ASK modulation of a RFID transceiver built in accordance with an embodiment of the invention.

[0054] Figure 35A shows a channel-select filter response in listen before talk mode of a RFID transceiver built in accordance with an embodiment of the invention.

[0055] Figure 35B shows a channel-select filter response in talk mode of a RFID transceiver built in accordance with an embodiment of the invention.

[0056] Figure 36 shows a photograph of a die having a RFID transceiver built in accordance with an embodiment of the invention.

**[0057]** Figure 37 shows a photograph of a UHF (ultra high frequency) RFID reader system incorporating a RFID transceiver built in accordance with an embodiment of the invention.

**[0058]** Figure 38 shows a table summarizing the performance results of a RFID transceiver built in accordance with an embodiment of the invention.

**[0059]** Figure 39 shows a table summarizing the range performance results of a RFID transceiver built in accordance with an embodiment of the invention.

**[0060]** Figure 40 shows the response of a digital low pass filter (channel select filter) of a RFID transceiver built in accordance with an embodiment of the invention.

**[0061]** Figure 41A shows a signal in a transmission path of a RFID transceiver built in accordance with an embodiment of the invention.

**[0062]** Figure 41B shows a transmitted signal from a RFID transceiver built in accordance with an embodiment of the invention, along with a detection envelope.

**[0063]** Figure 41C compares a transmission spectrum mask of a RFID transceiver built in accordance with an embodiment of the invention against a detection envelope.

**[0064]** Figure 42A shows a detected signal, in time domain, in a RFID transceiver built in accordance with an embodiment of the invention.

**[0065]** Figure 42B shows a SSB modulation spectrum of a RFID transceiver built in accordance with an embodiment of the invention.

[0066] Figure 42C shows a detected signal, in time domain, in a RFID transceiver built in accordance with an embodiment of the invention.

[0067] Figure 43 shows waveforms in a receiver path of a RFID transceiver built in accordance with an embodiment of the invention, where an ideal local oscillator is used.

[0068] Figure 44 shows the effect of phase noise, with a blocking signal present, on signal performance of a RFID transceiver built in accordance with an embodiment of the invention.

[0069] Figure 45 shows a two-tone output spectrum emitted from a power amplifier of a RFID transceiver built in accordance with an embodiment of the invention.

## DESCRIPTION

[0070] While embodiments of the invention have been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced. It will be appreciated that common numerals, used in the relevant drawings, refer to components that serve a similar or the same purpose.

[0071] Figure 1 shows a block level representation of a RFID (Radio Frequency Identification) system 180 built in accordance to an embodiment of the present invention.

[0072] The RFID system 180 includes a RFID transceiver 100 electrically connected with a microcontroller (MCU) 104, a crystal oscillator 106, a transmitter/receiver (Tx/Rx) isolation unit 112 and a power amplifier (PA) 108. The PA 108 is in turn connected with a filter 110 and the filter 110 is also connected with the Tx/Rx isolation unit 112. An antenna 114 is coupled to the Tx/Rx isolation unit 112 to transmit signals (Tx\_out) 126 from the RFID transceiver 100 and to send received signals (Rx\_in) 124 to the RFID transceiver 100.

[0073] The RFID transceiver 100 includes a transmitter path 105 and a receiver path 102. The transmitter path 105 includes a pulse shaper 138 to tunably shape the pulse of a signal to be transmitted 126 in different predefined frequency ranges; a modulator 140 to modulate the shaped pulse to be transmitted 126 into one of a plurality of predefined frequency ranges. The receiver path 102 includes a demodulator 103 to demodulate the received signal 124 from a plurality of predefined frequency ranges.

[0074] It is advantageous to achieve isolation between the transmitter portion and the receiver portion in a RFID reader system having an integrated transmitter and receiver arrangement. This is because the transmitter output may leak into the receiver front-end if the transmitter and the receiver front-end are not sufficiently isolated. The capability of the receiver front end to handle a leaked signal from the transmitter, without affecting performing of the desired signals, is referred to as the receiver front-end linearity. It is difficult to achieve, using 0.18- $\mu$ m CMOS (Complimentary Metal Oxide Semiconductor) technology, an integrated transmitter and receiver arrangement that has the same linearity compared to a discrete transmitter and receiver arrangement. It was found that the above arrangement of the RFID system 180 provided good isolation between the transmitter portion and the receiver portion.

[0075] In use, the MCU 104 controls the operation of the RFID transceiver 100 by sending, to the RFID transceiver 100, data for transmission (Tx\_data) 116 and

serial peripheral interface (SPI) circuit control signals 118. The MCU 104 also processes both in-phase (I) receiver data (Rx\_data I) 120 and quadrature-phase (Q) receiver data (Rx\_data Q) 122 from the RFID module 100. The crystal oscillator 106 is used to provide a stable reference clock signal 128 to the RFID module 100, and has a resonance of 20MHz in this embodiment. The PA 108 allows for the RFID transceiver 100 to be used over longer distances.

[0076] The transmitted Tx\_out signal 126 is a carrier signal modulated with the Tx\_data 116, while Rx\_data I 120 and Rx\_data Q 122 RFID are both data demodulated from the received Rx\_in signal 124. The Tx/Rx isolation unit 112 ensures that the transmitted Tx\_out signal 126 and the received Rx\_in signal 124 are isolated from each other.

[0077] Figure 2 shows a block level representation of the architecture of a RFID transceiver 200 built in accordance to an embodiment of the present invention. It will be appreciated that the RFID transceiver 200 can be used in place of the RFID transceiver 100 of Figure 1.

[0078] The RFID transceiver 200 includes a receiver path 202, a transmitter path 204, a dual-loop phase locked loop (PLL) synthesizer 206 and a serial peripheral interface (SPI) circuit 208.

#### I) Receiver path 202

[0079] The receiver path 202 includes: a low-noise amplifier (LNA) 210; a set of in-phase (I) and quadrature-phase (Q) mixers 212i (I-Mixer) and 212q (Q-Mixer); a set of I and Q amplifiers 214i (I-Amp) and 214q (Q-Amp); a set of I and Q channel-select filters (CSF) 216i (I-CSF) and 216q (Q-CSF); a set of I and Q variable gain amplifiers (VGA) 218i (I-VGA) and 218q (Q-VGA); a set of analogue to digital converters (ADC) 220i and 220q; and an amplitude-shift keying (ASK) demodulator 222.

[0080] The Rx\_in signal 124 enters the input of the LNA 210, while the LNA 210 output is coupled to both respective inputs of the I-Mixer 212i and Q-Mixer 212q. Thus, the receiver path 202 includes at least one amplifier to amplify the received signal 124. The LNA 210 can operate in a high gain mode or a low gain mode depending on the different operation modes of the RFID transceiver 200.

[0081] The I-Mixer 212i and the Q-Mixer 212q outputs are coupled to respective inputs of the I-Amp 214i and the Q-Amp 214q respectively via external direct (DC) blocking capacitors 224. The I-Amp 214i and the Q-Amp 214q outputs are coupled to respective inputs of the I-CSF 216i and the Q-CSF 216q, while the outputs of the I-CSF 216i and the Q-CSF 216q are connected to respective inputs of the I-VGA 218i and the Q-VGA 218q. The I-VGA 218i output is coupled to the respective ADC 220i input and the ASK demodulator 222 input, while the Q-VGA 218q output is coupled to the respective ADC 220q input and the ASK demodulator 222 input.

[0082] The receiver path 202 uses a direct-conversion architecture, since the receiver input Rx\_in signal 124 includes a backscatter signal 228b from an RFID tag 228, where the backscatter signal 228b has the same frequency as the transmitted carrier in the transmitted Tx\_out signal 126. The receiver front-end down converts the received signal Rx\_in signal 124 to baseband signals. Also, at the receiver front-end, the LNA 210 is designed to achieve high sensitivity in the listen-before-talk (LBT) mode and high Input Third Order Intercept Point IIP3 in the talk-mode, where a control signal LBT/Talk Mode 226 determines the respective instantaneous mode (LBT or Talk) the LNA 210 is in. In the embodiment shown in Figure 2, the LNA 210 is designed with switchable gain, which provides the advantage that the LNA 210 can be used in both the listen-before-talk mode and talk-mode under the European Telecommunications Standards Institute (ETSI) RFID standard. The LNA 210 is switched to low gain for talk mode and high gain for LBT mode. The LNA 210 will be elaborated upon later with reference to Figures 15 and 16.

[0083] In a RFID system, RFID tags are not battery powered and work in a passive mode taking power from the RFID reader. The read range is limited mainly by the RFID tag 228 sensitivity rather than by the passive RFID reader sensitivity. Currently available RFID tags have sensitivity of around -10 dBm.

[0084] The PLL 206 is coupled to the I-Mixer 212i and the Q-Mixer 212q, so that the PLL 206 provides the I-Mixer 212i and the Q-Mixer 212q respectively with an in-phase local oscillator signal (I-LO) 230i and a quadrature local oscillator signal (Q-LO) 230q. The signals I-LO 230i and Q-LO 230q facilitate mixing, in the I-Mixer 212i and the Q-Mixer 212q, of the Rx\_in signal 124 with I and Q local oscillator (LO) frequencies employed by the RFID module 200, where the Rx\_in signal 124 includes the incoming backscatter signal 228b from the RFID tag 228. The mixing achieves down conversion in the I-Mixer 212i and the Q-Mixer 212q, so that the I-Mixer 212i provides an output signal 213 having a first differential in-phase signal and a second differential in-phase signal and the Q-Mixer 212q provides an output signal 215 having a first differential quadrature signal and a second differential quadrature signal.

[0085] The external blocking capacitors 224 help to block fixed DC offset.

[0086] In another embodiment, a high pass filter (not shown in Figure 2, but refer reference numeral 224/424 in Figure 4) is deployed in the receiver path 202, between the I-Mixer 212i and the Q-Mixer 212q outputs and their respective I-VGA 218i and Q-VGA 218q inputs. The high pass filter may be a single order high pass filter including external AC coupling capacitors 424 (Figure 4) and the input resistors of the respective I-VGA 214i and Q-VGA 214. Higher order high pass filters may be required which can be deployed as 224. Referring to Figure 2B in conjunction with Figure 2, to reduce information loss, the corner frequency 270 of the high pass filter is designed to be as low as possible. In designing the corner frequency 270 of the high pass filter to be as low as possible, the settling time increases. However, RFID protocols specify, for RFID tag detection, shorter data preambles compared to other

communication protocols. The shorter data preamble means that the RFID tag 228 has to be detected within a shorter settling time. Thus, to detect the RFID tag 228 via backscatter modulation, the high pass filter is made tunable in accordance to the backscatter signal 228b data rate settling time. For example, the corner frequency is chosen to be between about 5 to about 10 percent of the backscatter frequency.

[0087] Returning to Figure 2, since the I-Mixer 212i and the Q-mixer 112q have direct-conversion architectures, fully differential architecture is chosen for analog base-band signal processing components, namely the I-Amp 214i, the Q-Amp 214q, the I-CSF 216i, the Q-CSF 216q, the I-VGA 218i, the Q-VGA 218q, the ADCs 220i and 220q, and the ASK demodulator 222.

[0088] The I-Amp 214i and the Q-Amp 214q, acting as intermediate-frequency (IF) amplifiers, respectively amplify the output signal 213 (having the first differential in-phase signal and the second differential in-phase signal) emitted from the I-Mixer 212i and amplify the output signal 215 (having the first differential quadrature signal and the second differential quadrature signal) from the Q-Mixer 212q. In the embodiment shown in Figure 2, the I-Amp 214i and the Q-Amp 214q each provide amplification of around 12dB.

[0089] The I-CSF 216i and the Q-CSF 216q allows the RFID transceiver 200 to operate in channels complying with, in the embodiment shown in Figure 2, either the FCC (Federal Communications Commission) or the ETSI (European Telecommunications Standards Institute) standards. Each of the I-CSF 216i and the Q-CSF 216q have a tunable pass-band frequency to be either around 320 kHz or around 1.5 MHz. The tunable I-CSF 216i filters the amplified differential signal 217 provided by the I-Amp 214i, while the tunable Q-CSF 216q filters the amplified differential signal 219 provided by the Q-Amp 214q.

[0090] A received signal strength indicator (RSSI) circuit (not shown, but compare RSSI circuits 405i and 405q in Figure 4) may be placed along the receiver

path 202 to detect the strength of the signal (from the respective external blocking capacitors 224) realized in logarithmic form. The output from the RSSI circuit may be used to control the gains of both the I-VGA 218i and the Q-VGA 218q to improve the dynamic receive range. Successive detection architecture is adopted for realizing the logarithmic amplifier. It is composed of five stages of limiting amplifier combined with a full-wave rectifier and low pass filter. The limiting amplifier design may use the same architecture as the fixed gain amplifier shown in Figure 20.

[0091] The VGAs 218i and 218q each provide, in the embodiment shown in Figure 2, a 60dB gain in the receiver path 202, with control range of about 48 dB. The I-VGA 218i amplifies the output 221 (having the filtered first differential in-phase signal and the filtered second differential in-phase signal) from the I-CSF 216i. The Q-VGA 218q amplifies the output 223 (having the filtered first differential quadrature signal and the filtered second differential quadrature signal) from the Q-CSF 216q.

[0092] The output signals 225 and 227 from the I-VGA 218i and the Q-VGA 218q are sent to both the ASK demodulator 222 and the respective ADCs 220i and 220q. Thus, the ASK demodulator 222 and the ADCs 220i and 220q receive the amplified filtered first differential in-phase signal (in output signal 225), the amplified filtered second differential in-phase signal (in output signal 225), the amplified filtered first differential quadrature signal (in output signal 227), and the amplified filtered second differential quadrature signal (in output signal 227). The ASK demodulator 222 demodulates the signals from both the I-VGA 218i and the Q-VGA 218q into I-ch. data 232i and Q-ch. data 232q.

[0093] On the other hand, the ADCs 220i and 220q, which both may be of 10-bit configuration, provide digital outputs 234i and 234q for further processing by digital signal processing (DSP), if desired. Thus, the in-phase analog-to-digital converter ADC 220i converts an analog in-phase signal provided by the I-VGA 218i to the digital in-phase signal 234i. On the other hand, the quadrature analog-to-digital

converter ADC 220q converts an analog quadrature signal provided by the Q-VGA 218q to the digital quadrature signal 234q. It will be appreciated, in the embodiment shown in Figure 2, that the ADCs 220i and 220q are designed, together with the I-CSF 216i and the Q-CSF 216q, to meet the requirements under interference conditions specified in both the FCC and the ETSI standards.

**[0094]** Collectively, the outputs 234i and 232i form the Rx\_data I 120 (also refer Figure 1); while the outputs 234q and 232q form the Rx\_data Q 122 (also refer Figure 1).

**[0095]** The architecture of the receiver path 202 may be easier to integrate compared to using a superheterodyne architecture and achieves a reduction in chip area without the conversion to an intermediate frequency stage. The receiver path 202 architecture converts the modulated RF signals to base band signals directly which means the LO and the RF carrier frequencies are the same. Another advantage is synchronization is not needed between the I and Q branches for ASK demodulation, thus simplifying design of the base-band. The two I and Q branches ensure that there one branch detects the backscatter signal 228b even when there is a phase difference in the backscatter signal 228b carrier frequency and the local oscillator of the RFID transceiver 200 (i.e. the operating frequency of the RFID transceiver 200).

## II) Transmitter path 204

**[0096]** The transmitter path 204 includes a set of I and Q digital-to-analogue converters (DAC) 236i and 236q; a set of tunable I and Q pulse-shaping filters (PSF) 238i (I-PSF) and 238q (Q-PSF); a modulator 240; a pre-amplifier 242 and a power amplifier (PA) 244.

**[0097]** I and Q transmit data 248i and 248q from an external processor (not shown) are sent to their respective I and Q DACs 236i and 236q inputs. The I and Q DACs 236i and 236q outputs are coupled to respective inputs of the I-PSF 238i and

the Q-PSF 238q. The I-PSF 238i and the Q-PSF 238q outputs are coupled to respective inputs of the modulator 240. The modulator 240 output is coupled to the pre-amplifier 242 input, while the pre-amplifier will output the TX\_out signal 126 (also see Figure 1).

**[0098]** In the embodiment shown in Figure 2, the DACs 236i and 236q have 10-bit configurations, where the resolutions of the 10-bit DACs 236i and 236q are selected based on a consideration of system optimization between analog and digital portions. The DAC 236i converts a digital signal 248i to an analog signal 249i to be transmitted, wherein the DAC 236i is coupled to the pulse shaper I-PSF 238i such that the analog signal 249i to be transmitted is supplied to the pulse shaper I-PSF 238i. The DAC 236q converts a digital signal 248q to an analog signal 249q to be transmitted, wherein the DAC 236q is coupled to the pulse shaper I-PSF 238q such that the analog signal 249q to be transmitted is supplied to the pulse shaper I-PSF 238q.

**[0099]** By feeding proper data bits to the respective I and Q DACs 236i and 236q, various modulations schemes, namely double-sideband - amplitude-shift keying (DSB-ASK), phase-reversed ASK (PR-ASK) or single-sideband ASK (SSB-ASK) as desired, by the various communication standard protocols used within the 860MHz to 960MHz RFID band, can be realized.

**[00100]** These standard protocols are, for example, the EPC (Electronic Product Code) Class-1 Generation-2 standard, where there are a multiple-reader mode and a dense-reader mode. Under the EPC Class-1 Generation-2 standard, these two modes specify different transmit spectrum mask and different transmit bandwidth requirement. Similarly, the European standard ETSI EN 302 208-1 specifies another reader mode with a respective transmission spectrum mask and a transmission bandwidth.

**[00101]** For the RFID transceiver 200 to operate within the above standard protocols, the pulse shaping filters I-PSF 238i and Q-PSF 238q are made tunable to reduce the transmission bandwidth so that the baseband waveform spectrum is shaped to fit within the respective transmitting mask specified by the respective standard protocols. In this embodiment shown in Figure 2, the tunable pulse shaping filters I-PSF 238i and Q-PSF 238q are switchable to select three pass bands of 40 KHz, 80 KHz and 160 KHz for 0.5 dB bandwidth. A first attenuation of 30 dB starts at 150 KHz, 300 KHz and 750 KHz respectively. A second attenuation of 65 dB begins at 280 KHz, 560 KHz and 1120 KHz respectively. Further, the I-PSF 238i and the Q-PSF 238q remove spectral spur introduced by the I and Q DACs 236i and 236q. Further details on the architecture of the I-PSF 238i and the Q-PSF 238q are shown in Figure 24.

**[00102]** The modulator 240 adopts an I Q configuration to realize the three modulation schemes, DSB-ASK, PR-ASK and SSB-ASK. For DSB-ASK and PR-ASK, only the I-section of the I-Q modulator 240 is used. For SSB-ASK, both the I and Q sections of the I-Q modulator 240 are needed. The PLL 206 is coupled to the modulator 240 to provide an in-phase radio frequency oscillator signal (I-RF) 250i and a quadrature radio frequency oscillator signal (Q-RF) 250q. The I-RF 250i and the Q-RF 250q signals provide the carrier radio frequency (RF), having a predefined or desired frequency range, for transmission. The signals I-RF 250i and Q-RF 250q are modulated, in the I-Mixer 212i and the Q-Mixer 212q, with the I-PSF 238i and the Q-PSF 238q output signals with the transmission data 248i and 248q.

**[00103]** The modulated carrier signal 252 is amplified by the PA 244 to about +10 dBm. Thus, the transmitter path 204 further includes at least one amplifier to amplify the modulated signal 252 to be transmitted. In the embodiment shown in Figure 2, the PA 244 provides a 10 dBm 1dB compression point output power with a gain control of around 15dB. Further, the transmitter path 204 may further include an attenuator (not shown) to attenuate portions of the modulated signal 252 to be transmitted, wherein the attenuator (not shown) is coupled to the modulator 240 to

receive the modulated signal 252 to be transmitted. The attenuator may be a passive device that operates independently from the PA 244.

**[00104]** To meet ETSI standards, an RFID transceiver should have a sensitivity of around -96dBm or more in the listen mode. Under the ETSI standard, testing to determine whether a signal is present is based on the detection of the presence of the center frequency of a pre-selected channel. However, for detected signals having a power level around the threshold level of about -96dBm, a small DC voltage will also be obtained under direct conversion. The small DC voltage may be submerged in DC offset caused by some LO leakage in the direct conversion architecture, thus making detection of the small DC voltage difficult.

**[00105]** Two test modes, using external software control of the signals I-LO 230i and Q-LO 230q, are used by the RFID transceiver 200 of Figure 2 to detect the presence of a backscatter signal 228b having a power level around the threshold level of about -96dBm. The two test modes are used in the direct conversion architecture.

**[00106]** Referring to Figure 2C in conjunction with Figure 2, the first test mode setting has the data signals I-LO 230i and Q-LO 230q set to the pre-selected channel frequency  $c_n$  when RF scanning is performed, i.e. the transmitter path 204 is switched on and an un-modulated Tx\_out signal 126 is transmitted to verify that the RFID transceiver 200 is operating at the pre-selected channel frequency  $c_n$ . Next, the RFID transceiver 200 is switched off, and then only the receiver path 202 is switched on. The software will set the local oscillator (LO) frequency to adjacent channels having frequency intervals of 200kHz either greater ( $c_{n+1}$ ,  $c_{n+2}$ , ...) or lesser ( $c_{n-1}$ ,  $c_{n-2}$ , ...) than from the pre-selected channel frequency  $c_n$ . The RFID transceiver 200 will continue to cycle through the various adjacent channels ( $c_{n-1}$ ,  $c_{n-2}$ ,  $c_{n+1}$ ,  $c_{n+2}$ ) if no Rx\_in signal 124 having the pre-selected channel frequency  $c_n$  is detected.

**[00107]** In the scenario where the local oscillator frequency is set to either  $c_{n+1}$  (i.e. the offset frequency immediately greater than the pre-selected channel frequency  $c_n$ )

the RFID transceiver 200 will be able to detect the pre-selected channel frequency  $c_n$ , as the pre-selected channel frequency  $c_n$  is only offset by about 200kHz from the local oscillator frequency  $c_{n+1}$ . The local oscillator frequency of the RFID transceiver 200 will then be set to  $c_{n-1}$  (i.e. the offset frequency immediately less than the pre-selected channel frequency  $c_n$ ) to verify that the RFID transceiver 200 still detects the pre-selected channel frequency  $c_n$ . Subsequently, the local oscillator frequency of the RFID transceiver 200 will be set to the pre-selected channel frequency  $c_n$ .

**[00108]** The second test mode setting has the local oscillator frequency set to an offset frequency of the pre-selected channel center frequency  $c_n$ , for example, 100 kHz. At the same time, the transmitter path 204 is transmitting a 100 kHz clock signal 116 from the base band. With SSB modulation, the transmitted Tx\_out signal 126 will contain the pre-selected channel center frequency  $c_n$ . Along the receiver path 202, the down converted signal (i.e. the signal emitted from the I-Mixer 212i and the Q-Mixer 212q) will have a 100 kHz frequency, which is detectable by the RFID transceiver 200. The local oscillator frequency of the RFID transceiver 200 will then be switched to the channel center frequency  $c_n$  for normal operation.

**[00109]** Returning to Figure 2, the RFID transceiver 200 works in half duplex mode. Thus, the DACs 248i and 248q, along with the ADCs 220i and 220q, can share the same interface pins (not shown), making the shared pins bi-directional I/O (input/output) pins. The sharing of pins reduces the pin count by half, and allows for a more compact chip.

### III) Dual loop synthesizer 206

**[00110]** The dual loop synthesizer 206 generates the desired or predefined frequency, which the RFID transceiver 200 is to be operated at, in the form of in-phase and quadrature-phase (Q) components (through the I-RF 250i and Q-RF 250q signals) for feeding to the transmitter path 204 for modulation, and to the receiver path 202 for down-conversion through the signals I-LO 230i and Q-LO 230q.

Further detail on the dual loop synthesizer 206 architecture is provided later with reference to Figure 7.

#### IV) SPI interface/circuit 208

**[00111]** The RFID transceiver 200 communicates with peripheral devices via the SPI interface 208. The SPI interface 208 provides programmability and control of various aspects of the RFID transceiver 200, such as the transmitter path 204 power; frequency setting of the dual loop synthesizer 206; activation/de-activation of the various components in both the transmitter path 204; and the receiver path 202 to conserve power when needed. The SPI interface 208 allows writing control & configuration data into the RFID transceiver 200 via the micro-controller 104 (Figure 1). There are 20 shift registers which are used to fulfill different requirements of control conditions. The SPI circuit 208 may be a digital circuit synthesized from Verilog code.

**[00112]** Different RFID systems, built in accordance with embodiments of the invention, are described under the heading “Other RFID system embodiments”

#### Other RFID system embodiments

**[00113]** Figure 3 shows a block level representation of a RFID (Radio Frequency Identification) system 302 built in accordance to an embodiment of the present invention.

**[00114]** Similar to the RFID system of Figure 1, the RFID system 302 includes a RFID transceiver 300 electrically connected with the microcontroller (MCU) 104. However, the RFID transceiver 300 is connected to antennas 303 and 304 via respective filters 306 and 308. The antenna 303 is used to transmit the signals Tx\_out 126, while the antenna 304 is used to receive backscatter signals 228b from the RFID tag 228, which is sent to the RFID transceiver 300 via the Rx\_in signals 124.

[00115] The RFID transceiver 300 has a similar architecture to the RFID transceiver 200 of Figure 2, thus components having like reference numerals are not further elaborated.

[00116] A receiver 310 receives the Rx\_in signal 124. It will be appreciated that the receiver 310 serves the same functions as the LNA 210, together with the I-Mixer 212i and the Q-Mixer 212q, i.e. the receiver 310 amplifies the Rx\_in signal 124 and subsequently performs down conversion to obtain the in-phase I and the quadrature-phase Q data components from the Rx\_in signal 124. Subsequently, the I and Q data components are either digitized by the I/Q ADC 220i/220q to obtain the digitized I data 234i and Q data 234q; or the I and Q data components undergo ASK/BPSK demodulation to obtain the demodulated I-ch data 232i and the Q-ch data 232q.

[00117] The receiver 310 also sends received signal strength indicator (RSSI) RSSI\_I 354i and RSSI\_Q 354q data signals which provide an indication of the strength of the received signal Rx\_in signal 124. The RSSI\_I 354i and RSSI\_Q 354q data signals are used to control the receiver 310 gain via the LNA control signal 226.

[00118] The local oscillation frequency of the RFID transceiver 300 can also be controlled externally through an external LO 330 to a switch 348. The switch 348 sends an appropriate signal to the modulator 240 so that the transmitted signal Tx\_out data 126 is transmitting at the externally controlled frequency. Further, the switch 348 sends another appropriate signal to the receiver 310 to down convert the received signal Rx\_in 124 at the externally controlled frequency.

[00119] An attenuator 342 is integrated between the modulator 240 and the PA 244. The attenuator 342 is a passive device that operates independently from the PA 244.

[00120] Figure 4 shows a block level representation of a RFID (Radio Frequency Identification) system 402 built in accordance to an embodiment of the present invention.

[00121] The RFID system 402 includes a RFID transceiver 400 electrically connected with the microcontroller (MCU) 104, the transmitter/receiver (Tx/Rx) isolation unit 112 and the filter 110. The filter 110 is also connected with the Tx/Rx isolation unit 112. The antenna 114 is coupled to the Tx/Rx isolation unit 112 to transmit signals (Tx\_out) 126 from the RFID transceiver 400 and to send the received signals Rx\_in 124 to the RFID transceiver 400.

[00122] The RFID transceiver 400 has a similar architecture to the RFID transceiver 300 of Figure 3, thus components having like reference numerals are not further elaborated.

[00123] The LNA 210 receives the Rx\_in signal 124. The amplified Rx\_in signal 124 will be down-converted in the I-Mixer 212i and the Q-Mixer 212q, where the I phase and the Q phase data components from the Rx\_in signal 124 are subsequently amplified by respective amplifiers 414i and 414q and then passed through a filter 424. A pair of capacitors, such as the capacitors 224 of Figure 2 may be used for the filter 424. The output from the VGA 218i and the VGA 218q are either digitized by the ADCs 220i and 220q to obtain the digitized I data 234i and Q data 234q; or undergo ASK demodulation in the respective ASK demodulators 222i and 222q to obtain the demodulated I-ch data 232i and the Q-ch data 232q. Collectively, the outputs 234i and 232i form the Rx\_data I 120 (also refer Figure 1); while the outputs 234q and 232q form the Rx\_data Q 122 (also refer Figure 1).

[00124] Received signal strength indicator (RSSI) circuits 405i and 405q detect the strength of the signal, which is emitted from the I and the Q CSF 216i and 216q, realized in logarithmic form. Both RSSIs 405i and 405q produce respective RSSI\_I 354i and RSSI\_Q 354q data signals, where both the RSSI\_I 354i and the RSSI\_Q

354q data signals are sent to the microcontroller 104, whereupon the microcontroller 104 will change the VGAs 218i and 218q gains to improve the dynamic receive range. Successive detection architecture is adopted for realizing the logarithmic amplifier. It is composed of five stages of limiting amplifier combined with a full-wave rectifier and low pass filter. The limiting amplifier design is the same as the fixed gain amplifier used in VGA.

[00125] The in-phase (I) and the quadrature-phase (Q) data components can also be sent, in the form of analog signals A\_I 448i and A\_Q 448q, to the transmitter path 204. The analog signals A\_I 448i and A\_Q 448q are sent directly to their respective pulse shaping filters I-PSF 238i and Q-PSF 238q as A\_I 448i and A\_Q 448q are already in a form suitable for processing by the pulse shaping filters I-PSF 238i and Q-PSF 238q.

[00126] The RFID transceiver 400 also includes a 0/90 signal generator 446, which generates LO signals in 0 degree phase and 90 degree phase.

[00127] A digital application specific integrated circuit (ASIC) 408 provides a monitor and control interface to the RFID transceiver 400. It will be appreciated that the ASIC 408 is analogous to the SPI 208 of Figure 2, thus the ASIC 408 is not further elaborated. An external base-band (not shown) controls the RFID transceiver by having the microcontroller 104 send control signals SPI 118 to the ASIC 408. The base band is able to control the RFID transceiver 400 to operate in various modes (e.g.: to perform DSB-ASK, PR-ASK or SSB-ASK modulation) or to debug the various components in the RFID transceiver 400. It will be appreciated that to save power, the receiver path 202 and the transmitter path 204 may each be independently switched on/off. Further to save power in the talk mode, the receiver path 202 may be switched on only when the tag 228 starts to send backscatter signals 228b.

[00128] Figures 5 and 6 show block level representations of the RFID (Radio Frequency Identification) system of Figure 4, when the RFID system 402 is used under different operating conditions.

[00129] In Figure 5, the RFID system 402 is used for low-end applications which use low cost microcontrollers running at low MHz clock frequencies, wherein the DACs 236q and 236i (Figure 4); the ADCs 220i and 220q (Figure 4); and the RSSI circuits 405i and 405q are not used. Powering down the DACs 236q and 236i; the ADCs 220i and 220q; and the RSSI circuits 405i and 405q reduces the power consumed by the RFID transceiver 400. Further, as demodulation, performed by the ASK demodulators 222, is within the RFID transceiver 400, a simpler microcontroller 104, such as a 8 bit microcontroller. A capacitor (not shown) may be used for the external filter 424 to achieve AC coupling.

[00130] In Figure 6, the RFID system 402 is used for high-end applications for example long range fix readers, which make use of DSP for: i) base-band data processing; ii) digital filtering at the filter 110 of the transmitted signal Tx\_out 126; iii) I/Q data generation 248i and 248q for both single sideband ASK modulation and phase-reversed ASK modulation in the modulator 240; iv) modulation depth control in the modulator 240; and v) noise filtering in the LNA 210 for receiver to improve sensitivity. The DSP circuitry is located in the microcontroller 104 and base band data processing is performed in the microcontroller 104. In Figure 6, the RSSI circuits 405i and 405q may be used to control the VGAs 218i and 218q gains to improve dynamic receive range. A high pass filter (not shown) or a resonant tank circuit (not shown) may be used for the external filter 424 for dense reader mode.

[00131] The various components of the Dual-loop synthesizer 206 (see Figures 2 to 6) are now described under the heading "Dual-loop synthesizer 206"

### III) Dual-loop synthesizer 206

[00132] Figure 7 shows a block level representation of the architecture of the dual loop PLL 206 of a RFID transceiver (see Figures 2-6) built in accordance to an embodiment of the present invention.

[00133] The operation of the PLL 206 is controlled digitally through the SPI 208 (Figure 2). The PLL 206 ensures that the RFID transceiver (see Figures 2-6) is able to operate with sufficient sensitivity and in spectrum masks complying with, for example, either the FCC (Federal Communications Commission) or the ETSI (European Telecommunications Standards Institute) standards in the UHF frequency range from about 860MHz to about 960MHz, which is the RFID band used in most parts of the world. . The PLL 206 achieves phase-noise with frequency resolution of about 50kHz for the band from about 860 MHz to about 960 MHz.

[00134] The PLL synthesizer 206 uses a dual-loop architecture that includes two integer-N synthesizers 704 and 706, and one single-sideband (SSB) mixer 702. The synthesizer 704 includes a phase frequency detector (PFD) and charge pump 708, a 5-bit programmable counter 710, a 4-bit swallow counter 712, a prescaler-8/9 714, a voltage-control oscillator (VCO1) 716 and uses the clock signal 128 (compare Figure 1) from the crystal oscillator 106 (Figure 1) as a reference, to achieve lower in-band phase-noise. In the embodiment shown in Figure 7, the crystal oscillator 106 operates at 20MHz. The output frequency  $f_{VCO1}$  from the VCO1 716 can be obtained as follows:

$$f_{VCO1} = (8 \times P_1 + S_1) \times 20MHz$$

where P1 and S1 are the values of the programmable counter 710 and the swallow counter 712 respectively. The frequency range for the synthesizer 704 is from about 2060MHz to about 2260MHz.

[00135] The synthesizer 706 includes a PFD and charge pump 720, a 7-bit programmable counter 722, a 5-bit swallow counter 724, a prescaler-32/33 726, a voltage-control oscillator (VCO2) 728, and uses a reference frequency of about 800KHz. The reference frequency for the synthesizer 706 is derived by dividing the

20 MHz clock signal 128 reference by 25 (see reference numeral 732). Similarly, the output frequency  $f_{VCO2}$  from the VCO2 716 can be obtained as follows:

$$f_{VCO2} = (32 \times P_2 + S_2) \times 800 \text{ KHz}$$

where P2 and S2 are the values of the programmable counter 722 and the swallow counter 724 respectively. The frequency range for the synthesizer 706 is from about 2400MHz to about 2560MHz.

**[00136]** There are eight selectable VCO bands for the VCO1 716 and the VCO2 728, so that the phase-noise does not change over the frequency range of between about 860 to about 960 MHz.

**[00137]** The synthesizer 704 output signal 734 frequency is divided by 2 (at a frequency divider 718) and the synthesizer 706 output signal 736 frequency is divided by 16 (at a frequency divider 730) before being fed to the SSB mixer 702. The frequency division provides, for the synthesizer 704, phase noise improvement of about 6dB. Further, as the VCO1 716 can be tuned from about 2020MHz to about 2220MHz, frequency division makes available a quadrature-phase frequency of about 1010MHz to about 1110MHz for the synthesizer 704. Similarly, the frequency division provides, for the synthesizer 706, phase noise improvement of about 24dB. Further, as the VCO2 728 can be tuned from about 2400MHz to about 2560MHz, frequency division makes available a quadrature-phase frequency of about 150MHz to about 160MHz for the synthesizer 706.,

**[00138]** The frequency dividers 718 and 730 are based on conventional current-mode logic (CML) which is realized using two high-speed D flip-flops connected back-to-back. The frequency dividers 718 and 730 generate differential quadrature I and Q signals for the single-sideband (SSB) mixer 702.

**[00139]** After mixing the divided outputs 734 and 736 (respectively from the synthesizer 704 and the synthesizer 706) in the SSB mixer, low phase noise and a

lower side-band signal from about 860MHz to about 960MHz with a frequency resolution of about 50 KHz is obtained, as the SSB mixer 702 is designed to reject upper-sideband frequencies from about 1160 MHz to about 1270 MHz. The higher band frequency signals can be further suppressed by the modulator 240 (Figure 2) and PA 244 (Figure 2) as both the modulator 240 and the PA 244 are, in the embodiment shown in Figure 2, tuned for the frequency band from about 860MHz to about 960MHz. Thus the output frequency,  $f_{out}$ , that can be generated from the SSB mixer 702 is based on the following equation:

$$f_{out} = \frac{f_{vco1}}{2} - \frac{f_{vco2}}{16}$$

[00140] 3-stage polyphase filters and buffers 738 provide the filtered and buffered differential I and Q signals, I-LO 212i, Q-LO 212q, I-RF 250i and I-RF 250q, where I-RF 250i and I-RF 250q are fed to the modulator 240 (Figure 2), while I-LO 212i and Q-LO 212q are respectively fed to the I-Mixer 212i and the Q-Mixer 212q.

[00141] A true single-phase clock (TSPC) prescaler-8/9 is used for synthesizer 704. The prescaler consists of a divide-by-4/5 synchronous counter and a divide-by-2 asynchronous counter, in combination with 5-bit programmable counter and 4-bit swallow counter. For Synthesizer-II prescaler-32/33, a conventional 7-bit programmable counter and a conventional 5-bit swallow counter are used.

[00142] Turning to the two LC-tank VCO1 716 and VCO2 728, since the PLL synthesizer 206 covers a wider bandwidth, it is desirable to use complementary NMOS and PMOS transistors to realize the VCO1 716 and the VCO2 728, so as to get a more linear tuning curve (see Figure 9) and thus achieve consistent performance over the operating frequency band of from about 860 MHz to about 960 MHz.

III)a) Voltage Controlled Oscillator 716

[00143] Figure 8 shows a schematic diagram of circuitry that can be used to implement the voltage-controlled oscillator VCO1 716 (Figure 7) and the voltage-controlled oscillator VCO2 728 (Figure 7) both used in the PLL synthesizer 206 of an RFID transceiver (see Figures 2-6) built in accordance with an embodiment of the invention.

[00144] The VCO 716/728 includes four transistors, namely two PMOS transistors 812 and 814 and two NMOS transistors 816 and 818. Two inductors 802 and 804, connected in series, are further connected between the drain terminal 816<sub>D</sub> of the NMOS transistor 816 and the drain terminal 818<sub>D</sub> of the NMOS transistor 818. The quality factor (Q value) of the inductors 802 and 804, for the embodiment shown in Figure 8, is about 5. The gate terminal 816<sub>G</sub> of the NMOS transistor 816 is connected to the drain terminal 818<sub>D</sub> of the transistor 818 while the gate terminal 818<sub>G</sub> of the NMOS transistor 818 is connected to the drain terminal 816<sub>D</sub> of the NMOS transistor 816. A series of voltage tunable capacitors or varactors, namely 824, 822, 820 and 826 are connected between the respective drain terminals 816<sub>D</sub> and 812<sub>D</sub> of NMOS transistor 816 and PMOS transistor 812. The same tuneable capacitors or varactors 824, 822, 820 and 826 are also connected between the respective drain terminals 818<sub>D</sub> and 814<sub>D</sub> of NMOS transistor 818 and PMOS transistor 814. Each varactor is controlled by a respective input voltage signal, where input voltage signals Va, Vb, Vc and a control voltage 806 respectively control varactors 824, 822, 820 and 826. The input signal voltages Va, Vb and Vc are respectively connected to the varactors 824, 822 and 820 via an inverter. A biasing current source I<sub>bias</sub> 808 is connected to the respective source terminals 812<sub>S</sub> and 814<sub>S</sub> of the PMOS transistors 812 and 814. The source terminals 812<sub>S</sub> and 814<sub>S</sub> are also connected to a ground potential via an external capacitor 810.

[00145] To get low phase-noise, the biasing current I<sub>bias</sub> 808 is about 12 mA. The external capacitor 810 is connected to current source I<sub>bias</sub> 808 to bypass flicker noise.

[00146] Varactors 824, 822 and 820 are binary-coded accumulation-mode MOS varactors, each having a 2 value capacitance, namely a bigger value or a smaller value. The control voltage 806, which is emitted from the PLL 206 (Figure 2), sets the chosen frequency. Input signal voltages  $V_a$ ,  $V_b$  and  $V_c$  act as digital control voltages that change the VCO 716/728 bands, thereby changing the VCO1 716 (Figure 7) operating band and the VCO2 728 (Figure 7) operating band. The accumulator-mode MOS varactors 824, 822 and 820 are also used for frequency tuning, and allow for a tuning sensitivity of 80MHz/V to be obtainable for VCO1 716 (Figure 7). The input voltages,  $V_a$ ,  $V_b$  and  $V_c$ , in conjunction with (and explained later with reference to Figure 9) the varactors 824, 822 and 820, allow for the VCO1 716 (Figure 7) to have eight frequency bands (see Figure 9), each band being selected by applying appropriate voltage logic for  $V_a$ ,  $V_b$  and  $V_c$ .

[00147] Similarly, the VCO 716/728 allows for the VCO2 728 (Figure 7) to have four bands, and a tuning sensitivity smaller than 150 MHz/V. For VCO2 728, only 2mA bias current is used.

[00148] Spiral inductors used in CMOS IC design suffer from dissipative mechanisms beyond simple conductor loss. One way to improve the phase noise is to improve the quality factor  $Q$  of the inductors 802 and 804 used. Another way to obtain good phase-noise, is to reduce the tuning sensitivity, which can be done by using multiple-bands for the VCO 716/728.

[00149] It has been found that between VCO1 716 and VCO2 728 (Figure 7), VCO1 has a greater contribution to the phase noise of the output signal from the SSB mixer 702 (Figure 7). Thus, emphasis is placed on reducing the tuning sensitivity of the VCO1.

[00150] Figure 9 shows tuning curves 902, 905, 906, 908, 910, 912, 914 and 918 for all eight bands of an 8-band voltage-controlled oscillator VCO1 used in a RFID

transceiver (see Figures 2-6) built in accordance with an embodiment of the invention.

[00151] A corresponding one of the eight bands of the VCO1 716 (Figure 7) will be selected for each respective logic sequence 916 for Va, Vb and Vc. For instance, when  $V_a = 0$ ,  $V_b = 0$  and  $V_c = 0$ , the tuning curve 902 will be obtained as the tuning voltage is varied from 0 to 1.8V.

### III)b) Phase Frequency Detector (PFD) and Charge Pump 708

[00152] Figure 10 shows a schematic diagram of a charge-pump circuit 1000 of the phase frequency detector (PFD) and charge pump 708 block used in the PLL synthesizer 206 of an RFID transceiver (see Figures 2-6) built in accordance with an embodiment of the invention.

[00153] The charge pump circuit 1000 includes a plurality of transistors, namely three NMOS transistors, 1002, 1006 and 1010 and two PMOS transistors, 1004 and 1008. The charge pump circuit 1000 further includes an amplifier A1 and a block 1012.

[00154] The source terminals of the NMOS transistors 1002, 1006 and 1010 respectively are connected to a ground potential. A biasing current source I<sub>bias</sub> 1014 supplies current to the gate terminals of the NMOS transistors 1002, 1006 and 1010. The drain terminal and the gate terminal of the NMOS transistor 1002 are connected. The drain terminals of the NMOS transistor 1006 and the PMOS transistors 1004 are connected to an inverting terminal A<sub>1</sub> of the amplifier A1. The drain terminal of the NMOS transistor 1010 is connected to the block 1012. The output from the block 1012 is connected to the non-inverting terminal A<sub>1+</sub> of the amplifier A1. The output terminal of the amplifier A1 is connected to the gate terminals of the PMOS transistors 1004 and 1008. The source terminals of the PMOS transistors 1004 and 1008 are connected to a reference potential. The drain terminal of the PMOS transistor 1008 is connected to the block 1012.

[00155] The block 1012 includes an amplifier A2 and four complementary switches or transmission gates 1016, 1018, 1020 and 1022. Each transmission gate 1016, 1018, 1020 and 1022 is a parallel combination of an NMOS transistor coupled to a PMOS transistor with the input at the gate terminal of either the NMOS or the PMOS transistors being complementary to the input at the gate terminal of the other transistor. Taking the transmission gate 1018 as an example, the input at the NMOS transistor is UP, while the input at the PMOS transistor is  $\overline{UP}$ . Similarly, and taking the transmission gate 1020 as an example, the input at the NMOS transistor is  $\overline{DN}$ , while the input at the PMOS transistor is DN.

[00156] Each of the transmission gates 1016, 1018, 1020 and 1022 has a respective input (1016i, 1018i, 1020i and 1022i) and a respective output (1016o, 1018o, 1020o and 1022o). The input terminals 1016i and 1018i of the transmission gates 1016 and 1018 are both connected to the drain terminal of the PMOS transistor 1008. The output terminal 1016o of the transmission gate 1016 is connected to the input terminal 1020i of the transmission gate 1020. The output terminal 1018o of the transmission gate 1018 is connected to the input terminal 1022i of the transmission gate 1022. The output terminal 1016o of the transmission gate 1016 and the input terminal 1020i of the transmission gate 1020 are connected to the output terminal A2o of the amplifier A2. The output 1018o of the transmission gate 1018 and the input terminal 1022i of the transmission gate 1022 are connected to the non-inverting terminal A2+ of the amplifier A2. The inverting terminal A2- of the amplifier A2 is connected to the output terminal A2o of the amplifier A2. The output terminals 1020o and 1022o of the transmission gates 1020 and 1022 are both connected to the drain terminal of the NMOS transistor 1010.

[00157] A current can flow through the transmission gates 1016, 1018, 1020 and 1022 in either direction, i.e from the respective inputs 1016i, 1018i, 1020i and 1022i of the transmission gates 1016, 1018, 1020 and 1022 to the respective outputs 1016o, 1018o, 1020o and 1022o of the transmission gates 1016, 1018, 1020 and 1022; and

similarly from the respective outputs 1016o, 1018o, 1020o and 1022o of the transmission gates 1016, 1018, 1020 and 1022 to the respective inputs 1016i, 1018i, 1020i and 1022i. Depending on whether there is a voltage on the gate terminals of the transmission gates 1016, 1018, 1020 and 1022, the connection between the respective inputs 1016i, 1018i, 1020i and 1022i and the respective outputs 1016o, 1018o, 1020o and 1022o of the transmission gates 1016, 1018, 1020 and 1022 is either low-resistance or high-resistance, respectively. The operation of any of the transmission gates 1016, 1018, 1020 and 1022 is as such: when the gate input to the NMOS transistor is '0', a complementary '1' will be input to the PMOS transistor gate, thereby turning off both transistors. However when the gate input to the NMOS is '1', a complementary '0' will be input to the PMOS transistor gate, thereby both transistors are turned on and passes any signal '1' or '0' equally well without degradation. The use of the transmission gates 1016, 1018, 1020 and 1022 reduces undesirable threshold voltage effects which give rise to loss of logic levels in pass transistors.

### III)c) SSB Mixer 702

[00158] Figure 11 shows a schematic diagram of the single sideband (SSB) mixer 702 used in the PLL synthesizer 206 of an RFID transceiver (see Figures 2-6) built in accordance with an embodiment of the invention.

[00159] The SSB mixer 702 includes two Gilbert-cell mixers 1102 and 1104.

[00160] The Gilbert-cell mixer 1102 includes a plurality of NMOS transistors 1106, 1108, 1110, 1112, 1114 and 1116; an inductor 1140; a capacitor 1146 and a current source Ib1 1118.

[00161] Similarly, the Gilbert-cell mixer 1104 includes a plurality of NMOS transistors 1126, 1128, 1130, 1132, 1134 and 1136; an inductor 1142; a capacitor 1148 and a current source Ib2 1138.

[00162] The drain terminals of the transistors 1106, 1110, 1126 and 1130 are connected together to form an Out<sub>+</sub> terminal of the SSB mixer 702. The drain terminals of the transistors 1108, 1112, 1128 and 1132 are connected together to form an Out<sub>-</sub> terminal of the SSB mixer 702. Collectively, the Out<sub>+</sub> terminal and the Out<sub>-</sub> terminal form the output 1150 of the SSB mixer 702, where the outputs from both the mixers 1104 and 1106 are either added or subtracted from each other.

[00163] One terminal of the capacitor 1146 is connected to the Out<sub>+</sub> terminal, while the other terminal of the capacitor 1146 is connected to a reference voltage 1152. The inductor 1140 is connected in parallel with the capacitor 1146. Similarly, one terminal of the capacitor 1148 is connected to the Out<sub>-</sub> terminal, while the other terminal of the capacitor 1148 is connected to a reference voltage 1152. The inductor 1142 is connected in parallel with the capacitor 1148.

[00164] Turning to the Gilbert-cell mixer 1102, the gate terminals of the transistors 1108 and 1110 are connected together. The source terminals of the transistors 1106 and 1108 are both connected to the drain terminal of the transistor 1114. The source terminals of the transistors 1110 and 1112 are both connected to the drain terminal of the transistor 1116. The source terminals of the transistors 1114 and 1116 are both connected to Ib1 1118.

[00165] Similarly, in the Gilbert-cell mixer 1104, the gate terminals of the transistors 1128 and 1130 are connected together. The source terminals of the transistors 1126 and 1128 are both connected to the drain terminal of the transistor 1134. The source terminals of the transistors 1130 and 1132 are both connected to the drain terminal of the transistor 1136. The source terminals of the transistors 1134 and 1136 are both connected to Ib2 1138.

[00166] The I and Q signals from the frequency divider 718 (Figure 7), which have frequencies from about 1010 to about 1110MHz, act as local oscillator input in the form of f1\_0, f1\_90, f1\_180 and f1\_270 signals. The f1\_0 signal is sent to both the

gate terminals of the transistors 1106 and 1112, while the f1\_90 signal is sent to both the gate terminals of the transistors 1128 and 1130. The f1\_180 signal is sent to both the gate terminals of the transistors 1108 and 1110, while the f1\_270 signal is sent to both the gate terminals of the transistors 1126 and 1132.

[00167] The other I and Q signals from the frequency divider 730 (Figure 7), which have frequencies from about 150 to about 160MHz are in the form of f2\_0, f2\_90, f2\_180 and f2\_270 signals. The f2\_0 signal is sent to the gate terminal of the transistor 1114, while the f2\_90 signal is sent to the gate terminal of the transistor 1134. The f2\_180 signal is sent to the gate terminal of the transistor 1116, while the f1\_270 signal is sent to the gate terminal of the transistor 1136. Care is taken in layout to reduce amplitude and phase mismatches.

[00168] Lower sideband signals of frequency from about 860 to about 960MHz are generated at the output 1150 of the SSB mixer 702. Suppressed upper-sideband signals are also generated at the output. Referring to Figure 12, the upper-sideband signal 1202 may be suppressed 1204 by more than 35dB. Figure 12 illustrates image rejection of the SSB mixer 702 (Figure 7).

[00169] Further detail on the other components of the RFID transceiver (see Figures 2-6) are provided in the preceding paragraphs.

#### I) Receiver path 202

[00170] Figure 13A shows a block level representation of the architecture of the receiver path 202 of a RFID transceiver (see Figures 2-6) built in accordance to an embodiment of the present invention.

[00171] The receiver path 202 includes two stage gain control. The first stage is controlled from gain control 1 unit 1306a and the second stage is controlled from gain control 2 unit 1306b. The gain control units 1306a and 1306b generate digital control signals to VGA/Filter 214 from the digital ASIC 408.

[00172] Figure 13B shows a block level representation of another architecture of a receiver path 1302 of a RFID transceiver (see Figures 2-6) built in accordance to an embodiment of the present invention.

[00173] The receiver path 1302 shown in Figure 13B uses components, such as the demodulator 232i/232q and the 10-bit ADC 220i/220q and the VGA 218i/218q shown in Figure 2, thus like reference numerals are not further elaborated.

[00174] A VGA/Filter block 1350 provides about 12dB of gain through a pre amplifier 1340. The pre-amplifier 1340 receives an input signal 1324 and sends the amplified signal to a low pass filter (LPF) 1310. The LPF 1310 is controlled by a listen before talk (LBT) signal 1352. A received signal strength indicator (RSSI) circuit 1342 monitors for the presence of the input signal 124. The output of the RSSI 1342 then determines whether the VGA/Filter block 1350 gain is to be set lower or higher.

[00175] Figure 13C shows a block level representation of a preamplifier stage 1370 of a RFID transceiver (see Figures 2-6) built in accordance to an embodiment of the present invention. It will be appreciated that the preamplifier 1340 employed in Figure 13B, can be replaced with the preamplifier stage 1370 arrangement of Figure 13C.

[00176] The preamplifier stage 1370 includes a fixed gain amplifier 1372, an adder 1374, a gm cell 1376 and capacitors 1378. The fixed gain amplifier provides a 12 dB gain to the input signal 124 to raise the overall gain from 48 dB to 60 dB as well as to improve the noise figure of the RFID transceiver (see Figures 2 to 6). To cancel DC offset, the gm cell 1376, along with the capacitors 1278, provide a gm-C filter arrangement that acts as a simple low pass filter that feeds back the output DC offset to the adder 1374 to subtract the DC components in the input signal 124. The gm-C filter provides high gain to the cancellation loop while consuming a small

current in the  $\mu\text{A}$  range. The fixed gain amplifier 1372 may be designed based on a differential pair arrangement with diode connected loads, as shown in Figure 8.

D)a) Receiver path front end

[00177] Figure 14 shows a block level representation of the architecture of a receiver path front-end 1400 of a RFID transceiver (see Figures 2-6) built in accordance to an embodiment of the present invention.

[00178] The signals I-LO 230i and Q-LO 230q, which are both from the PLL 206 (Figure 2), pass through an I-Buffer 1404i and a Q-Buffer 1404q respectively before the data signals I-LO 230i and Q-LO 230q are sent to the I-Mixer 212i and the Q-Mixer 212q. The I-Mixer 212i and the Q-Mixer 212q outputs are coupled to I-IF amplifier 1414i and a Q-IF amplifier 1414q inputs respectively. The receiver path front-end 1400 also includes a bias circuit 1402.

[00179] The bias circuit 1402 provides a current that is proportional to absolute temperature (PTAT) current and bias voltages to the receiver path front-end 1400. The IF buffer at the output of the passive mixers is designed to be linear. The I-IF amplifier 1414i and the Q-IF amplifier 1414q act as IF buffers whose outputs are ac-coupled to the inputs of the I-Amp 214i (Figure 2) and the Q-Amp 214q (Figure 2), where in this embodiment of the invention, the I-Amp 214i and the Q-Amp 214q both have a gain of about 12db each.

[00180] To achieve a listen-before-talk sensitivity of better than about -96dBm and talk-mode sensitivity of better than about -85dBm, a +12dB switchable attenuator 806 is provided before the LNA 210.

D)a)i) LNA 210

[00181] Figure 15 shows a schematic diagram of the LNA 210 of a RFID transceiver (see Figures 2-6) built in accordance to an embodiment of the present invention.

[00182] As mentioned above, the LNA 210 can operate in a high gain mode or a low gain mode depending on the different operation modes of the RFID transceiver 200.

[00183] The LNA 210 has two stages. The first stage 210a (also see Figure 8) is a gain stage which uses single-ended cascode topology, while the second stage 210b (also see Figure 8) is an active single-to-differential (S-to-D) stage which does not provide any gain, but provides differential outputs 1502 which are fed to the double-balanced I and Q channel passive mixers 212i and 212q (Figure 8) as RF inputs. The first stage 210a of the LNA 210 achieves good isolation between output 1502 and input 1510. The input impedance matching is solved through the use of inductive degeneration in series with the source terminal 1504s of MOSFET (Metal Oxide Semiconductor Field Effect Transistor) 1504; inductors Lg1 and Lg2 in series with the gate 1504g; and a 1pF capacitor C3 between the gate 1504g and the source 1504s. The inductance required at the input of the cascode stage 210a is about 24nH, which is realized by putting two inductors Lg1 and Lg2, each rated about 12nH, in series.

[00184] The single-to-differential stage 210b is designed with unity gain, instead of a transformer gain, to keep the overall noise figure of the LNA 210 low. Flicker noise dominates the noise figure of direct-conversion receivers. To minimize such flicker noise, passive mixers are used for the I-Mixer 212i and the Q-Mixer 212q, instead of active mixers. Compared with active mixers, passive mixers achieve better linearity, consume less power and occupy a smaller area.

[00185] Figure 16 shows a block level representation of the structure and configuration of the LNA 210 (Figure 2) in the receiver path 202 (Figure 2) of a RFID transceiver (see Figures 2-6) built in accordance to an embodiment of the present invention.

[00186] Figure 16 also illustrates that, in the default logic level '0' mode, the LNA 210 operates to provide a high gain in the listen mode. When the switch changes to logic level '1', the LNA 210 will operate in talk mode and provide a low gain.

D)a)ii) I-Mixer and Q-Mixer

[00187] Figure 17 shows a schematic diagram of a down-conversion mixer 1700, which can be used to realize the I-Mixer 212i and the Q-Mixer 212q of a RFID transceiver (see Figures 2-6) built in accordance to an embodiment of the present invention.

[00188] The down conversion mixer 1700 includes four NMOS transistors 1702, 1704, 1706 and 1708; and a capacitor CL.

[00189] The source terminals of the transistors 1702 and 1708 are connected together to a RF\_P terminal, while the source terminals of the transistors 1704 and 1706 are connected together to a RF\_M terminal. The drain terminals of the transistors 1708 and 1706 are connected together to a BB\_P terminal, while the drain terminals of the transistors 1702 and 1704 are connected together to a BB\_M terminal. The capacitor CL is connected between the BB\_P and the BB\_M terminal. The gate terminals of the four transistors 1702, 1704, 1706 and 1708 are connected to terminals LO\_M, LO\_P, LO\_P and LO\_M respectively. RF\_P and RF\_M are input terminals, while BB\_P and BB\_M are base band output signals.

I)b) Channel Select Filter And Variable Gain Amplifier (VGA)

I)b)i) Channel Select Filter (CSF) 216i/216q

[00190] Figure 18A shows a block level representation of the channel select filter (CSF) 216i/216q of a RFID transceiver (see Figures 2-6) built in accordance to an embodiment of the present invention. Figure 18B shows frequency characteristics of the CSF 216i/216q.

[00191] From Figure 18B, it will be observed that the pass-band frequency 1802 of the CSF 216i/216q is tunable to be about 320kHz or to be about 1.5MHz. The operating frequency of the CSF 216i/216q. A filter select signal 1806, operating in line with table 1804, determines which pass-band frequency 1802 is selected. At select '0', the filter select signal 1806 configures the CSF 216i/216q to work in the listen mode and at the frequency 320kHz; while at select '1', the filter select signal 1806 configures the CSF 216i/216q to work in the listen mode and at the frequency 320kHz.

[00192] Figure 19 shows a schematic diagram of the channel select filter (CSF) 216i/216q in the receiver path 202 (Figure 2) of a RFID transceiver (see Figures 2-6) built in accordance with an embodiment of the invention.

[00193] To obtain less sensitivity to the inherent variations in the CMOS IC fabrication process, the CSF 216i/216q is a LPF designed using ladder filter architecture with an integrator based approach as shown in Fig. 19.

[00194] The CSF 216i/216q includes three first amplifier blocks 1902a, 1902b and 1902c; four second amplifier blocks 1904a, 1904b, 1904c and 1904d; and switches 1906, 1908, 1910 and 1912. Using the first amplifier block 1902a as an example, each first amplifier block (1902a, 1902b and 1902c) includes a first amplifier 1922; resistors 1914r, 1916r, 1918r1, 1918r2, 1920r1 and 1920r2; and capacitors 1914c and 1916c. The resistor 1914r and the capacitor 1914c are connected in parallel between the negative output terminal of the first amplifier 1922 and the non-inverting input of the first amplifier 1922. The resistor 1916r and the capacitor 1916c are connected in parallel between the positive output terminal of the first amplifier 1922 and the inverting input of the first amplifier 1922. One end of the resistors 1918r1 and 1918r2 is each connected in parallel to the non-inverting input of the first amplifier 1922, while the other end of the resistors 1918r1 and 1918r2 is each connected to different terminals, as shown in Figure 19, within the CSF 216i/216q. For example, the other end of the resistor 1918r1 is connected to the

IN\_P terminal, while the other end of the resistor 1918r2 is connected to the negative output terminal of the second amplifier of the second amplifier block 1904a and the inverting input of the second amplifier of the second amplifier block 1904b via a respective resistor. One end of the resistors 1920r1 and 1920r2 is each connected in parallel to the non-inverting input of the first amplifier 1922, while the other end of the resistors 1920r1 and 1920r2 is each connected to different terminals as shown in Figure 19, within the CSF 216i/216q. The positive and the negative outputs of the first amplifier 1922 are connected to different terminals, as shown in Figure 19, within the CSF 216i/216q.

**[00195]** Using the second amplifier block 1904a as an example, each second amplifier block (1904a, 1904b, 1904c and 1904d) includes a second amplifier 1932; resistors 1928r1, 1928r2, 1930r1 and 1930r2; and capacitors 1924 and 1926. The capacitor 1924 is connected in parallel between the negative output terminal of the second amplifier 1932 and the non-inverting input of the second amplifier 1932. The capacitor 1926 is connected in parallel between the positive output terminal of the second amplifier 1932 and the inverting input of the second amplifier 1932. One end of the resistors 1928r1 and 1928r2 is each connected in parallel to the non-inverting input of the second amplifier 1932, while the other end of the resistors 1928r1 and 1928r2 is each connected to different terminals, as shown in Figure 19, within the CSF 216i/216q. For example, the other end of the resistor 1928r1 is connected to the positive terminal of the first amplifier 1922, while the other end of the resistor 1928r2 is connected to the positive output terminal of the second amplifier of the second amplifier block 1904b and the inverting input of the first amplifier of the first amplifier block 1902b via a respective resistor. One end of the resistors 1932r1 and 1932r2 is each connected in parallel to the non-inverting input of the second amplifier 1932, while the other end of the resistors 1932r1 and 1932r2 are connected to different terminals, as shown in Figure 19, within the CSF 216i/216q. The positive and the negative outputs of the second amplifier 1932 are connected to different terminals, as shown in Figure 19, within the CSF 216i/216q.

[00196] The output of the first amplifier block 1902a is connected to the input of the second amplifier block 1904a, while the input of the first amplifier block 1902a is connected to both the output of the second amplifier block 1904a and the input of the second amplifier block 1904b. The input of the second amplifier block 1904a is also connected to the input of the first amplifier block 1902b and the output of the second amplifier block 1904b. The input of the second amplifier block 1904b is also connected to the switch 1912 and the output of the first amplifier block 1902b. The input of the first amplifier block 1902b is also connected to the switch 1910, while the output of the second amplifier block 1902b is connected to the switch 1908.

[00197] The output of the first amplifier block 1902c is connected to the input of the second amplifier block 1904d, while the input of the first amplifier block 1902c is connected to the output of the second amplifier block 1904d, the input of the second amplifier block 1904c, and the switch 1906. The input of the second amplifier block 1904d is also connected to the switch 1910 and the output of the second amplifier block 1904c. The input of the second amplifier block 1904c is also connected to the switch 1912 and the output of the block second amplifier 1904d.

[00198] The pole locations of the CSF 216i/216q are chosen to implement a Chebyshev transfer function with 0.5 dB passband ripple and to provide attenuation at the selected operating frequencies. The order of the filter CSF 216i/216q can switch between fourth order for 1.53 MHz cutoff frequency and seventh order for 331 kHz cutoff frequency. This serves to adapt to the talk mode (TM) and listen-before-talk (LBT) mode respectively. The CSF 216i/216q topology is fully differential for good linearity and for good power supply rejection.

#### I)b)ii)Variable Gain Amplifier (VGA)

[00199] Figure 20 shows a block level representation of the variable gain amplifier (VGA) 218i/218q in the receiver path 202 (Figure 2) of a RFID transceiver (see Figures 2-6) built in accordance with an embodiment of the invention.

[00200] The VGA 218i/218q provides gain varying from 0dB to 48dB in 1dB gain step intervals. The VGA 218i/218q has a coarse gain stage 2006, which is controlled by a coarse gain control signal 2002 and a fine gain stage 2008, which is controlled by a fine gain control signal 2004. For example, at a logic sequence 2010 of “001”, the coarse gain stage 2006 will provide a gain of 8dB, while at a logic sequence 2012 of “001”, the fine gain stage 2006 will provide a gain of 1dB.

[00201] Figure 21 shows a schematic diagram of the variable gain amplifier (VGA) 218i/218q in the receiver path 202 (Figure 2) of a RFID transceiver (see Figures 2-6) built in accordance with an embodiment of the invention.

[00202] The coarse gain stage 2006 consists of five fixed gain amplifiers 2102a, 2102b, 2102c, 2102d and 2102e, each of them having a respective switch 2104a, 2104b, 2104c, 2104d and 2104e.

[00203] The fine gain stage 2008 is realized by an amplifier 2112 employing variable resistor 2114a feedback configuration respectively between the OUT\_N terminal of the amplifier 2112 and the non-inverting input terminal of the amplifier 2112. Another variable resistor 2114b is connected between the OUT\_P terminal of the amplifier 2112 and the inverting input terminal of the amplifier 2112. By controlling the ratio of the feedback resistors 2114a and 2114b via the fine gain control signal 2004 (see Figure 20), the gain can be adjusted in 1dB step over a 8dB gain range. A Gm-C cell (not shown) and an adder circuit (not shown) are used as the feedback circuit to cancel the DC offset. One end of a resistor 2116a is connected to the non-inverting input terminal of the amplifier 2112, while the other end of the resistor 2116a is coupled to an IN\_P terminal. One end of a resistor 2116b is connected to the inverting input terminal of the amplifier 2112, while the other end of the resistor 2116b is coupled to an IN\_N terminal.

[00204] The IN\_P terminal of the VGA 218i/218q coincides with the non-inverting input of the amplifier 2102a, while the input IN\_N terminal of the VGA 218i/218q coincides with the inverting input of the amplifier 2102a. The IN\_P terminal is also coupled to the OUT\_P terminal of the CSF 216i/216q (Figure 19), while the IN\_N terminal is also coupled to the OUT\_N terminal of the CSF 216i/216q (Figure 19). In addition, the IN\_P terminal is coupled to the negative output terminals of the amplifiers 2102a, 2102b, 2102c, 2102d and 2102e, while the IN\_N terminal is coupled to the positive output terminals of the amplifiers 2102a, 2102b, 2102c, 2102d and 2102e. The negative output terminal of the amplifier 2102a is connected to the non-inverting input of the amplifier 2102b, while the positive output terminal of the amplifier 2102a is connected to the inverting input of the amplifier 2102b.

[00205] It will be appreciated that the amplifiers 2102b to 2102e are cascaded in a similar fashion as how the amplifier 2102a is cascaded with the amplifier 2102b, with the exception that the output terminals of the amplifier 2102e terminate at the respective switch 2104e.

[00206] The gain of the coarse gain stage 2006 can be adjusted in steps of 8dB, over a 40dB gain range, by the coarse gain control signal 2002 closing the desired switches 2104a, 2104b, 2104c, 2104d and 2104e, whereby the output from the selected amplifiers 2102a, 2102b, 2102c, 2102d and 2102e are sent to the fine gain stage 2008 for further amplification, if necessary.

[00207] The fixed gain amplifiers 2102a, 2102b, 2102c, 2102d, 2102e and 2112 may each be a simple source coupled pair arrangement (not shown) with a diode connected load (not shown).

#### I)c) ASK Demodulator 222

[00208] The ASK modulated signal when directly down converted to Zero IF (which means LO signal is at the same frequency of the RF carrier) will be a square wave irrespective of the modulation depth. The amplitude of the square

waveform depends on the modulation depth. Since the modulation depth can vary from 10% to 100%, the amplitude for which the demodulator has to work varies from 0.05 V(p-p) to 2 V (p-p). Hence, a high swing comparator (not shown) is used for demodulating the ASK modulated signal. Thus, the ASK demodulator 222 is optimized to work from 10% ~ 100% ASK signals.

#### I)d) ADCs 220i/220q

[00209] The 10-bit ADCs 220i/220q use pipe-lined architectures to obtain a analogue to digital conversion rate of around 10Mps

#### II) Transmitter path 204

##### Pulse-Shaping Filter (PSF) 238i/238q

[00210] Figure 22 shows a block level representation of the pulse-shaping filter (PSF) 238i/238q in the transmitter path 204 (Figure 2) of a RFID transceiver (see Figures 2-6) built in accordance with an embodiment of the invention.

[00211] The PSF 238i/238q includes an input level shifter 2202 which receives an input signal which is emitted by the respective DACs 236i and 236q (see Figure 2). The input level shifter 2202 is coupled to a second order Chebyshev stage filter 2204, which is in turn coupled to another second order Chebyshev stage filter 2206. The another second order Chebyshev stage filter 2206 is coupled to a first order Butterworth stage filter 2208. Finally, an output level shifter 2210 is coupled to the first order Butterworth stage filter 2208 where the output level shifter 2210 output is sent to the modulator 240 (see Figure 2) input.

[00212] Figure 23A shows a block level representation of the pulse-shaping filter (PSF) 238i/238q in the transmitter path 204 (Figure 2) of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention. Figure 23B shows frequency characteristics of the pulse-shaping filter PSF 238i/238q.

[00213] From Figure 23B, it will be observed that the pass-band frequency 2302 of the PSF 238i/238q is tunable to be about 40kHz, 80kHz or 160kHz. A filter select signal 2306, operating in line with table 2304, determines which pass-band frequency 2302 is selected. At select '00', the filter select signal 2306 configures the PSF 238i/238q to have a passband frequency of about 40kHz; at select '01', the filter select signal 2306 configures the PSF 238i/238q to have a passband frequency of about 80kHz; at select '10', the filter select signal 2306 configures the PSF 238i/238q to have a passband frequency of about 160kHz; while select '11' is not used.

[00214] It was described above that the tunable pulse shaping filters I-PSF 238i and Q-PSF 238q are designed to have a first attenuation of 30 dB at 150 KHz, 300 KHz and 750 KHz respectively; and a second attenuation of 65 dB at 280 KHz, 560 KHz and 1120 KHz respectively.

[00215] To meet these attenuation requirements, a fifth order biquad structure with the first four poles being realized by a Chebyshev filter and the last pole being realized by a Butterworth filter was employed. Figure 24 shows the biquad structure 2400.

[00216] The bi-quad structure 2400 was chosen as it has less passive (RC) component value spread. As the corner frequencies and the stop band frequencies are related for the three filters, the resistor determining the frequency becomes multiples ( $R_Q$  and  $R_2$ ) as well when the capacitor ( $C_1$  and  $C_2$ ) is constant. Hence, the resistors  $R_Q$  and  $R_2$  were realized as parallel connection of three arms such that one or two arms are switched off to get the response for 80 KHz and 160 KHz filter respectively. A digital combinatorial logic (not shown) sends the filter select signal 2306 (Figure 23) to have the PSF 238i/238q (compare Figure 2) operate in the different frequency modes of 40, 80 and 160kHz. The input level shifter 2202 (also compare Figure 22) converts the common mode voltage from 0.25 V to 0.9 V ( $V_{DD}/2$ ). The output level shifter 2210 (also compare Figure 22) converts the

common mode voltage from 0.9 V to 0.35 V to drive the modulator 240 (Figure 2) having a PMOS based input (not shown). When the PSF 238i/238q (Figure 2) and the level shifters 2202 and 2210 are powered up, total current consumption is about 1.8 mA. In power down, the current consumption is less than about 1 $\mu$ A.

#### II)a) Modulator 240

**[00217]** Figure 25 shows a block level representation of the modulator 240 (Figure 2) in the transmitter path 204 (Figure 2) of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

**[00218]** The modulator 240 provides the three modulation schemes of DSB-ASK, PR-ASK and SSB-ASK through a DSB-ASK unit 2502, a PR-ASK unit 2504 and a SSB-ASK unit 2506 respectively. The DSB-ASK unit 2502, the PR-ASK unit 2504 and the SSB-ASK unit 2506 are controlled using a switch 2508. The modulation depth provided by each of the DSB-ASK unit 2502, the PR-ASK unit 2504 and the SSB-ASK unit 2506 is controlled by a modulation depth control signal 2510, whereby each ASK signal can have different modulation depths. The modulator 240 may be implemented using Gilbert-cell mixers with high linearity.

**[00219]** Figure 26 shows a block level representation of the single sideband amplitude shift keying (SSB-ASK) unit 2504 (also compare Figure 25) used by a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

**[00220]** The SSB-ASK unit 2504 includes an I-Mixer 2612i, a Q-Mixer 2612q, a summer unit 2650, a 0/90 quadrature signal generator 2646, an external local oscillator (LO) unit 2630 and a single to differential converter 2648. The 0/90 quadrature generator 2646 is coupled to both the I-Mixer 2612i and the Q-Mixer 2612q, while I-Mixer 2612i and the Q-Mixer 2612q are coupled to the summer unit 2650.

[00221] The I-Mixer 2612i and the Q-Mixer 2612q respectively facilitate modulation of a carrier with a frequency determined by the external LO unit 2630, where the carrier is modulated with I\_data signal 2648i and Q\_data signal 2648q. It will be appreciated that the I\_data 2648i and the Q\_data 2648q are analogous to the I\_data signal 248i (Figure 2) and the Q\_data signal 248q (Figure 2) after processing in the respective DACs 236i and 236q (Figure 2) and PSFs 238i and 238q (Figure 2). The outputs from the I-Mixer 2612i and the Q-Mixer 2612q are then added in the summer unit 2650 for amplification in the power amplifier 244 (Figure 2).

## II)b) Power Amplifier 244

[00222] Figure 27 shows a block level representation of the power amplifier (PA) 244 in the transmitter path 204 (Figure 2) of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

[00223] The power amplifier 244 includes a programmable attenuator 2702, an input matching unit 2704, power FETs 2708, a bias supply 2706 and an output matching unit 2710.

[00224] The programmable attenuator 2702 is coupled to the input matching unit 2704. The power FETs 2708 are coupled to the input matching unit 2704, the bias supply 2706 and the output matching unit 2710. The programmable attenuator 2702 is controlled by a 4-bit control signal 2712, while the power FETs are controlled by a power down control signal 2714.

[00225] Single-stage Class-A amplifiers with power output of +10dBm and output P1dB of +11dBm and power added efficiency of more than about 25% may be used. The power amplifier 244 is fully-integrated with programmability of transmit power in step of 1dB upto 16dB. The various components 2702, 2704, 2706, 2708 and 2710 use PTAT reference current source to enable them to operate from about -25°C to about +75°C.

[00226] Figure 28 shows a schematic diagram of the power amplifier 244 in the transmitter path 204 (Figure 2) of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

[00227] The various components 2702, 2704, 2706, 2708 and 2710 (Figure 27) are connected as shown in Figure 28.

[00228] In the embodiment shown in Figure 28, the Linear Class-A power amplifier 244 is designed with 15dB power control range. M1 and M2 are transistors having a cascode structure. M1 is biased to operate in Class-A mode, the bias voltage coming from a PTAT circuit (not shown) connected through resistor R2. M2 is self biased from the output through resistor R1 and capacitor C3, which improves the linearity of M2. M3 and M4 are transistors used to power down M2. M3 is a PMOS transistor which is used to switch on and off the gate voltage of M2. When the control voltage 2714 is low, the gate voltage of M2 is supplied from the drain of M2. When the control voltage 2714 is high, the gate of M2 is cut off from the drain of M2. M4 is a NMOS transistor which is part of a power off control circuit 2802. The function of M4 is to connect the gate of M2 to the ground to avoid floating during power down conditions. Inductor L1, capacitor C4 and capacitor C5 are part of the output matching circuit 2710 which provides maximum power for an optimum load impedance of 50 Ohm. The optimum load impedance is found with load-pull simulation. L1 also functions as DC feeding and can thus be considered to form part of the bias supply unit 2706 unit as well. Capacitor C6 is a decoupling capacitor for DC supply. Capacitor C1, inductor L2 and capacitor C2 are part of the input matching circuit 2704. All of the passive components are integrated on chip. C1 to C5 may be MIM capacitors, while C6 may be a MOS capacitor. L1 and L2 may be spiral inductors on a top metal layer. R1 and R2 may be polyresistors. The bias voltage is generated from a PTAT circuit (not shown) which may have reverse characteristics over temperature to the power amplifier 244 so that the resultant

characteristic of power output vs. temperature is nearly flat over the entire temperature range from -25°C to +75°C.

V) Application specific integrated circuit (ASIC) 408

[00229] Figure 29 shows a block level representation of the digital application specific integrated circuit (ASIC) 408 (also compare Figure 4) of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

[00230] The ASIC 408 provides a simple monitor and control interface to all the functions of the RFID transceiver (see Figure 2-6) through a power gain control signal 2902; a modulation scheme and depth control signal 2904; a synthesizer programming signal 2906; a power down control signal 2908; a filter switch, LNA switch, LO switch control signal 2910; and VGA control 1 and VGA control 2 signals 2912. Communication with the ASIC 408 is achieved using the serial peripheral interface signal 118 (also see Figure 4).

[00231] For example, the synthesizer programming signal 2906 can be used to control the operation of the PLL 206 (see Figure 4), while the VGA control 1 and VGA control 2 signals 2912 can control the operation of the I-VGA 218i (Figure 2) and the I-VGA 218q (Figure 2).

[00232] Table 3002 in Figure 30 summarises the logic control of the ASIC 408 and the corresponding effect achieved for each respective logic sequence. From table 3002, it can be appreciated that the RFID transceiver (see Figure 2-6) is switched on (i.e. logic level '10') only when the RFID transceiver (see Figure 2-6) receives backscatter signals.

[00233] The ASIC 408 provides for 20 shift registers for individual control of each of the individual components (for example 210, 212i and 212q, etc of Figure 2) in the RFID transceiver (see Figure 2-6). Tables 3004 and 3006 in Figure 30 summarises how each individual component in the RFID transceiver (see Figure 2-6)

can be powered down. It will be appreciated that selective powering down of the desired individual components facilitates debugging of the RFID transceiver (see Figure 2-6).

#### Measured Results

**[00234]** The RFID transceiver (see Figure 2-6) was fabricated in a commercial foundry using a standard 0.18 $\mu$ m CMOS process. The analog and mixed-signal circuits are simulated using h-spice and the RF blocks simulated using ADS (Advanced Design System). The RFID transceiver (see Figure 2-6) was packaged in a low-cost commercial TQFP100 package. The RFID transceiver (see Figure 2-6) performance was evaluated separately on a FR4 board and evaluated from a temperature of about -25°C to about +75°C. A UHF RFID reader system, incorporating a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention, was also fabricated to credit card size on 2-layer FR4 PCB material, with components on only one side of the PCB and the other side of the PCB being a complete ground plane. The performance of three such UHF RFID reader systems were tested and compared with the performance of commercially available discrete UHF reader. Measurement results, as discussed below, indicate that a UHF RFID reader systems incorporating a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention, matches the performance of conventional high-cost bulky Reader modules.

**[00235]** Figure 31 shows the transmit spectrum mask 3102 for a multiple interrogator environment, which meets the EPC Gen-2 standard. Channel spacing 3106 is about 500kHz for US. From Figure 31, it is observed that the measured output spectrum 3104, facilitated by the PSF, the band limited modulator and the power amplifier components of the RFID transceiver (see Figure 2-6) meets the standard.

**[00236]** Figure 32 shows measured pulse-shaping filter characteristics of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

[00237] Figure 33 shows measured carrier phase-noise at 860MHz (graph 3302) and 960MHz (graph 3304) of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention. Figure 33 illustrates that there is consistent phase noise over the entire RFID UHF band, where the measured noise is about -101dBc/Hz at 100kHz offset throughout the frequency range.

[00238] Figure 34A shows DSB-ASK modulation of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention. Figure 34B shows PR-ASK modulation of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention. Figure 34C shows SSB-ASK modulation of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention. Figures 34A to 34C demonstrate the possibility of using the RFID transceiver (see Figure 2-6) for all the modulation schemes used under the EPC Global Gen-2 standard. The desired modulation depth can be adjusted through the high-resolution 10-bit DACs.

[00239] Figure 35A shows a channel-select filter response in listen before talk mode of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention. Figure 35B shows a channel-select filter response in talk mode of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

[00240] Figure 36 shows a photograph of a die 3602 having a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention. The die 3602 is about 6 x 6mm and manufactured using a 1P6M 0.18 um CMOS process from Chartered semiconductor. The die 3602 can be fabricated on A TQP-100 package on FR-4 PCB.

[00241] Figure 37 shows a photograph of a UHF RFID reader system incorporating a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

[00242] Figure 38 shows a table summarizing the performance results of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

[00243] Figure 39 shows a table summarizing the range performance results of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

[00244] Figure 40 shows the response of a digital low pass filter (channel select filter) of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention. The response is to a 10 bit word length for a 80kHz pass band.

[00245] Figure 41A shows a signal 4102 in a transmission path of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention. The signal 4102 has undergone analog filtering but not modulation yet. Figure 41B shows a transmitted signal 4104 from a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention, along with a detection envelope 4106. Figure 41C compares a transmission spectrum mask 4108 of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention against the detection envelope 4106.

[00246] Figure 42B shows a SSB modulation spectrum of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention. Figures 42A and 42C show detected signals, in time domains, in a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

[00247] Figure 43 shows waveforms in a receiver path of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention, where an ideal local oscillator is used.

[00248] Figure 44 shows the effect of phase noise, with a blocking signal present, on signal performance of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

[00249] Figure 45 shows a two-tone output spectrum emitted from a power amplifier of a RFID transceiver (see Figure 2-6) built in accordance with an embodiment of the invention.

[00250] While embodiments of the invention have been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

**CLAIMS**

What is claimed is:

1. A radio frequency identification transceiver, comprising:  
a transmitter path, comprising:  
a pulse shaper to tunably shape the pulse of a signal to be transmitted in  
different predefined frequency ranges;  
a modulator to modulate the shaped pulse to be transmitted into one of a  
plurality of predefined frequency ranges;  
a receiver path, comprising:  
a demodulator to demodulate a received signal from a plurality of  
predefined frequency ranges.
2. The radio frequency identification transceiver of claim 1,  
wherein the transmitter path further comprises a digital-to-analog converter to  
convert a digital signal to be transmitted to an analog signal to be transmitted,  
wherein the digital-to-analog converter is coupled to the pulse shaper such that the  
analog signal to be transmitted is supplied to the pulse shaper.
3. The radio frequency identification transceiver of claim 1,  
wherein the transmitter path further comprises an attenuator to attenuate portions  
of the modulated signal to be transmitted, wherein the attenuator is coupled to the  
modulator to receive the modulated signal to be transmitted.

4. The radio frequency identification transceiver of claim 1,  
wherein the transmitter path further comprises at least one amplifier to amplify the modulated signal to be transmitted.
5. The radio frequency identification transceiver of claim 1,  
wherein the receiver path further comprises at least one amplifier to amplify the received signal.
6. The radio frequency identification transceiver of claim 5,  
wherein the amplifier is a low noise amplifier.
7. The radio frequency identification transceiver of claim 5,  
wherein the amplifier comprises two amplifier stages, a gain stage and a single-to-differential stage to provide a first differential signal and a second differential signal.
8. The radio frequency identification transceiver of claim 1,  
wherein the receiver path further comprises:
  - an in-phase mixer to provide a first differential in-phase signal and a second differential in-phase signal;
  - a quadrature mixer to provide a first differential quadrature signal and a second differential quadrature signal.

9. The radio frequency identification transceiver of claim 8,  
wherein the receiver path further comprises:
- an in-phase amplifier coupled to the in-phase mixer to amplify the first differential in-phase signal and the second differential in-phase signal;
  - a quadrature amplifier coupled to the quadrature mixer to amplify the first differential quadrature signal and the second differential quadrature signal.
10. The radio frequency identification transceiver of claim 9,  
wherein the receiver path further comprises at least one tunable filter to filter the amplified differential signals provided by the in-phase amplifier and the quadrature amplifier.
11. The radio frequency identification transceiver of claim 10,  
wherein the receiver path further comprises:
- an in-phase variable gain amplifier to amplify the filtered first differential in-phase signal and the filtered second differential in-phase signal;
  - an quadrature variable gain amplifier to amplify the filtered first differential quadrature signal and the filtered second differential quadrature signal.
12. The radio frequency identification transceiver of claim 1 and claim 11,

wherein the demodulator is coupled to an output of the in-phase variable gain amplifier to receive the amplified filtered first differential in-phase signal and the amplified filtered second differential in-phase signal and to an output of the quadrature variable gain amplifier to receive the amplified filtered first differential quadrature signal and the amplified filtered second differential quadrature signal.

13. The radio frequency identification transceiver of claim 1 and claim 11,  
wherein the receiver path further comprises:
  - an in-phase analog-to-digital converter to convert an analog in-phase signal provided by the in-phase variable gain amplifier to a digital in-phase signal;
  - a quadrature analog-to-digital converter to convert an analog quadrature signal provided by the quadrature variable gain amplifier to a digital quadrature signal.
14. The radio frequency identification transceiver of claim 1, further comprising:  
a synthesizer to provide oscillator signals.
15. The radio frequency identification transceiver of claim 8 and claim 14,  
wherein the synthesizer is coupled to the in-phase mixer to provide an in-phase local oscillator signal to the in-phase mixer;

wherein the synthesizer is coupled to the quadrature mixer to provide a quadrature local oscillator signal to the quadrature mixer.

16. The radio frequency identification transceiver of claim 14,  
wherein the synthesizer is coupled to the modulator to provide an in-phase radio frequency oscillator signal and a quadrature radio frequency oscillator signal to the modulator.
17. The radio frequency identification transceiver of claim 14,  
wherein the synthesizer comprises at least one phase locked loop circuit.
18. The radio frequency identification transceiver of claim 1,  
wherein the predefined frequency ranges are in the range of about 860 MHz to about 960 MHz.