WHAT IS CLAIMED IS:

1. A leakage compensation dynamic register, comprising:

an input terminal for inputting data;

an output terminal for outputting the data;

a clock signal terminal for supplying a clock signal;

an analog switch unit for transmitting the data under control of the clock signal;

a data latch unit for latching the data under control of the clock signal; and

an output drive unit for inverting and outputting the data received from the data latch unit;

the analog switch unit, the data latch unit and the output drive unit being sequentially connected in series between the input terminal and the output terminal, and the analog switch unit and the data latch unit having a node therebetween,

wherein the leakage compensation dynamic register further comprises a leakage compensation unit electrically connected between the node and the output terminal, wherein the leakage compensation unit has a first terminal electrically connected to the output terminal, a second terminal electrically connected to the node, and a control terminal electrically connected to a power supply or the node;

wherein the leakage compensation unit comprises a PMOS transistor and a NMOS transistor connected in series between the output terminal and the node, the PMOS transistor has a source terminal electrically connected to the output terminal, a drain terminal electrically connected to a drain terminal of the NMOS transistor, and a gate terminal electrically connected to the control terminal, and the NMOS transistor has a source terminal electrically connected to the node, the drain terminal, and a gate terminal electrically connected to the control terminal; and

wherein the gate terminal of the PMOS transistor and the gate terminal of the NMOS transistor are electrically connected to the power supply or to the node.

2. A leakage compensation dynamic register, comprising:

an input terminal for inputting data;

an output terminal for outputting the data;

a clock signal terminal for supplying a clock signal;

an analog switch unit for transmitting the data under control of the clock signal;

a data latch unit for latching the data under control of the clock signal; and

an output drive unit for inverting and outputting the data received from the data latch unit;

the analog switch unit, the data latch unit and the output drive unit being sequentially connected in series between the input terminal and the output terminal, and the analog switch unit and the data latch unit having a node therebetween,

wherein the leakage compensation dynamic register further comprises a leakage compensation unit electrically connected between the node and the output terminal, wherein the leakage compensation unit has a first terminal electrically connected to the output terminal, a second terminal electrically connected to the node, and a control terminal electrically connected to a ground or the node;

wherein the leakage compensation unit comprises a PMOS transistor and a NMOS transistor connected in series between the output terminal and the node, the PMOS transistor has a source terminal electrically connected to the node, a drain terminal, and a gate terminal electrically connected to the control terminal, and the NMOS transistor has a source terminal electrically connected to the output terminal, a drain terminal electrically

connected to the drain terminal of the PMOS transistor, and a gate terminal electrically connected to the control terminal; and

wherein the gate terminal of the PMOS transistor and the gate terminal of the NMOS transistor are electrically connected to the ground or to the node.

3. A leakage compensation dynamic register, comprising:

an input terminal for inputting data;

an output terminal for outputting the data;

a clock signal terminal for supplying a clock signal;

an analog switch unit for transmitting the data under control of the clock signal;

a data latch unit for latching the data under control of the clock signal; and

an output drive unit for inverting and outputting the data received from the data latch unit;

the analog switch unit, the data latch unit and the output drive unit being sequentially connected in series between the input terminal and the output terminal, and the analog switch unit and the data latch unit having a node therebetween,

wherein the leakage compensation dynamic register further comprises a leakage compensation unit electrically connected between the node and the output terminal, wherein the leakage compensation unit has a first terminal electrically connected to the output terminal, a second terminal electrically connected to the node, and a control terminal electrically connected to a power supply; and

wherein the leakage compensation unit comprises a PMOS transistor having a source terminal electrically connected to the output terminal, a drain terminal electrically connected to the node, and a gate terminal electrically connected to a power supply.

4. A leakage compensation dynamic register, comprising:

an input terminal for inputting data;

an output terminal for outputting the data;

a clock signal terminal for supplying a clock signal;

an analog switch unit for transmitting the data under control of the clock signal;

a data latch unit for latching the data under control of the clock signal; and

an output drive unit for inverting and outputting the data received from the data latch unit;

the analog switch unit, the data latch unit and the output drive unit being sequentially connected in series between the input terminal and the output terminal, and the analog switch unit and the data latch unit having a node therebetween,

wherein the leakage compensation dynamic register further comprises a leakage compensation unit electrically connected between the node and the output terminal, wherein the leakage compensation unit has a first terminal electrically connected to the output terminal, a second terminal electrically connected to the node, and a control terminal electrically connected to a ground; and

wherein the leakage compensation unit comprises a NMOS transistor having a source terminal electrically connected to the node, a drain terminal electrically connected to the output terminal, and a gate terminal electrically connected to a ground.

5. The leakage compensation dynamic register according to any of claims 1 to 4, wherein the clock signal comprises a first clock signal and a second clock signal in a reversed phase.

6. The leakage compensation dynamic register according to any of claims 1 to 4, wherein the analog switch unit is a transmission gate.

7. The leakage compensation dynamic register according to any of claims 1 to 4, wherein the data latch unit is a three-state inverter.

8. The leakage compensation dynamic register according to any of claims 1 to 4, wherein the output drive unit is an inverter.

9. A data operation unit, comprising a control circuit, an operational circuit and a plurality of leakage compensation dynamic registers interconnected with each other, the plurality of leakage compensation dynamic registers being connected in series and/or in parallel, wherein the plurality of leakage compensation dynamic registers are the leakage compensation dynamic register according to any of claims 1 to 8.

10. A chip, comprising at least one of the data operation units according to claim 9.

11. A hash board for a computing apparatus, comprising at least one of the chips according to claim 10.

12. A computing apparatus, comprising a power supply board, a control board, a connection board, a radiator and a plurality of hash boards, the control board connected to the hash boards through the connection board, the radiator provided around the hash boards, and the power supply board configured to supply a power supply for the connection board,

the control board, the radiator and the hash boards, wherein the hash board is the hash board according to claim 11.