

METHOD AND APPARATUS FOR A PRINTED CIRCUIT BOARD USING LASER ASSISTED METALLIZATION AND PATTERNING OF A SUBSTRATE

Background

Field

[0001] The embodiments relate to microelectronic structures, and more particularly to microelectronic structures made using laser assisted activation and patterning.

Description of the Related Art

[0002] The state of the art provides numerous techniques for manufacturing a printed circuit board. The starting material is a microelectronic substrate, typically a dielectric board such as, for example, an ABF (Ajinomoto Build-up Film) layer, which may then be processed according to one of the numerous techniques mentioned above to provide the printed circuit.

[0003] One such technique involves providing the dielectric layer, and then laser drilling via openings into the dielectric layer. Thereafter, the dielectric layer is roughened, subjected to chemical copper plating, such as electroless plating, to provide a thin layer of copper over the entire dielectric layer including on the walls of the via openings. A dry-film resist (DFR) is then laminated onto the thin layer of copper, and the DFR thereafter subjected to an expose and develop process to form the circuit design pattern in accordance with the requirements of the circuit specifications. After subjecting the DFR to a developing solution in order to wash away exposed areas of the same, the combination of the dielectric layer-thin copper layer-patterned DFR is subjected to electrolytic copper plating in order to provide a copper layer (hereinafter "thick copper layer") much thicker than the thin copper layer mentioned above both on regions of the thin copper layer not covered by the patterned DFR (in order to provide conductive traces on the dielectric layer), and, in addition, inside the via

openings. Thus, after further plating of the thick copper layer to protect the same from etching, the patterned DFR is stripped from the combination to expose the thin copper layer not covered by the thick copper layer. The thus bare thin copper layer is now completely etched away down to the dielectric layer leaving a printed circuit board.

[0004] Another conventional technique for providing printed circuit boards involves the provision of a dielectric layer, such as an ABF layer, followed by a laser drilling process for providing via openings in the ABF layer. Thereafter, a DFR is laminated onto the dielectric layer, and the DFR thereafter subjected to an expose and develop process to form the circuit design pattern in accordance with the requirements of the circuit specifications. After subjecting the DFR to a developing solution in order to wash away exposed areas of the same, the combination of the dielectric layer-thin copper layer-patterned DFR is subjected to an etching process in order to ablate a predetermined thickness of the dielectric layer that remains uncovered by the patterned DFR, thus providing recesses within the dielectric layer corresponding to a location of the conductive traces to be provided on the dielectric layer. The patterned DFR is then stripped from the dielectric layer. Thereafter, the dielectric layer is subjected to electroless copper plating to provide a thin layer of copper over the entire dielectric layer including on the walls of the via openings and inside the recesses provided at the location of the traces. A thicker layer of copper is then provided onto the thin copper layer by way of electrolytic plating, and the thus formed combination subjected to either back etching, grinding or CMP in order to result in a printed circuit board.

[0005] Another known technique for providing interconnects according to the prior art is typically referred to as "Laser Embedded Technology," or LET. In LET, laser ablation is used to provide via openings in a dielectric layer, such as an ABF layer. Thereafter, locations for the traces

are ablated also using laser irradiation to provide recessed trace locations on the dielectric layer. Thereafter, electroless plating, and, thereafter, electrolytic plating with copper are provided on the thus ablated dielectric layer. Copper plating as described above results in the formation of a copper layer on the active surface of the dielectric layer, the copper layer filling the recessed trace locations and extending above the same. Thereafter, a process such as chemical mechanical polishing is used to remove the excess copper of the copper layer extending beyond the recessed trace locations, in this way resulting in the interconnects on the active surface of the dielectric layer.

[0006] However, techniques of the prior art such as those described above, may exhibit low throughput due to increased processing time, and, in addition, may be ineffective for meeting current alignment budgets among others because they require the use of multiple processes for generating the vias and traces, which processes lead to a compounding of possible alignment errors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0008] Fig. 1 is a cross sectional view of a microelectronic substrate, or panel;

[0009] Fig. 2 is a cross sectional view showing the substrate of Fig. 1 as having been provided with a via opening therein to yield a via-defining substrate according to an embodiment;

[0010] Fig. 3 is a cross sectional view showing the substrate of Fig. 2 as having been provided with a laser activatable laser activatable film thereon to yield a film-substrate combination according to an embodiment;

[0011] Fig. 4a is a cross sectional view showing the film in the combination of Fig. 3 as having been exposed to laser irradiation to selectively activate portions of the film based on a predetermined interconnect pattern to yield a selectively-activated-film-substrate combination according to an embodiment;

[0012] Fig. 4b is a top plan showing the film in the combination of Fig. 3 as having been exposed to laser irradiation to selectively activate portions of the film based on a predetermined interconnect pattern to yield a selectively-activated-film-substrate combination according to an embodiment;

[0013] Fig. 5a is a cross sectional top plan view showing the combination of Figs. 4a and 4b as having had non-activated portions of the film removed therefrom to yield a patterned f-build-up-layer-substrate combination according to an embodiment;

[0014] Fig. 5b is a top plan view showing the combination of Figs. 4a and 4b as having had non-activated portions of the film removed therefrom to yield a patterned f-build-up-layer-substrate combination according to an embodiment;

[0015] Fig. 6a is a cross sectional view showing the combination of Figs. 5a and 5b as having been provided with a conformal electrolessly deposited first conductive layer to yield an electrolessly plated substrate according to an embodiment;

[0016] Fig. 6b is a top plan view showing the combination of Figs. 5a and 5b as having been provided with a conformal electrolessly deposited first conductive layer to yield an electrolessly plated substrate according to an embodiment;

[0017] Fig. 7a is a cross sectional view showing the electrolessly plated substrate of Figs. 6a and 6b as having been provided with an electrolytically deposited second conductive layer to yield an electrolytically plated substrate according to an embodiment;

[0018] Fig. 7b is a top plan view showing the electrolessly plated substrate of Figs. 6a and 6b as having been provided with an electrolytically deposited second conductive layer to yield an electrolytically plated substrate according to an embodiment;

[0019] Fig. 8 is a top plan view showing the electrolytically plated substrate of Figs. 7a and 7b as having had its tie bars removed to yield a patterned substrate or printed circuit board;

[0020] Fig. 9 is a schematic representation of a system incorporating a printed circuit board according to an embodiment;

[0021] Fig. 10 is a cross sectional view of a result of an embodiment of microelectronic substrates, or panels being laminated;

[0022] Figs. 11A-B are cross sectional views of a result of an embodiment of microelectronic substrates, or panels after being patterned using laser projection machining/patterning;

[0023] Figs. 12A-B are cross sectional views of a result of an embodiment of microelectronic substrates, or panels after a dielectric layer lamination process;

[0024] Fig. 13 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after an organic material build up process;

- [0025] Fig. 14 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after laser via drilling;
- [0026] Fig. 15 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after dip coating;
- [0027] Fig. 16 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after laser activation;
- [0028] Fig. 17 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after washing;
- [0029] Fig. 18 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after selective electrolytic plating;
- [0030] Fig. 19 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after subsequent dielectric build up;
- [0031] Fig. 20 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after laser via drilling;
- [0032] Fig. 21 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after dip coating;
- [0033] Fig. 22A is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after laser activating the surface of the substrate illustrated in Fig. 21;
- [0034] Fig. 22B is a top plan view of a result of an embodiment of a microelectronic substrate, or panel after laser activating the surface of the substrate illustrated in Fig. 21;

[0035] Fig. 23A is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after washing;

[0036] Fig. 23B is a top plan view of a result of an embodiment of a microelectronic substrate, or panel after washing;

[0037] Fig. 24A is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after a dielectric layer build up;

[0038] Fig. 24B is a top plan view of a result of an embodiment of a microelectronic substrate, or panel after a dielectric layer build up;

[0039] Fig. 25 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after via drilling;

[0040] Fig. 26 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after controlled-collapse-chip-connect (C4) solder ball and first level interconnect (FLI) bumping;

[0041] Fig. 27 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after etching a sacrificial metal layer away forming metal protrusions;

[0042] Fig. 28 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after electroless plating;

[0043] Fig. 29 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after via filling and/or electrolytic plating;

[0044] Fig. 30 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after dry film resist (DFR) lamination;

[0045] Fig. 31 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after trace ablation and assisted metallization;

[0046] Fig. 32 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after trace electroless plating;

[0047] Fig. 33 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after trace electrolytic plating; and

[0048] Fig. 34 is a cross sectional view of a result of an embodiment of a microelectronic substrate, or panel after DFR stripping.

DETAILED DESCRIPTION

[0049] The embodiments discussed herein generally relate to a method, a printed circuit board and a system using laser assisted metallization and patterning. Referring to the figures, exemplary embodiments will now be described. The exemplary embodiments are provided to illustrate the embodiments and should not be construed as limiting the scope of the embodiments.

[0050] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present invention, however, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0051] Referring now to Fig. 1 by way of example, embodiments of the present invention comprise providing a microelectronic substrate or panel, such as substrate 100, provided on a conductive layer 101 (see Fig. 2).

The substrate may include a non-conductive material, such as plastic or fiberglass, such as ABF, or any other dielectric suitable to serve as a substrate for a printed circuit board. Conductive layer 101 may, by way of example, comprise copper, and may further represent a conductive trace on an underlying substrate (not shown).

[0052] As seen in Fig. 2 by way of example, embodiments of the present invention comprise providing via openings such as opening 110, in the substrate, such as substrate 100, to provide a via-defining substrate, such as substrate 120. According to a preferred embodiment, the via openings such as opening 110 may be provided using laser drilling or laser projection machining, such as high intensity laser drilling as is well known in the art. However, the via openings such as opening 110 may be provided according to any one of well known methods as would be readily recognizable by one skilled in the art.

[0053] Referring thereafter to Fig. 3 by way of example, embodiments of the present invention comprise providing a laser activatable film, such as, for example, film 130, comprising a laser activatable material on the via-defining substrate. According to an embodiment, the laser activatable film may have a thickness in the submicron range up to about between about 3 to about 5 microns. By "laser activatable material," what is meant in the context of the instant description is a material that is adapted to be activated when exposed to laser irradiation to provide a build up layer for a conductive material, such as, for example, copper. By "build-up layer," what is meant in the context of the present invention is a seed layer, that is, a layer adapted to allow selective provision of a conductive material thereon according to its pattern. According to a one embodiment, the laser activatable material may comprise palladium acetate or $(\text{CH}_3\text{CO}_2)_2\text{Pd}$. According to an embodiment, provision of the laser activatable film, such as film 130 shown in Fig. 3, may be effected by dip coating via-defining substrate 120 in a laser-activatable material seeding solution, such as, for example, a palladium acetate seeding

solution. Other methods for providing the laser activatable film according to embodiments, include, by way of example, sputtering and chemical or physical vapor deposition. As seen in Fig. 3, the laser activatable film, such as film 130, covers an active surface of the via-defining substrate, such as substrate 120, and includes via portions, such as portions 135 and 136, which respectively cover the walls and the bottom of the via opening, such as via opening 110, respectively. By "active surface," what is meant in the context of the present invention is a surface of the substrate adapted to be provided with interconnects, such as vias and traces, according to an interconnect pattern. Provision of the laser activatable film on the active surface of the via-defining substrate yields a film-substrate combination, such as film-substrate combination 140 of Fig. 3.

[0054] Referring next to Figs. 4a-8 by way of example, embodiments of the present invention comprise providing interconnects according to a predetermined interconnect pattern on the via-defining substrate using laser assisted metallization. Laser assisted metallization will be explained in further detail below with respect to the embodiment of Figs. 4a-8.

[0055] Referring first to Figs. 4a-4b by way of example, laser assisted metallization according to embodiments comprises exposing the laser-activatable material of the laser activatable film to laser irradiation to selectively activate portions of the laser activatable film according to the predetermined interconnect pattern, and, optionally, to a predetermined tie bar pattern, to yield a selectively-activated-film-substrate combination, or SATFP combination, such as combination 150 of Figs. 4a and 4b. By "predetermined interconnect pattern," what is meant in the context of the instant description is a pattern corresponding to the predetermined interconnect traces and/or vias to be provided on the active surface of the substrate. By "predetermined tie-bar pattern," what is meant in the context of the instant description is a pattern corresponding to the predetermined tie bars to be provided on the active surface of the substrate. Thus, as seen in

the embodiment of Figs. 4a and 4b, the SATFP combination 150 may comprise a substrate portion 102 formed from substrate 100 of Fig. 1 as described above, and, in addition, a film 152 covering substrate portion 102 and defining a pattern 154, as best seen in Fig. 4b. The pattern 154 corresponding to film 152 is defined by laser activated portions 130', 135' and 136' of film 152, by non-activated portions 130 of film 152, and by laser activated tie bar regions 144 as will be described in greater detail below. The laser activated portions may include a material adapted to provide a build up layer for further conductive material to be selectively provided thereon. For example, the laser activated portions may include a graphite rich conductive seeding material. According to an embodiment, when the laser activatable film comprises palladium acetate, the laser activated portions of the film comprise a palladium-seeded build-up layer including a palladium rich modified organic material build-up surface. In particular, laser activation of a palladium acetate material selectively ablates the acetates in the material, leaving behind the palladium rich modified organic material as noted above.

[0056] The laser source for both laser drilling of via openings and for the activation of the laser activatable material may be any suitable source that generates laser beams. Examples of the laser source may include a Nd:YAG laser tool or a pulsed ultra-violet (UV) excimer laser, the latter being preferred according to embodiments. The wavelength may be any suitable wavelength for the application, such as Neodymium-doped Yttrium Aluminum Garnet (Nd:YAG, 1064nm), Xenon Fluoride (XeF, 351 nm), Xenon Chloride (XeCl, 308 nm), Xenon Bromide (XeBr, 282nm), Krypton Fluoride (KrF, 248 nm), Argon Fluoride (ArF, 193 nm), and Fluoride Dimer (F₂, 157 nm), wavelength ranges in the UV or deep UV ranges being preferred according to embodiments. By way of example, to activate the laser activatable film using laser irradiation, according to an embodiment, a laser pulse duration may first be chosen, such as, for example, about 20 ns to about 50 ns for a laser source set at wavelengths including, for example, 193

nm, 248 nm or 308 nm. Once pulse duration is set, the number of pulses to be delivered may be determined as a function of a thickness of the laser activatable film. A rough estimate for determining the number of pulses to be delivered would be based on the thickness to be activated per pulse. For example, with respect to an organic film such as palladium acetate, the activated thickness per pulse ratio would be about 1 micron for a 193 nm, 248 nm or 308 nm laser source. Whether or not "activation" has been achieved may be determined in a number of ways, such as, for example, through a testing process involving measuring a conductivity of respective laser activated portions obtained as a result of corresponding laser irradiation doses. A laser activated portion with a conductivity comparable to that of a metal or of a metal-like conductor would then be considered "activated" according to embodiments, and would set the laser irradiation dose to be delivered for a given laser activatable film thickness and laser activatable material. Alternatively or in conjunction with the above testing method, a composition of each respective laser activated portion may further be determined to ascertain conductivity and hence activation.

[0057] To provide the laser activated portions 130', 135' and 136', and non-activated portions 130' of pattern 154, the film-substrate 140 of Fig. 3 may be selectively subjected to laser irradiation according to a predetermined interconnect pattern. According to a preferred embodiment, the selective irradiation according to the predetermined interconnect pattern may be effected for example by laser irradiation of the film of film-substrate combination through a mask, the pattern of which corresponds to the predetermined interconnect pattern. In the alternative, the selective irradiation may be effected by a computer aided design (CAD) driven laser direct write. Selective laser irradiation of the laser activatable film according to the predetermined interconnect pattern results in laser activated portions of the film, such as portions 130', corresponding to a predetermined pattern of traces to be provided on the active surface of the substrate, and such as portions 135' and 136', corresponding to a predetermined pattern for a vias by way of via opening 110. Optionally, to provide laser activated tie bar regions 144, the film-substrate combination 140 of Fig. 3 may, according to embodiments, be selectively subjected to laser irradiation according to a predetermined tie bar pattern. As would be recognized by one skilled in the art, the activated tie bar regions would be provided where electrolytic plating on the build up layer is contemplated. The activated tie bar regions would thus allow the provision of tie bars thereon which would in turn provide the necessary electrical interconnections during electrolytic plating, as will be described further below. According to a preferred embodiment, the selective irradiation according to the predetermined tie bar pattern may be effected for example by using laser direct writing on the film of the film-substrate combination, such as a CAD driven laser direct write. Selective laser irradiation of the laser activatable film according to a predetermined tie bar pattern may occur simultaneously with selective laser irradiation of the laser activatable film according to a predetermined interconnect pattern, and results in laser activated tie bar regions of the film, such as regions 144 shown in Fig. 4b.

[0058] Referring next to Figs. 5a and 5b by way of example, laser assisted metallization according to embodiments comprises removing non-activated portions of the partially activated film to yield a patterned-build-up-layer-substrate combination. As shown in the embodiments of Figs. 5a and 5b, a removal of non-activated portions 130' would result in a patterned-build-up-layer-substrate combination 161 as shown, including substrate portion 102 having exposed surfaces 104, activated tie bar regions 144, and further including a patterned build up layer 162 including the activated portions 130', 135' and 136' and activated tie bar regions. According to a preferred embodiment, removing comprises subjecting the partially activated film to a wash. For example, when the material of the patterned build up layer includes a palladium rich modified organic material obtained through laser activation of a palladium acetate laser activatable film, the wash may comprise a water wash.

[0059] Referring next to Figs. 6a-8 by way of example, laser assisted metallization according to embodiments comprises providing interconnects according to the predetermined interconnect pattern on the patterned-build-up-layer-substrate combination to provide a printed circuit board. By "interconnects," what is meant in the context of the present invention is the combination of conductive traces and vias according to the predetermined interconnect pattern. For example, as seen in Fig. 8, the printed circuit board 190 comprises substrate portion 102 and interconnects 192 provided on the substrate portion 102, the interconnects comprising traces 189 and a via 187 as shown according to the predetermined interconnect pattern. Providing interconnects may be provided according to any well known method using the build up layer 162 as a seed layer. For example, providing interconnects may be effected using solely electroless plating, that is, electroless plating without any further metallization, or using a combination of electroless plating and electrolytic plating. Providing interconnects using a combination of electroless plating and electrolytic plating as mentioned

above will now be described in further detail in relation to the example preferred embodiment of Figs. 6a-8.

[0060] Thus, as seen in Figs. 6a-6b by way of example, laser assisted metallization according to embodiments comprises providing a first conductive layer on the build-up layer of the patterned-build-up-layer-substrate combination through electroless plating, the first conductive layer defining a seed layer having a pattern corresponding to the pattern of the build up layer, thus providing an electrolessly plated substrate, such as electrolessly plated substrate 164 of Figs. 6a and 6b. It is noted that, as is well known, to the extent that the build-up layer 162 serves as a seed for the further electrolessly plated conductive layer, the build-up layer serves as a site of atomic nucleation for the electrolessly plated conductive layer, and, as a result, no longer exists as a "layer" proper, the atoms thereof having been dispersed after electroless plated. As a result, a build-up layer is not shown in Figs. 6a-8. It is noted, however, that, to the extent that the build-up layer serves as a site of atomic nucleation, atoms from the build-up layer still remain at least in the electrolessly plated copper layer. As seen in Figs. 6a and 6b, the electrolessly plated substrate 164 includes substrate portion 102 having exposed regions 104, build up layer 162, and an electrolessly plated first conductive layer including conformal conductive seed layer 168 selectively provided on the build up layer 162. Seed layer 168 includes, in the shown embodiment, seed layer portions 165 and 166, which respectively occupy regions corresponding to the walls and the bottom of via opening 110, seed layer portion 160, which respectively occupy regions corresponding to the traces, and tie bar seed layer portions 174.

[0061] Referring next to Figs. 7a and 7b by way of example, laser assisted metallization according to embodiments comprises providing a second conductive layer on the first conductive layer of the electrolessly plated substrate through electrolytic plating such that the second conductive layer defines a pattern corresponding to the pattern of the first conductive

layer and of the build up layer, thus providing an electrolytically plated substrate, such as electrolytically plated substrate 164 of Figs. 6a and 6b. As seen in Figs. 6a and 6b, the electrolytically plated substrate 180 includes substrate portion 102 having exposed regions 104, build up layer 162, an electrolessly plated first conductive layer including conformal conductive seed layer 168 selectively provided on the build up layer 162, and an electrolytically plated second conductive layer 182. Second conductive layer includes, in the shown embodiment, second conductive layer portion 185, which defines via 187, second conductive layer portion 188, which defines traces 189, and tie bar portions 183 which define tie bars 184.

[0062] Referring next to Fig. 8 by way of example, embodiments of the present invention further comprise removing the tie bars to provide a printed circuit board, such as printed circuit board 190. Thus, as seen in Fig. 8, the printed circuit board comprises traces 189 and a via 187 according to the predetermined interconnect pattern. According to a preferred embodiment, removing the tie bars may comprise laser ablation of the tie bars. By "removing," what is meant in the context of the present invention encompasses both substantially complete removal and trimming, as would be recognized by one skilled in the art. As described above with respect to the example embodiment shown in Figs. 1-8, embodiments of the present invention propose a process flow for a novel, laser-based substrate manufacturing process of laser assisted metallization and patterning ("LAMP"). The LAMP technology, as described above, may use laser irradiation to provide via openings, such as by way of drilling, and may selectively metallize an organic material of a build up layer to form a required design circuitry pattern, or predetermined interconnect pattern, without the necessity for any lithographic processing. The laser may be used through laser projection machining, laser assisted metallization and laser direct writing. Laser projection machining may be used to provide via openings using laser ablation, in a well known manner. Laser assisted metallization may be used according to embodiments to activate a laser

activatable material on the surface of a substrate according to the predetermined interconnect pattern. Activation of the laser activatable material and removal of any non-activated portions of the laser activatable material results in the formation of patterned a build up layer on the substrate including a conductive material seed element, such as a palladium rich modified organic material as a copper seed layer. Laser direct writing may optionally be used to create a tie bar structure needed for electrolytic plating where electrolytic plating is contemplated. A printed circuit board obtained according to method embodiments comprises a via-defining substrate comprising a microelectronic substrate defining via openings therein; and interconnects provided on the via-defining substrate according to a predetermined interconnect pattern, the interconnects comprising a conductive layer having a pattern corresponding to the predetermined interconnect pattern, the conductive layer further being made substantially from a first material, the conductive layer further comprising a second material different from the first material, the second material including a metallic seeding material and being present on the via-defining substrates only at regions corresponding to the interconnects.

[0063] Advantageously, embodiments of the present invention provide a printed circuit board that has an electric circuit firmly attached to the dielectric surface and vias that are electrically connected and suitable for accepting the electronic components that will be mounted thereon. Embodiments of the present invention provide many advantages over the process on record (POR) substrate process such as high resolution, elimination of the multisteps lithographic process, improved alignment capabilities, and eliminate de-smearing. In particular, embodiments of the present invention according to LAMP use laser irradiation both for creating via openings and, in addition, for providing a patterned build up layer having a pattern corresponding to the desired (predetermined) interconnect pattern, thus eliminating the need for lithography with respect to providing the interconnects. The use of LAMP according to embodiments

advantageously: (1) eliminates the lithography process, and therefore the need to use dry film resist (DFR) and its associated processes; (2) eliminates the need for a desmear process; (3) provide high resolution patterning and metallization by allowing the patterning and metallization of features sizes in the nanometer range as governed by the wavelength range of the laser source used, such as, for example, a UV wavelength range; (4) provides improved alignment capabilities for both via and interconnect patterning and metallization since (a) eliminates compound effects of having to use both laser irradiation for generation of via openings and lithography for generation of the interconnect pattern; (b) provides a higher imaging alignment than that associated with a contact masking process for lithography; (c) where a UV laser is used as the laser source, provides better alignment when compared with the IR CO₂ laser used in prior art processes for laser via drilling.

[0064] With respect to the LET process described in the Background section above, embodiments of the present invention advantageously dispense with a necessity to ablate the substrate on two occasions as described, once to provide the via openings, and again to provide recessed trace locations as described above. In addition, embodiments of the present invention advantageously dispense with a need to etch the substrate in order to provide an interconnect pattern on the substrate, thus significantly improving throughput and meanwhile producing traces that are identical to known non-LET traces, that is, traces disposed substantially at the substrate surface rather than embedded traces. In addition, embodiments of the present invention advantageously dispense with a need to remove excess conductive material from the trace and/or via locations through any means, such as through grinding or through chemical mechanical polishing. Advantageously, embodiments of the present invention result in the introduction of conductive material seeding only in areas corresponding to the predetermined interconnect pattern. Additionally, where the provision of the interconnects according to an embodiment involves solely electroless

plating, that is, electroless plating without electrolytic plating, advantageously, significant cost and throughput advantages may be achieved.

[0065] Referring to Fig. 9, there is illustrated one of many possible systems in which embodiments of the present invention may be used. The shown system 90 therefore comprises an electronic assembly 1000 which includes a printed circuit board such as, for example, printed circuit board 190 of Fig. 8 described above. In an alternate embodiment, the electronic assembly 1000 may include an application specific IC (ASIC). Integrated circuits found in chipsets (e.g., graphics, sound, and control chipsets) may also be packaged in accordance with embodiments of this invention.

[0066] For the embodiment depicted by Fig. 9, the system 90 may also include a main memory 1002, a graphics processor 1004, a mass storage device 1006, and/or an input/output module 1008 coupled to each other by way of a bus 1010, as shown. Examples of the memory 1002 include but are not limited to static random access memory (SRAM) and dynamic random access memory (DRAM). Examples of the mass storage device 106 include but are not limited to a hard disk drive, a compact disk drive (CD), a digital versatile disk drive (DVD), and so forth. Examples of the input/output module 1008 include but are not limited to a keyboard, cursor control arrangements, a display, a network interface, and so forth. Examples of the bus 1010 include but are not limited to a peripheral control interface (PCI) bus, and Industry Standard Architecture (ISA) bus, and so forth. In various embodiments, the system 90 may be a wireless mobile phone, a personal digital assistant, a pocket PC, a tablet PC, a notebook PC, a desktop computer, a set-top box, a media-center PC, a DVD player, and a server.

[0067] Another embodiment eliminates two steps of copper plating. That is elimination of electroless copper plating in the fabrication of substrates for a printed circuit board. Figs. 10-27 illustrate the embodiment

of making a coreless substrate using LAMP without using electroless plating.

[0068] Fig. 10 illustrates lamination of copper panels 1000 together. Figs. 11A-11B illustrate patterning copper panels 1000 using laser projection patterning (machining) on both of the copper panels. The result of the laser patterning are the patterns 1110.

[0069] Figs. 12A-12B illustrate double-sided lamination of dielectric layer 1200. Dielectric layer 1200 may be plastic or fiberglass, such as ABF, or any other dielectric suitable to serve as a substrate for a printed circuit board. Fig. 13 illustrates organic material 1310 build up lamination on the copper panel. It should be noted that while Figs. 13-27 illustrate processes on one of the copper panels, both copper panels can be processed with the same processes.

[0070] Fig. 14 illustrates laser drilling the organic build up material forming a plurality of vias 1400. Fig. 15 illustrates the result of dip coating the substrate illustrated in Fig. 14 with a palladium solution forming a seed coat 1510. Following with Fig. 16, the substrate illustrated in Fig. 15 has the palladium seed coat laser activated by laser assisted metallization. As illustrated, reference 1610 represents the activated portions of surface and reference 1620 represents the non-activated portions. In one embodiment when the seed coating is palladium acetate, the laser activated portions 1610 of the film (e.g., ABF) comprise a palladium-seeded build-up layer including a palladium rich modified organic material build-up surface. In particular, laser activation of a palladium acetate material selectively ablates the acetates in the material, leaving behind the palladium rich modified organic material as noted above. In one embodiment the laser activation of the surface follows the pattern for both lines and micro-vias is done by mask projection machining or through a CAD driven laser direct write .

[0071] Fig. 17 illustrates the result of washing the palladium acetate seed coat from the unpatterned portions 1620 of the substrate illustrated in Fig. 16 resulting in the seed coat removed from portion 1710. For example, when the material of the patterned build up layer includes a palladium rich modified organic material obtained through laser activation of a palladium acetate laser activatable film, the wash may comprise a water wash.

[0072] Fig. 18 illustrates the result of electrolytic copper plating 1810 the substrate 1000 illustrated in Fig. 17. The copper plating selectively covers the copper traces, via walls and tie bars. With the selective copper plating, DFR and litho-patterning are not required. In this embodiment, this process benefits in the elimination of two-step copper plating (i.e., electroless then electrolytic). In this embodiment, electrolytic copper plating is performed directly on the laser activated build up surface in the build up layers. This is made possible by the fact that all copper features are electrically connected to the sacrificial copper panel used during the build up building process.

[0073] Fig. 19 illustrates a subsequent dielectric build up process performed on the substrate illustrated in Fig. 18. After the dielectric build up layer 1910 is completed, Fig. 20 illustrates the result of laser via drilling the built up layer forming a plurality of vias 2010. Fig. 21 illustrates the result of dip coating the substrate illustrated in Fig. 20 with a palladium solution that seeds the substrate surface 2110. Fig. 22A illustrates the result of laser activating the surface of the substrate illustrated in Fig. 21. As illustrated, reference 2210 shows an activated via wall and reference 2230 shows an activated via bottom. Reference 2220 show a non-activated portion. Thus it is seen that the patterned activation selectively activates portions of the seed coat. Fig. 22B illustrates a top plan view of the substrate illustrated in Fig. 22A.

[0074] Fig. 23A illustrates the result of washing the palladium solution seed coat from the unpatterned portions 2310 of the substrate

illustrated in Fig. 22A. Fig. 23B illustrates a top plan view of the substrate illustrated in Fig. 23A.

[0075] Fig. 24A illustrates a subsequent dielectric build up process performed on the substrate illustrated in Fig. 23A. After the dielectric build up layer 2410 is completed laser trace ablation is performed on the built up layer as illustrated in Fig. 25 where traces 2510 are formed. As illustrated, a plurality of Fig. 26 illustrates the result of controlled-collapse-chip-connect (C4) solder ball (e.g., 2610) and first level interconnect (FLI) (e.g., 2710) bumping.

[0076] Fig. 27 illustrates the substrate of Fig. 26 having a sacrificial copper plate etched away to form copper protrusions 2800.

[0077] In another embodiment, after the dielectric build up (see Fig. 13), laser ablation for forming trace and tie bars (if desired), laser via drilling/ablation (see Fig. 14) and dip coating (see Fig. 15), laser assisted metallization of the substrate is performed (see Figs. 4A-B). After the laser assisted metallization activates the organic material selectively using the same projection mask (i.e., to embed the plating seed into the polymeric surface), the substrate is washed as in Fig. 17. In this embodiment, after the substrate is washed, electroless plating is performed on the substrate. Fig. 28 illustrates the result of electroless plating 2810 on the substrate after washing.

[0078] Fig. 29 illustrates the result of via filling and/or electrolytic plating the substrate with copper 2910. The need for chemical mechanical polishing (CMP) is eliminated in this embodiment as the copper plating only takes place in the selectively metallized region where the laser irradiation impinges.

[0079] In another embodiment, after dielectric build up (see Fig. 13), laser micro-via drilling/ablation (see Fig. 14), dip coating (see Fig. 15), laser

assisted metallization of the substrate, electroless plating (see Fig. 28) and via filling/plating (see Fig. 29), palladium DFR lamination 3010 is applied to the substrate. The result is illustrated in Fig. 30. In this embodiment, after the palladium DFR lamination of the substrate trace laser ablation and laser assisted metallization are performed on the substrate. The result is illustrated in Fig. 31 that shows trace 3110 and laser assisted metallization layer 3120.

[0080] Fig. 32 illustrates the result of performing trace electroless plating of copper 3210 on the substrate illustrated in Fig. 31. After the trace electroless plating, in this embodiment trace electrolytic plating 3310 is applied to the substrate. The result is illustrated in Fig. 33. The substrate is then DFR stripped as the result illustrates in Fig. 34. This embodiment eliminates a need for a CMP step as a laser is used to selectively metallize the build up layers following the same pattern used for ablation, and also for plating of tie bars.

[0081] The embodiments discussed above and illustrated in Figs. 10-34 may also be placed as a printed circuit board in a system, such as system 90 discussed above and illustrated in Fig. 9.

[0082] Some embodiments can also be stored on a device or machine-readable medium and be read by a machine to perform instructions. The machine-readable medium includes any mechanism that provides (i.e., stores and/or transmits) information in a form readable by a machine (e.g., a computer, PDA, cellular telephone, etc.). For example, a machine-readable medium includes read-only memory (ROM); random-access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; biological electrical, mechanical systems; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.). The device or machine-readable medium may include a micro-electromechanical system (MEMS), nanotechnology devices, organic, holographic, solid-state memory device and/or a rotating magnetic

or optical disk. The device or machine-readable medium may be distributed when partitions of instructions have been separated into different machines, such as across an interconnection of computers or as different virtual machines.

[0083] While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.

[0084] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may", "might", or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the element. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

What is claimed is:

1. A method comprising:
 - laser projection patterning a metal panel of a substrate;
 - laminating a dielectric layer on the metal panel;
 - laser irradiating the substrate to form a plurality of vias in the substrate;
 - laser activating a seed coat on the substrate to form activated seed coat portions and unactivated seed coat portions;
 - washing the unactivated seed coat portions from the substrate to yield a patterned build-up layer on the activated seed coat portions on the substrate; and
 - after washing the unactivated seed coat portions, forming a conductive layer on the activated seed coat portions.
2. The method of claim 1, further comprising:
 - dip coating the substrate in a seeding solution to provide the seed coat.
3. The method of claim 1, further comprising:
 - electrolytic plating a metal selectively on traces and the plurality of vias on the patterned build-up layer according to a predetermined interconnect pattern to yield interconnects, wherein a sacrificial copper plating is used to provide an electrical connection for the electrolytic plating.
4. The method of claim 3, further comprising:
 - electrolytic metal plating the traces.
5. The method of claim 3, further comprising:
 - palladium dry film resist lamination; and
 - dry film resist stripping the substrate.
6. The method of claim 1, further comprising:
 - performing laser assisted metallization before the washing the seed coat, and
 - providing a patterned conductive layer on the patterned-build-up-layer-substrate combination according to the predetermined interconnect pattern by electrolessly plating

the patterned-build-up-layer-substrate combination to yield an electrolessly plated substrate.

7. The method of claim 1, wherein the seed coat comprises palladium acetate.

8. The method of claim 1, wherein the build-up layer comprises a palladium seeded organic build-up layer.

9. The method of claim 1, wherein laser projection patterning further comprises drilling a plurality of micro vias.