Production of a Structure Comprising a Protective Layer against Chemical Treatments

Technical Field

The present invention relates to the production of a structure intended for electronics, optics or optoelectronics comprising a buried layer, the production of the structure comprising a chemical treatment employing chemical species liable to etch the buried layer.

In this document, the term buried layer will be applied to any layer contained in a structure and having material above and below it in this structure, with material properties substantially different from those of the adjoining material.

Prior Art

The contemporary structures intended for electronics, optics or optoelectronics are principally intended to be semiconducting, often comprising such layers, for instance SOI (silicon on insulator) structures in which the buried layer is an electrically insulating layer, for example a layer of SiO_2 or Si_3N_4.

The production of these structures or wafers frequently uses at least one of the following techniques: epitaxy, bonding between wafers, removal of thin layers.

These techniques for producing structures are usually implemented posteriorly, at the same time as and/or after chemical treatments employed for various reasons (such as cleaning the wafer or chemically etching one or more layers).

In certain cases, however, these chemical treatments may impair the quality of the structure which is produced, in particular by managing to etch

one or more layers which are buried in it.

Even if, by definition, a buried layer does not seem to have any contact with the exterior of the structure in which it is buried (and therefore does not have access paths for the chemical species) this is not always in fact true, particularly in cases where:

- it has a contact with the exterior at the level where it is flush with the edge of the structure;
- it underlies a thin layer whose surface is in contact with the exterior, and which comprises a number of defects that may constitute as many access paths for the chemical etching species to the buried layer, these defects being for example penetrating defects, contaminants, precipitates, etc.

These intrinsic etching problems of the layers buried in structures are encountered particularly in cases where these structures have a particularly thin layer at the surface and on the buried layer, typically of the order of a few tens of nanometers, in which case the presence of defects in these thin layers may have dramatic consequences on the quality of the final structure obtained, when said chemical etching species are employed.

This problem is encountered particularly in the chemical treatment, based on hydrofluoric acid HF, of SOI (silicon on insulator) structures customarily comprising a particularly thin useful layer of silicon on a layer of SiO_2, and a substrate conventionally of silicon, such HF etching being used in particular for deoxidation after an oxidizing heat treatment, for example.

If the silicon layer has defects such as those mentioned above, the buried SiO_2 layer risks being etched by the HF solution.

A defect of about 100 nanometers or more in such a silicon layer may for instance give access to

the buried layer, which, under the effect of the chemical species, may lead to the formation of holes in the oxide layer measuring several microns or even tens of microns in diameter, these holes also being referred to as "decorations" (see for example Figure 2).

The defects in useful layer, also referred to as HF defects, can therefore have a dramatic effect on the quality of the buried layer and on the entire structure, which is why the person skilled in the art defines these HF defects to be "killer" defects.

The presence of HF defects in proximity to a buried SiO_2 layer can cause damage to an even greater extent in the case of detachable substrates.

Ways of producing detachable substrates by controlling the bonding energy are described particularly in patent FR 2 823 599, the production principle being based on reducing the bonding forces between a substrate and a wafer (or a thin layer) which are bonded together, with respect to optimal bonding, by creating a weakened zone therein, the substrate-wafer (or layer) assembly forming the detachable substrate.

In the case of an HF treatment of a detachable substrate, and when such a weakened zone lies in a buried thickness of SiO_2, several problems of etching the buried SiO_2 may arise, particularly if:

- the bonding energy has not been controlled optimally enough, for example being too weak, leading to edge delamination problems, that is to say disbonding problems of silicon grains which lie at the periphery of the layer (see for example Figure 5); or if

- HF defects are present in the layer underlying the buried thickness of SiO_2, decorations then being created in these buried layers under the effect of the HF species. Because of the bonding imperfections that exist in the weakened zone, these decorations tend to be greater than in the case of

optimal bonding. These decorations may, for instance, be from 10 to 100 times more than in the case of a non-detachable substrate; the thin layer which lies above the decorations then risks losing some of its rigidity and tearing, which may lead to the presence of particles on the wafer and therefore to contamination problems during the subsequent processes in SOI structures, detachable substrates or other structures (see for example Figure 7).

In order to attempt to overcome these problems of chemical attack of buried layers, an improvement in the quality of the useful layers has been sought by reducing the defect density therein, thus giving less possible access to the buried oxide.

Other techniques in development tend, during the chemical treatments implemented, to employ chemical species which are less aggressive vis-à-vis the buried layer.

Summary of the Invention

Embodiments of the present invention seek to offer a solution to the problem posed by chemical attack of the buried layers. According to a first aspect of the present invention, there is provided a method for producing a structure with a plurality of layers intended for electronics, optics or optoelectronics comprising a buried layer, the method comprising the following steps:

a. formation of layers of the structure, comprising the formation of the buried layer;

b. chemical treatment of the structure, employing chemical species liable to etch substantially the material constituting the buried layer;

characterized in that step a comprises the formation on the buried layer of a protective layer, itself also buried, of a material selected to withstand sufficiently the chemical attack of chemical species of

the treatment employed during step b), thus blocking possible accesses to the buried layer through which these species could infiltrate.

Other characteristics according to example embodiments of the invention are:

- step a) may comprise bonding of two wafers;

- step a) may comprise, before bonding, the formation of the layer to be buried and of the protective layer at the surface of at least one bonding surface of one wafer;

- step a) may comprise, before bonding, the formation of the layer to be buried on the bonding surface of one of the two wafers and the formation of the protective layer on the bonding surface of the other wafer;

- step a) may comprise, after bonding, a reduction of one of the two wafers by means of one of the following techniques: Smart-Cut®, detachment level with a porous layer buried in the wafer to be reduced, lateral selective chemical attack of a layer, lapping, polishing, CMP, chemical etching, abrasion; so that only a thin layer above the protective layer remains of the reduced wafer;

- the structure formed according to step a) may be a semiconductor-on-insulator structure, the buried layer being at least a part of the insulating thickness of this structure;

- the protective layer may also be contained in the insulating thickness of the structure;

- the structure formed according to step a) may have a weakened zone;

- the weakened zone may be an interface between two layers, at least one of the two layers having a rough surface;

- step a) may comprise, before bonding, the formation of a weakened zone on one of the bonding surfaces of the wafers by chemical roughening.

According to a second aspect of the present invention, there is provided an application of said method to the

production of a detachable structure.

According to a third aspect of the present invention, there is provided an application of said method to the production of a semiconductor-on-insulator structure.

Presentation of the Figures

Figure 1 represents a set of two wafers bonded together, showing a step of a method for forming an SOI structure.

Figure 2 represents an SOI structure according to the prior art.

Figure 3 represents an SOI structure according to the invention.

Figure 4 represents a detachable substrate.

Figure 5 represents a detachable substrate according to the prior art.

Figure 6 represents a substrate according to the invention.

Figure 7 represents a detachable SOI structure according to the prior art.

Figure 8 represents a detachable SOI structure according to the invention.

Figure 9 represents a set of two bonded wafers during a step of producing a specific structure, one of the two wafers being a detachable substrate.

Detailed Description of the Invention

It is a principal object of the present invention to reduce the number and size of etching defects of a layer buried in a given structure, when the latter undergoes chemical treatments liable to etch the material of the buried layer.

When a buried layer is etched, the etching takes place locally and extends over delimited zones associated with features of surrounding structures, which may constitute access paths for chemical etching

species to the buried layer.

Etching of the buried layer is principally due to:

i) the presence of defects in proximity, particularly when the buried layer underlies a thin layer;

ii) strong action of the etching solution on the structure by:
- long exposure;
- strong dosing of the chemical species liable to etch the material of the buried layer.

As regards the first cause (i) for etching of the buried layer, it is principally encountered in the case where a particularly thin layer has one of its surfaces in contact with the buried layer and the other of its surfaces in contact with the exterior.

This is because even a minor defect in such a thin layer, which may amount to a few tens of nanometers, can represent an access path for the etching species to the buried layer.

The natures of these defects vary:

They may, for example, be defects penetrating through the thin layer, thus providing direct access to the buried layer.

These penetrating defects may have various causes, in particular associated with the process of producing the thin layer and the quality of its constituent material.

It is known, for example, that an epitaxially grown layer contains few defects of this type, and therefore presents a lower risk of damaging the buried layer underlying it during the chemical etching treatment.

However, techniques for producing other layers in other cases require production by moving layers from a donor substrate to a target substrate.

This is, in particular, the case with the

methods for fabricating SeOI (semiconductor-on-insulator) structures, in which case the thin layer of semiconductor material cannot be produced on the insulating layer by epitaxy.

These techniques of moving or transferring thin layers typically generate ten times more defects than when epitaxy is employed.

The structures then present buried layer etching problems.

Referring to Figure 1, a technique of transferring layers from a donor substrate 6 to a receiver substrate 1 conventionally comprises two main steps:

- bonding of the two substrates 1 and 6 level with a bonding interface 5;
- reduction of the donor substrate 6 in order to finally provide a substrate comprising the receiver substrate 1 and a thin layer, which is the remaining part of the donor substrate 6.

The bonding may be carried out by molecular adhesion.

Particularly powerful surface preparations to improve the bonding energy between the substrates 1 and 6 may be employed, for example exposing the surfaces to be bonded to a plasma (for example oxygen), cleaning, brushing.

Forming may thus be provided prior to the bonding of the bonding layers 2 and 3, level with at least one of the two surfaces to be bonded, followed by suitable heat treatment, for example applying thermoset adhesives or adhesives which can be set by application of UV radiation on the surfaces to be bonded, or forming oxide layers.

The donor substrate 6 may be reduced by progressively eliminating the donor substrate by polishing and/or chemical etching via the rear face (more familiar to the person skilled in the art under

the process name "etch-back" technique), or by separating the thin layer 4 from the donor substrate 6 level with a previously weakened zone 15 by applying thermal and/or mechanical energy; this weak zone 15 is advantageously produced by controlled implantation of atomic and/or molecular species level with it (these are referred to as Smart-Cut techniques) or by rendering a surface porous level with it.

These wafer production techniques cause defects to appear in the thin layer 4 being produced, for instance penetrating defects.

A particle removed from the surface of the donor wafer 6 during polishing may, for example, cause damage in the thickness by abrading the thin layer 4 which is formed.

Chemical etching during an etch-back process may etch the surface of the donor wafer 6 unevenly, for example, so that the layer buried under the thin layer 4 becomes exposed at certain positions.

The layer 4 formed on a porous weak layer 15 may present point defects accentuated by the subsequent treatment of removing the porous layer after detachment.

The techniques for finishing the thin layer 4 obtained after reducing the donor wafer 6, which are advantageously employed, may also give rise to the appearance of penetrating defects.

The following finishing techniques may be mentioned by way of example: polishing, chemical etching, abrasion, bombardment with atomic species, sacrificial oxidation.

Other defects such as metal contaminants, aggregates, oxygen precipitates, metal precipitates or stacking faults may nevertheless remain in the thin layer at the surface, and help chemical etching species to infiltrate the structure as far as the buried layer.

The problems which these defects may pose in conventional SeOI structures, and the solutions

provided by the present invention in order to resolve them, will be described with reference to Figures 2 and 3.

Referring to Figure 2, an SeOI structure 10 according to the prior art is presented, that is to say one consisting of a support substrate 1, a buried insulating layer 2 and a thin layer of semiconductor material 4.

This SeOI structure is produced, for example, according to a production method described above with reference to Figure 1, the bonding interface 5 lying inside or at the surface of the buried layer 2.

In this context, several variants of bonding techniques may be found in the book "Semiconductor Wafer Bonding Science and Technology" (Q-Y. Tong and U. Gösele, a Wiley Interscience publication, Johnson Wiley & Sons, Inc.).

This structure 10 contains defects in the thin layer 4, such as those giving access for chemical etching species to the buried layer 2.

For the sake of simplicity in the figures, the defects 16 and 16' have been represented as being penetrating defects, although it must of course be understood in this schematic figure that these defects may be of any other type, for example impurities as already mentioned.

Referring to Figure 2, the presence of the defects 16 and 16' in the thin layer 4 will allow the chemical species to reach the buried layer 2 level with the interfaces of the layers 2 and 4, locally etch the buried layer and thus form cavities 17, 17', respectively, also referred to as decorations 17 and 17'.

Principally, this type of thin layer 4 is intended to receive components and the buried insulating layer 2 is intended to impart certain properties to these future components, in which case the presence of these decorations 17 and 17' may be

detrimental to the quality of these future components.

Such problems may arise, for example, in an SeOI structure for which the buried insulating layer 2 is of SiO_2 and the chemical treatment which it undergoes employs a chemical solution comprising hydrofluoric acid HF.

These HF chemical treatments are commonly employed in the field of semiconductors, especially in the case where it is desirable to carry out final deoxidation of the surfaces of the structure 10 obtained, for example, after the use of oxidizing heat treatments.

Exposure of this structure 10 presenting the defects 16 and 16' to hydrofluoric acid etching then causes the decorations 17 and 17' in the buried SiO_2 2.

Owing to the ability which HF has to propagate along a non-stabilized interface, such as the interface between the layer 2 and the layer 4 level with the defect 16, the decorations 17 and 17' can reach sizes much larger than the size of the defects 16 and 16' which respectively initiated their formation.

For defects 16 and 16' of the order of from 0.1 to 1 micron in average diameter, HF chemical treatment can thus create defects of several microns, or even about ten microns in average diameter, in the buried layer SiO_2 2.

This is why these so-called "HF" defects are classed in the family of "killer" defects by the person skilled in the art, because they can irreversibly destroy a significant part of an SeOI structure 10.

Referring to Figure 3, a way according to the invention of protecting the buried layer 2 from a chemical etching treatment is proposed.

To this end, a layer or a coating is placed between the buried layer 2 and the thin layer 4.

This protective layer 3 is made of a material which is etched less or not at all by the chemical species employed during a chemical treatment which the

structure 10 undergoes, and in particular by the chemical species liable to etch the buried layer 2.

This protective layer 3 may be produced according to said aforementioned techniques for producing thin layers, or according to other techniques.

For example, it may be produced by epitaxy if it consists of a crystalline material, or by deposition of atomic species on a surface.

The primary function of this protective layer 3 is to protect the buried layer 2 against chemical attack.

Its constituent material and its thickness are therefore selected above all so that it presents a significant resistance to etching by the chemical species.

The protective layer 3 should furthermore therefore have a thickness greater than the minimum thickness below which it can present risks of being etched too much in its thickness.

The structure 10 is advantageously produced according to one of the techniques described above with reference to Figure 1, by means of one of the bonding techniques which were listed there.

The layer 2 to be buried and/or the protective layer 3 are then formed before bonding.

In a first configuration, they are already contained in the wafers to be bonded, for example during prior epitaxial growths.

In a second configuration, they are advantageously formed on the bonding surfaces of the wafers to be bonded.

Preferably, the buried layer 2 is formed at the surface of the first wafer to be bonded and the protective layer 3 is formed at the surface of the second wafer to be bonded.

These two layers 2 and 3 may thus be used as bonding layers, in addition to their first functions.

Referring to Figure 3, the thin layer 4 is identical to that of Figure 2 and it presents the same defects 16 and 16'.

But in contrast to the discussion above with reference to Figure 2, since the protective layer 3 is attacked little or not at all by the chemical species that can etch the buried layer 2 and the infiltration of the chemical species takes place through the thin layer level with the defects 16 and 16', the latter do not reach the buried layer 2.

The protective layer 3 thus very substantially reduces or prevents contact of the buried layer 2 with the infiltrated chemical species.

This result is obtained without attempting to improve the quality of the thin layer 4 (which has as many defects 16 and 16'), in contrast to the techniques employed in the prior art.

This technique is also obtained without modifying the chemical composition of the treatments which the structure 10 undergoes, in contrast to the prior art.

In a preferred configuration of the structure 10, it is an SeOI structure for which the buried layer 2, and optionally the protective layer 3, are made of an electrically insulating material and therefore constitute an insulating thickness of the SeOI structure.

The production of such an SeOI structure is advantageously carried out according to one of the techniques described above with reference to Figure 1.

The bonding 5 has preferably been carried out between the donor substrate 6 and the receiver substrate 1, respectively covered with the protective layer 3 and the buried layer 2.

In the case where the latter bonding technique is employed, further to consisting of a material which is etched little or not at all by the chemical species that can etch the buried layer 2, the protective layer

3 should have bonding performances substantially identical to those of the buried layer 2 so that they can adhere together, for instance bonding energies, flow properties and/or thermal expansion coefficients which are substantially similar.

In comparison with the example taken with reference to Figure 1 of an SeOI 10 whose insulating layer 2 is an SiO_2 layer, between the thin layer 4 and the insulating layer 2 an SeOI structure 10 according to the invention furthermore comprises a protective layer 3 which may be of a semiconductor material or an electrically insulating material.

Advantageously, the material of the protective layer 3 is an electrically insulating material and, with the buried SiO_2 layer, constitutes the insulating thickness of the SeOI 10.

This protective layer 3 of insulating material may preferably be Si_3N_4, SiON or diamond according to the invention.

This protective layer 3 is of Si_3N_4 according to a preferred configuration of the invention, this material having bonding properties approximately equivalent to the bonding properties of SiO_2 in terms of the bonding energy and transfer quality, particularly in the case of using a Smart-Cut method, referring for example to the document entitled "From SOI to SOIM Technology: application for specific semiconductor processes" by O. Rayssac et al. (in SOI Technology and Devices X, PV 01-03 ecs Proceedings, Pedington, and J (2001)).

The other main benefit of using a nitride for the protective layer 3, however, resides in its strong resistance to chemical treatments such as hydrofluoric acid treatments.

This silicon nitride may be obtained, for example, by nitriding or by depositing a nitride layer by CVD on the surface of the donor substrate 6.

The layer 2 to be buried will then

advantageously be obtained by oxidizing the surface of the receiver substrate 1.

As regards said cause ii) (mentioned above in this document) for etching of the buried layer 2, a structure 10 for which long explosion to chemical etching species, and/or strong dosing of these chemical etching species, leads to etching of the buried layer 2 is described below.

This structure 10 is a detachable structure as defined particularly in document FR 2 823 599.

A detachable structure consists of two wafers bonded together and is rendered detachable by controlling how the bonding of these two wafers can take place, and in particular the bonding energy.

These detachable structures are principally used as provisional substrates for the growth and/or fabrication of layers or components before these layers and/or components are transferred onto receiver substrates.

Finally, it is thus possible to produce a structure having a receiver substrate which, without using this detachable structure technique, could only with difficulty or not at all have been used as a substrate for producing these transferred layers or components.

Detachable structure applications are found, for example, in the field of light-emitting diodes in which, for example, a detachable sapphire substrate for producing epitaxial stacks is removed by detachment, the stacks then being transferred to another substrate which is less electrically insulating.

Likewise in telecommunications and microwave frequencies it is preferable for the components to be finally integrated on a support presenting a higher resistivity.

In some cases, the substrate necessary for producing certain structures or components costs an excessive amount. This is the case, for example, with

silicon carbide which is much more expensive than silicon but exhibits stability in particular at higher temperatures, and significantly improved powers and maximum working frequencies, and the cost of which is very high compared to silicon. It would therefore be beneficial for a fine layer of silicon carbide, grown epitaxially on a sapphire substrate, to be transferred onto an inexpensive substrate such as silicon.

Applications of the detachable structure may also be mentioned in the power field or in the field of chip cards.

Referring to Figure 4, a detachable substrate 10 consists of a support substrate 1 connected in a controlled way to a transfer structure 6 by means of a weakened zone 20.

This weakened zone 20 may be created in particular by roughening the surface of the detachable substrate 1, and optionally the transfer structure 6, by chemical treatment before the support substrate 1 and the transfer structure 6 are bonded, as described particularly in document FR 2 823 599.

The weakening level with the zone 20 depends principally on the chemical budget (identifying the threefold factor of chemical species doping/times/temperature) used, which determines the weakening finally obtained or, which equates to the same thing, the loss of bonding energy level with the weakened zone 20.

The loss of bonding energy level with the weakened zone 20 is associated with the surface roughness, which reduces the contact bonds between the detachable substrate 1 and the transfer substrate 6.

By altering the roughness, it is thus possible to control the bonding energy of the detachable substrate 1.

For SiO_2/SiO_2 bonding in which the two layers have each been roughened by 8000 Å via HF etching, leading to a roughness of the order of 0.625 nanometer

rms for each surface, the bonding energy is of the order of 500 mJ/m^2 instead of about 2 J/m^2 as conventionally encountered for SiO_2/SiO_2 bonding which has not undergone roughening, this result being taken from the article entitled "Proceedings of the 2nd International Conference on Materials for Microelectronics" (IOM communication page 183, 1998) by Olivier Rayssac et al.

After roughening the surface of the support substrate 1, the transfer structure 6 is bonded onto the support substrate 1 by one of the techniques described above in order to obtain the detachable structure 10.

Treatments may then optionally be carried out in the transfer structure 6, for example in order to produce some or all of the components.

In a next step, this transfer structure 6 is detached from the support structure 1 level with the weakened zone 20, in particular by applying stresses of mechanical type, such as inserting a blade level with the zone 20 or using a detachment pincer or a gas or liquid flow jet.

Nevertheless, it may happen that damage occurs level with the zone 20 or certain other fragile positions of the detachable structure 10 during the detachment, particularly if mechanical forces are exerted in order to assist detachment.

In order to avoid this, a structure and a detachment method are proposed with reference to Figure 5.

This detachable structure 10 is composed of a support substrate 1 comprising a layer 2 at the surface, and a transfer structure 6 comprising a layer 2' at the surface, the weakened zone 20 being the interface of the layers 2 and 2', produced according to one or other of the two techniques described above with reference to Figure 4.

The layers 2 and 2' consist of the same

material.

During or at the end of the production process (for example of components), the entire detachable structure 10 then undergoes a chemical treatment comprising chemical species liable to etch the layers 2 and 2'.

The chemical action of these species is made particularly strong by using at least one of the following two methods:

- long exposure of the detachable structure 10 to the chemical species,
- particularly strong dosing of the chemical species.

The effect of the chemical treatment is then to locally hollow the layers 2 and 2', level with where they are flush with the edge of the detachable structure 10.

The hollows 18 and 18' thus formed will accentuate the weakness of the weakened zone 20, but will above all act as an initiator for the detachment level with the zone 20 when the mechanical forces are applied.

This chemical preparation for the detachment is particularly expedient to overcome said wafer detachment problems.

Edge delamination problems, however, that is to say problems of detachment of materials belonging to the transfer structure 6 and/or the support substrate 1, may then prejudice the electronic or optoelectronic components which are finally intended to be obtained.

Referring to Figure 5, such delamination zones can be seen at 19, 19', 19'' and 19'''.

The example of a detachable substrate 1 whose oxidized surface 2 is subsequently roughened and finally bonded to a transfer substrate 6, itself also previously oxidized at the surface 2'', may for example be mentioned.

The layers 2 and 2' are then SiO_2 layers, for

oxidations taking place on silicon.

In the latter case, the detachable structure 10 may then be subjected to an HF treatment in which the hydrofluoric acid dosing is around 50%, and therefore particularly high in concentration, the effect of which is to laterally etch the SiO_2 layers 2 and 2' to be bonded.

The delamination zones 19, 19', 19'' and 19''' are then silicon delaminations of the transfer substrate 6 and of the support substrate 1.

Referring to Figure 6, a solution to the problem mentioned above is found by virtue of a structure and a method according to the invention.

The detachable structure 10 is constructed in the same way as the detachable structure 10 described in detail above with reference to Figure 5, with the exception that the layer 2' is replaced by a protective layer 3 of a material substantially different than the material of the layer 2.

The material of the protective layer 3 is selected so that the chemical species which are added during the chemical treatment, and which are liable to etch the buried layer 2, cannot etch it.

When the detachable structure 10 is subjected to a chemical treatment, only the layer 2 is therefore laterally etched.

This greatly limits the amplitude of the lateral attack, because only one of the two buried layers is etched substantially, while maintaining a property of initiating the detachment of the support substrate 1 from the transfer substrate 6.

The delamination level with the support substrate 1 is then minor.

There is no edge delamination level with the interface between the transfer structure 6 and the protective layer 3.

In comparison with the detachable structure 10 already discussed above with reference to Figure 5,

comprising two interface layers 2 and 2' of SiO_2, the example illustrated in Figure 6 comprises a layer of Si_3N_4 instead of the layer 2' of SiO_2.

This detachable substrate 10 is advantageously obtained by bonding between the support substrate 1, previously oxidized level with its silicon surface in order to give the oxide layer 2, and the transfer structure 6 previously covered with an Si_3N_4 deposit (for example by PECVD or LPCVD) level with its silicon surface in order to give the nitride layer 3.

In a first exemplary case, the weakened zone 20 is obtained by roughening the oxide layer 2 before bonding, by HF etching.

In a second exemplary case, the weakened zone 20 is obtained by roughening the nitride layer 3 before bonding, for example by etching with H_3PO_4 at 140°C, by dry etching with the aid of ballistic and/or chemical means such as RIE (abbreviation for "Reactive Ion Etching").

In a third exemplary case, the weakened zone 20 is obtained by roughening the layer 2 of SiO_2 and the layer 3 of Si_3N_4.

Referring to Figures 7, 8 and 9, the case is discussed of a chemical treatment on detachable SeOI structures 10, comprising a support substrate 1 adjacent to an insulating thickness in which the weakened zone 20 has been created, thus separating the insulating layer consisting of the two layers 2 and 2', and finally the thin layer 4 of the SeOI structure has been created.

Similarly as discussed above with reference to Figure 2, a particularly thin layer presenting defects can let chemical species of a chemical treatment penetrate through its defects, and allow them to etch the buried insulating thickness 2 and 2'.

Similarly as Figure 5, a particularly active chemical treatment due to:

- either long exposure of the detachable

structure 10 to the chemical species,

- or strong dosing of the chemical species,

will create an annular cavity in the structure 10 level with weakened zone 20.

Referring to Figure 7, the problems mentioned separately in the preceding exemplary cases are cumulative here, that is to say appearance of decorations within the buried layer 2-2' and edge delamination at 19 and 19' of the thin layer 4 and the detachable substrate 1.

In the case of a detachable SeOI, however, the decorations are larger in size than in the case of a non-detachable SeOI, because the weakened zone 20 has hollow parts (due to interfacial roughnesses obtained during the weakening by surface roughening) in which the chemical etching species will be introduced and attack the walls of these hollow parts.

In the case of a detachable SeOI according to the prior art, the etching by the chemical species can thus lead to typical decorations 10 to 100 times larger than in the case of a non-detachable SeOI.

Referring to Figure 8, a solution which the invention proposes is for a coating or a protective layer 3, the constituent material of which is etched little or not at all by the chemical species liable to etch the buried layer 2, to be inserted into the structure 10.

This protective layer 3, likewise as with reference to Figure 3, isolates the buried layer from the defect 16 and therefore substantially prevents etching of the buried layer "from the inside".

Owing to the reduction of the intermediate thickness between the thin layer 4 and the detachable substrate 1, the annular hollow 18' is smaller in size than that referred to in Figure 7, the edge delamination of the detachable substrate then being small or nonexistent, that of the thin layer 4 being substantially zero, and with the annular hollow

nevertheless maintaining the property of initiating detachment level with the weakened zone 20 when mechanical detachment forces are subsequently applied.

One application of such a detachable SeOI structure consists in producing electronic or optoelectronic components in the thin layer 4.

This structure 10 may be particularly beneficial in the case where these component layers are produced at high temperatures which few substrates can withstand.

Referring to Figure 9, the layer 4 can then be moved onto a transfer structure 6 by:

- bonding this transfer structure 6 to the layer 4; then by
- detaching the assembly level with the weakened zone 20; and finally by
- removing the protective layer 3.

A final structure containing a thin layer 4 present on a transfer structure 6 is thus obtained.

The substrates 1 and 6 discussed in this document, and particularly with reference to Figures 1 to 9, may be of silicon, germanium, SiGe, IV-IV alloy, III-V alloy, II-VI alloy, sapphire, SiC or any other material which can be employed by the present invention.

The thin layers 4 discussed in this document, and particularly with reference to Figures 1 to 3 and 7 to 9, may be of Si, Ge, SiGe, III-V alloy, II-VI alloy, SiC or other materials.

The buried layers 2 are advantageously of SiO_2, but may also be of another type of insulator or another type of material which can be etched substantially by chemical species employed during the chemical treatment of the structures 10.

The buried protective layer 3 is advantageously of Si_3N_4 in the particular case where the buried layer 2 is of SiO_2, although it may also be of SiON, diamond or other types of material liable to be etched little or

not at all by the chemical species, which are employed during the treatment of the structure 10 and are liable to etch the buried layer 2.

This invention applies not only to the production of an SeOI structure, but to any other production of structures for electronics, optics or optoelectronics.

CLAIMS

1. A method for producing a structure with a plurality of layers intended for electronics, optics or optoelectronics comprising a buried layer, the method comprising the following successive steps:

a. formation of layers of the structure, comprising the formation of the buried layer;

b. chemical treatment of the structure employing chemical species liable to etch substantially the material constituting the buried layer;

characterized in that step a) comprises the formation on the buried layer of a protective layer, itself also buried, of a material selected to withstand sufficiently the chemical attack of chemical species of the treatment employed during step b), thus blocking possible accesses to the buried layer through which these species could infiltrate.

2. The method as claimed in claim 1, characterized in that step a) comprises bonding of two wafers.

3. The method as claimed in claim 2, characterized in that step a) comprises, before bonding, the formation of the layer to be buried and of the protective layer at the surface of at least one bonding surface of one wafer.

4. The method as claimed in claim 2, characterized in that that step a) comprises, before bonding, the formation of the layer to be buried on the bonding surface of one of the two wafers and the formation of the protective layer on the bonding surface of the other wafer.

5. The method as claimed in one of the three preceding claims, characterized in that step a) comprises, after bonding, a reduction of one of the two wafers by means of one of the following techniques: Smart-Cut®, detachment level with a porous layer buried in the wafer to be reduced, lateral selective chemical attack of a layer, lapping, polishing, CMP, chemical etching, abrasion;

so that only a thin layer above the protective layer remains of the reduced wafer.

6. The method as claimed in the preceding claim, characterized in that the structure formed according to step a) is a semiconductor-on-insulator structure, the buried layer being at least a part of the insulating thickness of this structure.

7. The method as claimed in the preceding claim, characterized in that the protective layer is also contained in the insulating thickness of the structure.

8. The method as claimed in one of the preceding claims, characterized in that the structure formed according to step a) has a weakened zone.

9. The method as claimed in claim 8, characterized in that the weakened zone is an interface between two layers, at least one of the two layers having a rough surface.

10. The method as claimed in one of claims 2 to 7 combined with the preceding claim, characterized in that step a) comprises, before bonding, the formation of a weakened zone on one of the bonding surfaces of the wafers by chemical roughening.

11. The method as claimed in one of the preceding claims, characterized in that the buried layer is of SiO_2.

12. The method as claimed in one of claims 2 to 10, characterized in that the buried layer is of SiO_2 and was formed during step a) by oxidation of a silicon surface of one of the two wafers to be bonded.

13. The method as claimed in one of the two preceding claims, characterized in that the chemical species employed during step b) are based on hydrofluoric acid.

14. The method as claimed in one of the three preceding claims, characterized in that the protective layer consists of a nitride material.

15. The method as claimed in one of claims 2 to 14, characterized in that the protective layer is of

nitride and was formed during step a) by nitride deposition level with a bonding surface of one of the two wafers to be bonded.

16. The method as claimed in one of the two preceding claims, characterized in that the protective layer consists of Si_3N_4.

17. An application of the method as claimed in one of claims 8 to 10 to the production of a detachable structure.

18. An application of the method as claimed in claim 6 or 7 to the production of a semiconductor-on-insulator structure.