CLAIMS

1. A memory, comprising a clock processing circuit, the clock processing circuit comprising:

a duty cycle module, configured to receive a data clock signal externally generated, and adjust a duty cycle of the data clock signal to output an internal clock signal;

a first clock generation module, configured to receive the internal clock signal, and output a first read clock signal based on the internal clock signal; wherein the first read clock signal is a pulse signal;

a second clock generation module, configured to generate and output a second read clock signal during existence of the first read clock signal; wherein the second read clock signal is a non-periodic signal having exactly one level state change edge that indicates an end time of valid data in the read data signal; and

a selection module, configured to receive a selection indication signal, the first read clock signal and the second read clock signal, to output the first read clock signal as a target read clock signal in response to the selection indication signal being in a first state and to output the second read clock signal as the target read clock signal in response to the selection indication signal being in a second state differing from the first state.

2. The memory of claim 1, wherein the clock processing circuit further comprises a detection module and a mode register; wherein,

the detection module is configured to receive the internal clock signal, and detect a duty cycle of the internal clock signal to output a duty cycle parameter; and

the mode register is configured to receive and store the duty cycle parameter.

3. The memory of claim 2, wherein,

the memory is configured to receive a data read instruction; and output a read data signal based on the data read instruction, and output the target read clock signal through the clock processing circuit;

wherein the target read clock signal is used for latching the read data signal, and the level state change edge of the second read clock signal indicates an end time of valid data in

the read data signal.

4. The memory of claim 3, wherein,

the memory is further configured to set the selection indication signal to be in the first state in response to the data read instruction being a first read instruction; or, set the selection indication signal to be in the second state in response to the data read instruction being a second read instruction;

wherein the second read instruction instructs to obtain the duty cycle parameter in the mode register in the clock processing circuit, and the first read instruction is a data read instruction other than the second read instruction.

5. The memory of claim 4, wherein,

the memory is further configured to set the selection indication signal to be in the first state in response to the data read instruction being the first read instruction; or,

set the selection indication signal to be in the first state in response to the data read instruction being the second read instruction and the duty cycle of the internal clock signal being within a preset range; or,

set the selection indication signal to be in the second state in response to the data read instruction being the second read instruction and the duty cycle of the internal clock signal being not within a preset range.

6. The memory of any one of claims 1-5, wherein the first read clock signal comprises 8 clock cycles, and the level state change edge of the second read clock signal is aligned with a rising edge of a fifth clock cycle in the first read clock signal;

wherein the level state change edge of the second read clock signal is a change of the second read clock signal from a low level state to a high level state.

7. The memory of claim 6, wherein the duty cycle module comprises:

a receiving module, configured to externally receive and output the data clock signal; and

an adjustment module, configured to adjust the duty cycle of the data clock signal to output the internal clock signal.

8. The memory of claim 7, wherein the data clock signal is a write clock signal.

9. A control apparatus, the control apparatus being connected to a memory; wherein,

the control apparatus is configured to send a data read instruction to the memory; and receive a read data signal and a target read clock signal that are returned by the memory, and perform latch processing on the read data signal using the target read clock signal;

wherein the target read clock signal is a first read clock signal or a second read clock signal, the first read clock signal is a pulse signal, and the second read clock signal is a non-periodic signal having exactly one level state change edge that indicates an end time of valid data in the read data signal; wherein,

the control apparatus is configured to receive the first read clock signal returned by the memory in response to the data read instruction being a first read instruction, and perform latch processing on the read data signal using the first read clock signal; or,

receive the second read clock signal returned by the memory in response to the data read instruction being a second read instruction, and perform latch processing on the read data signal using the level state change edge of the second read clock signal;

wherein the memory comprises a clock processing circuit, the second read instruction instructs to obtain a duty cycle parameter in a mode register in the clock processing circuit, and the first read instruction is a data read instruction other than the second read instruction.

10. The control apparatus of claim 9, wherein,

the control apparatus is further configured to receive the first read clock signal returned by the memory in response to the data read instruction being a second read instruction, and perform latch processing on the read data signal using level state change edges of the first read clock signal.

11. A clock processing method, applied to a memory, the method comprising:

receiving a data clock signal externally generated; and adjusting a duty cycle of the data

clock signal to determine an internal clock signal;

determining a first read clock signal based on the internal clock signal; wherein the first read clock signal is a pulse signal;

generating a second read clock signal during existence of the first read clock signal; wherein the second read clock signal is a non-periodic signal having exactly one level state change edge that indicates an end time of valid data in the read data signal;

receiving a selection indication signal; and

outputting the first read clock signal as a target read clock signal in response to the selection indication signal being in a first state and outputting the second read clock signal as the target read clock signal in response to the selection indication signal being in a second state differing from the first state.

12. The clock processing method of claim 11, wherein the memory comprises a mode register, and the method further comprises:

detecting a duty cycle of the internal clock signal to obtain a duty cycle parameter; and

storing the duty cycle parameter into the mode register.

13. The clock processing method of claim 12, wherein the memory is connected to a control apparatus, and outputting the first read clock signal as a target read clock signal in response to the selection indication signal being in a first state and outputting the second read clock signal as the target read clock signal in response to the selection indication signal being in a second state differing from the first state comprises:

in response to receiving a first read instruction sent by the control apparatus, determining a read data signal based on the first read instruction, and determining the first read clock signal as the target read clock signal;

in response to receiving a second read instruction sent by the control apparatus, determining a read data signal based on the second read instruction, and determining the second read clock signal as the target read clock signal;

wherein the target read clock signal is used for latching the read data signal, the second

read instruction instructs to obtain the duty cycle parameter in the mode register, and the first read instruction is a data read instruction other than the second read instruction.

14. The clock processing method of claim 12, wherein the memory is connected to a control apparatus, and outputting the first read clock signal as a target read clock signal in response to the selection indication signal being in a first state and outputting the second read clock signal as the target read clock signal in response to the selection indication signal being in a second state differing from the first state comprises:

in response to receiving a first read instruction sent by the control apparatus, determining a read data signal based on the first read instruction, and determining the first read clock signal as the target read clock signal;

in response to receiving a second read instruction sent by the control apparatus and the duty cycle parameter being within a preset range, determining a read data signal based on the second read instruction, and determining the first read clock signal as the target read clock signal;

in response to receiving a second read instruction sent by the control apparatus and the duty cycle parameter being not within a preset range, determining a read data signal based on the second read instruction, and determining the second read clock signal as the target read clock signal;

wherein the target read clock signal is used for latching the read data signal, the second read instruction instructs to obtain the duty cycle parameter in the mode register, and the first read instruction is a data read instruction other than the second read instruction.

15. An electronic device, comprising the memory of any one of claims 1-8 and the control apparatus of any one of claims 9-10.