CLAIMS:

1. An integrated circuit device (100) comprising:

- a semiconductor substrate (101) having a resistivity of at least 100 Ω.cm;

- an electrically insulating layer (102) that contacts the semiconductor substrate, the electrically insulating layer being susceptible of inducing in the semiconductor substrate a parasitic surface conduction layer that interfaces with the electrically insulating layer; and

- an electrical circuit (103) located on the electrically insulating layer,

wherein the integrated circuit device comprises a plurality of depletion-inducing junctions (107) at least partially comprised in the semiconductor substrate, the plurality of depletion-inducing junctions being adapted to autonomously induce in the semiconductor substrate a plurality of depleted zones (301) that interface with the electrically insulating layer, whereby the depletion-inducing junctions are disposed in one of the following manners: an array-like manner and a checkerboard-like manner, and whereby at least some depletion-inducing junctions of the plurality interface with a section of the electrically insulating layer that lies in-between two sections (104, 105) of the electrical circuit.

2. An integrated circuit device according to claim 1, wherein at least one depletion-inducing junction (108, 109) among the plurality of depletion-inducing junctions (107) comprises a doped region (108) in the semiconductor substrate (101) near the electrically insulating layer (102), the doped region having polarity that is opposite to a polarity of free charge carriers in an adjacent region where a bulk section of the semiconductor substrate interfaces with the electrically insulating layer.

3. An integrated circuit device according to claim 2, wherein the at least one depletion-inducing junction (108, 109) comprises another doped region (109) in the semiconductor substrate (101) near the electrically insulating layer (102), the one and the other doped region interfacing with each other and having opposite polarities.

4. An integrated circuit device according to claim 1, wherein at least one depletion-inducing junction among the plurality of depletion-inducing junctions (107) comprises an electrical conductor (1204) that traverses the electrically insulating layer (1202) and that interfaces with the semiconductor substrate (1201) thereby forming a Schottky contact.

5. An integrated circuit device according to any of claims 1 to 4, comprising a set of electrical contacts (701) through which a biasing voltage can be applied to at least some depletion-inducing junctions of the plurality.

6. An integrated circuit device according to any of claims 1 to 5, wherein at least some depletion-inducing junctions of the plurality that are disposed in an array-like manner are further disposed in a loop-like manner surrounding at least one of the two sections of the electrical circuit.

7. A semiconductor wafer adapted for manufacturing an integrated circuit device (100) according to any of claims 1 to 6, the semiconductor wafer comprising:

- a semiconductor substrate having a resistivity of at least 100 Ω.cm;
- an electrically insulating layer that contacts the semiconductor substrate, the electrically insulating layer being susceptible of inducing in the semiconductor substrate a parasitic surface conduction layer that interfaces with the electrically insulating layer; and
- a semiconductor layer located on the electrically insulating layer in which the electrical circuit can be formed,

wherein the semiconductor wafer comprises a plurality of depletion-inducing junctions (107) at least partially comprised in the semiconductor substrate, the plurality of depletion-inducing junctions being adapted to autonomously induce in the semiconductor substrate a plurality of depleted zones (301) that interface with the electrically insulating layer, whereby the depletion-inducing junctions are disposed in one of the following manners: an array-like manner and a checkerboard-like manner.

8. A method of manufacturing an integrated circuit device (100) according to any of claims 1 to 6, comprising the step of forming a plurality of depletion-inducing junctions (107) at least partially in a semiconductor substrate having a resistivity of at least 100 Ω.cm, the depletion-inducing junctions being formed to autonomously induce in the

semiconductor substrate a plurality of depleted zones (301) that interface with a section of an electrically insulating layer susceptible of inducing in the semiconductor substrate a parasitic surface conduction layer that interfaces with the electrically insulating layer, whereby the depletion-inducing junctions are formed so that these are disposed in one of the following manners: an array-like manner and a checkerboard-like manner.

9. A method of manufacturing according to claim 8, wherein the depletion-inducing junctions are formed using a processing step that is also used to form the electrical circuit.

10. A method of manufacturing according to claim 8, wherein the depletion-inducing junctions are at least partially formed using at least one of the following techniques: implantation and diffusion.