ABSTRACT

MEMORY CONTROLLERS WITH INTERLEAVED MIRRORED MOMORY MODES

A memory controller comprising: first and second memory channel interfaces; and memory access control circuitry to: send first and second primary data sections to the first and second memory channel interfaces, respectively, and send first and second redundant data sections to the second and first memory channel interfaces, respectively, wherein the first and second redundant data sections are redundant with respect to the first and second primary data sections, respectively, and wherein the memory access control circuitry at time operates in an interleaved mirrored memory mode and at other times in a non-interleaved mode.

Figure 2