THIS SHEET HAS BEEN REPLACED

BUS INTERFACE LOGIC FOR COMPUTER SYSTEM HAVING DUAL BUS ARCHITECTURE

Abstract

A computer system is provided, comprising system memory and a memory controller for controlling access to system memory, a central processing unit electrically connected with the memory controller, and a bus interface unit electrically connected to the memory controller by a system bus and electrically connected to an input/output device by an input/output bus. The bus interface unit includes translation logic for temporarily storing, in response to a predetermined set of operating conditions, data transferred between the system bus and the input/output bus through the bus interface unit. The predetermined set of operating conditions occur when (i) the memory controller on behalf of the central processing unit writes data to the input/output device, or (ii) the memory controller on behalf of the central processing unit initiates a read or write cycle destined for the input/output device acting as a slave on the input/output bus, and the data bus width of the memory controller is greater than a corresponding data bus width of the input/output device.