

ABSTRACT

HIGH SPEED OVER-SAMPLER APPLICATION IN A SERIAL TO PARALLEL CONVERTER

The present invention is a serial to parallel data conversion method and device where new serial data are stored within a first n-bit register prior to presentation at an n-bit parallel output. Subsequently, additional data are stored within a second n-bit register while the data stored within the first register are presented at the parallel output. Data storage and data presentation are thereafter alternated, thereby eliminating the problem of setup time seen in prior art.

(Figure 2 is suitable for publication.)