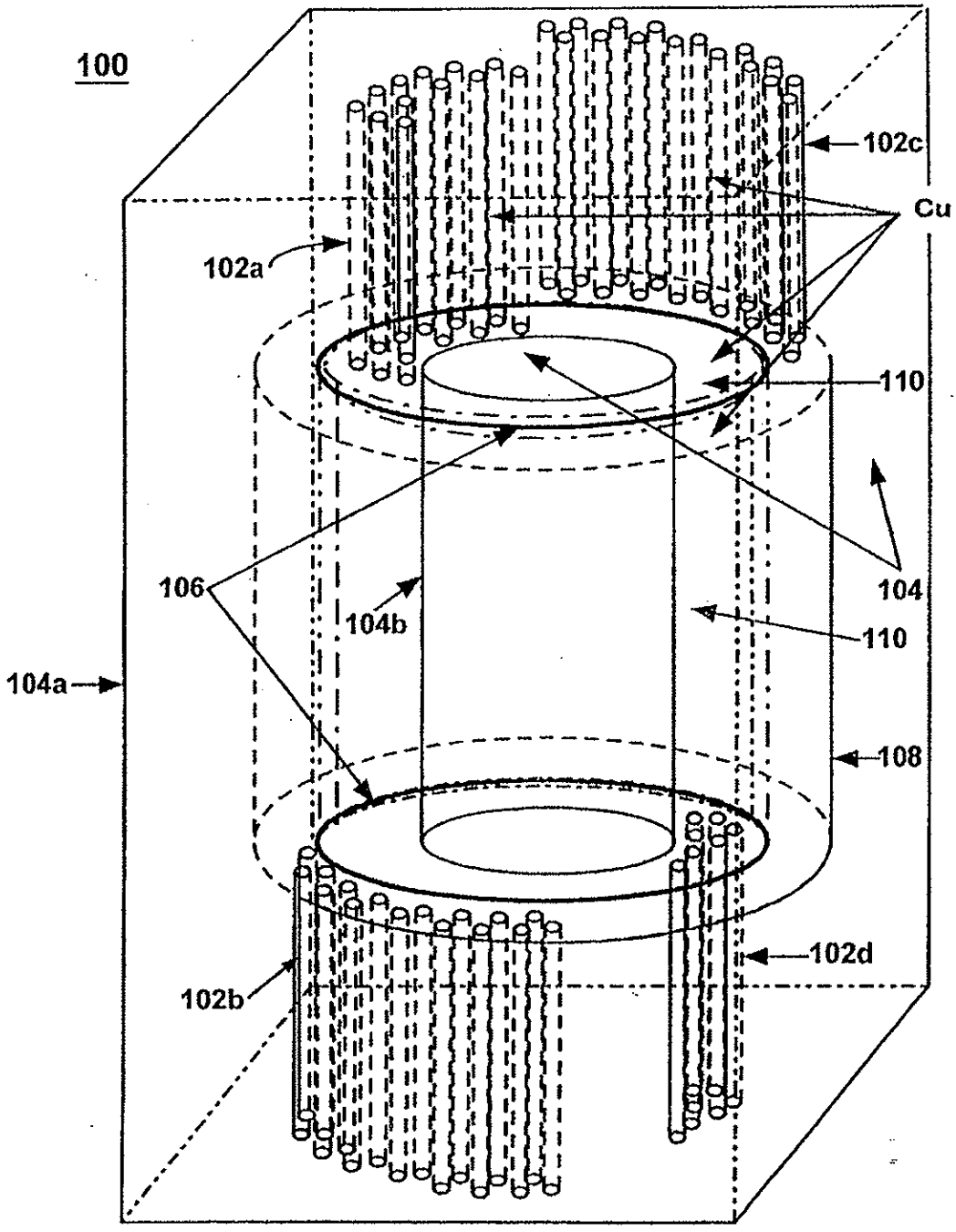


FIG. 1A

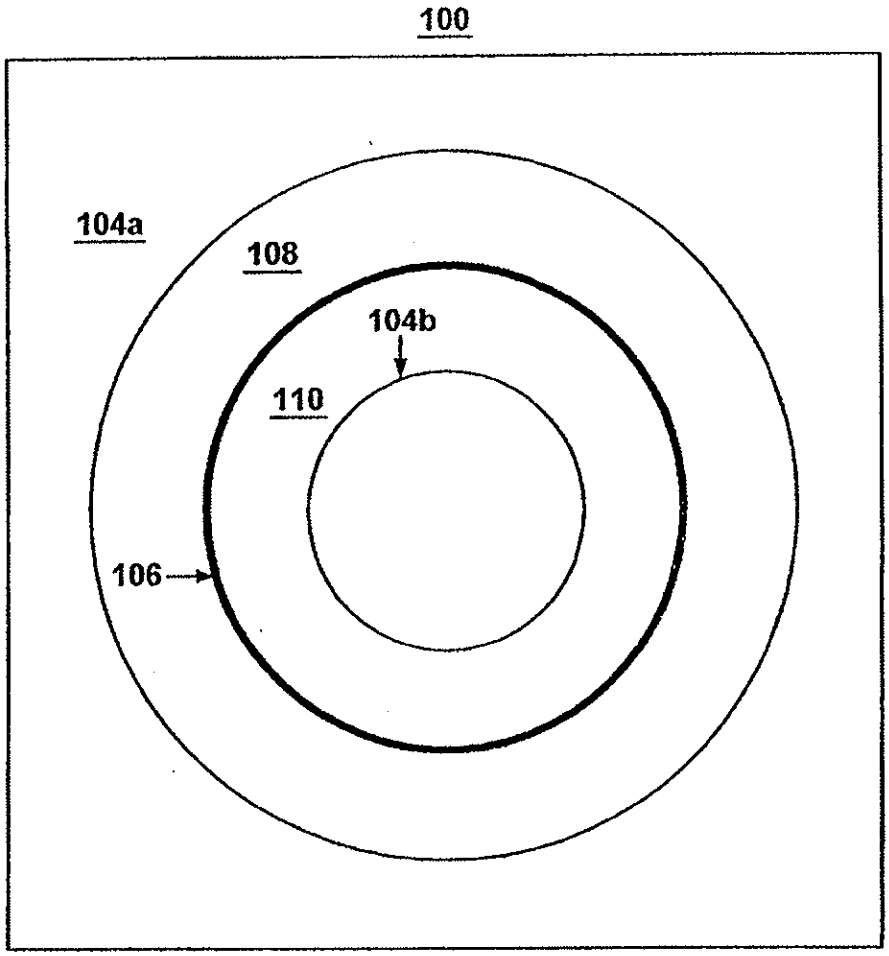


FIG. 1B

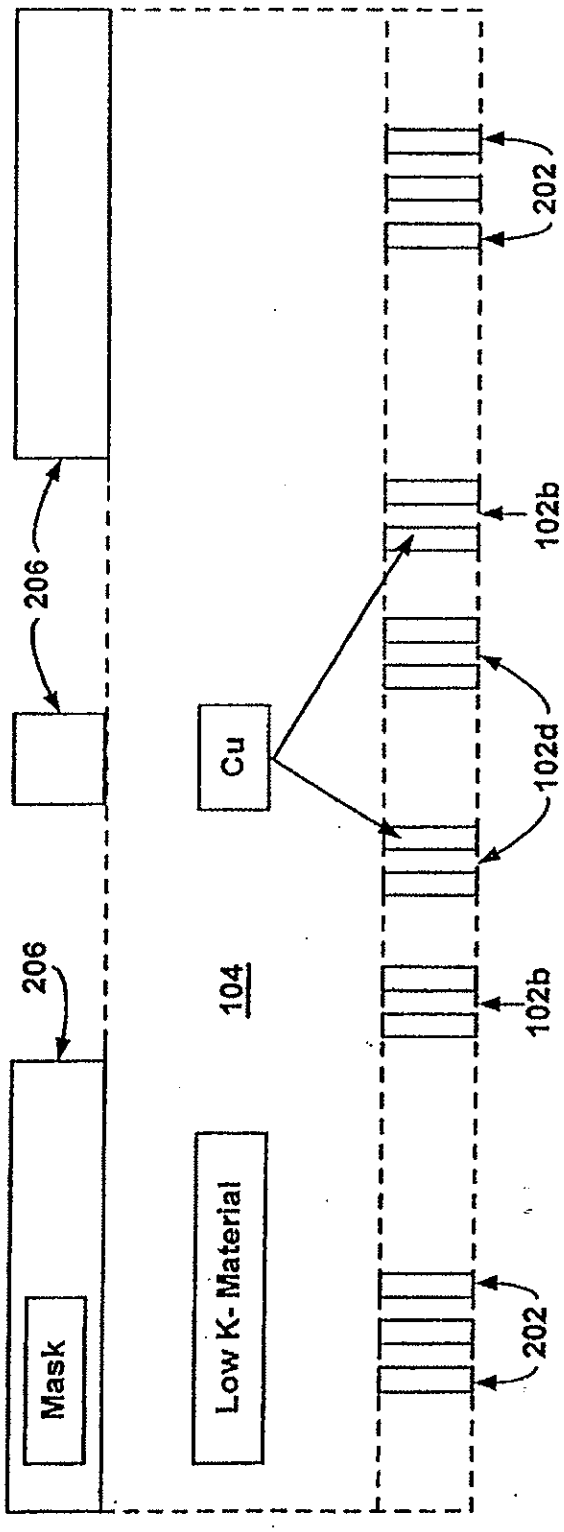


FIG. 2A

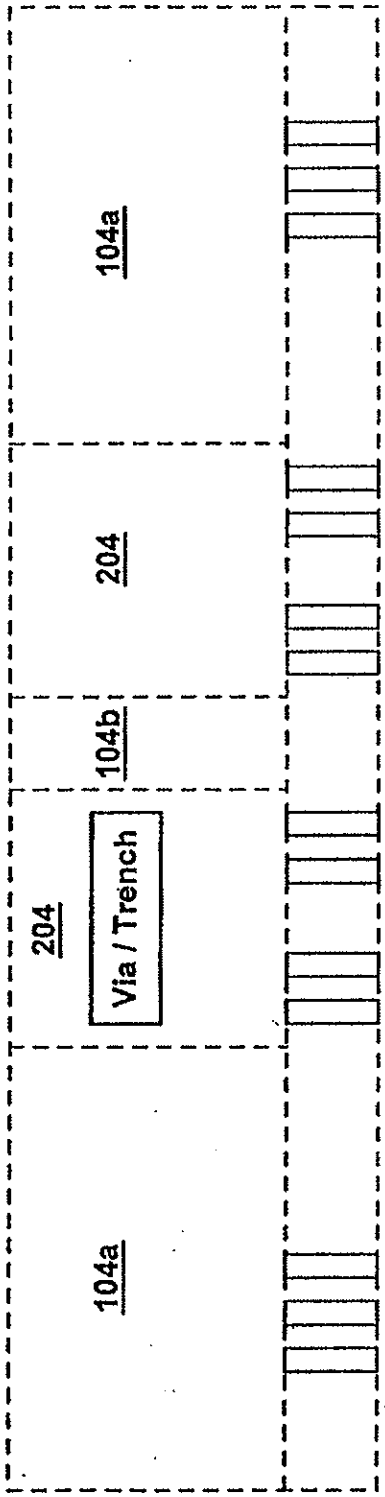


FIG. 2B

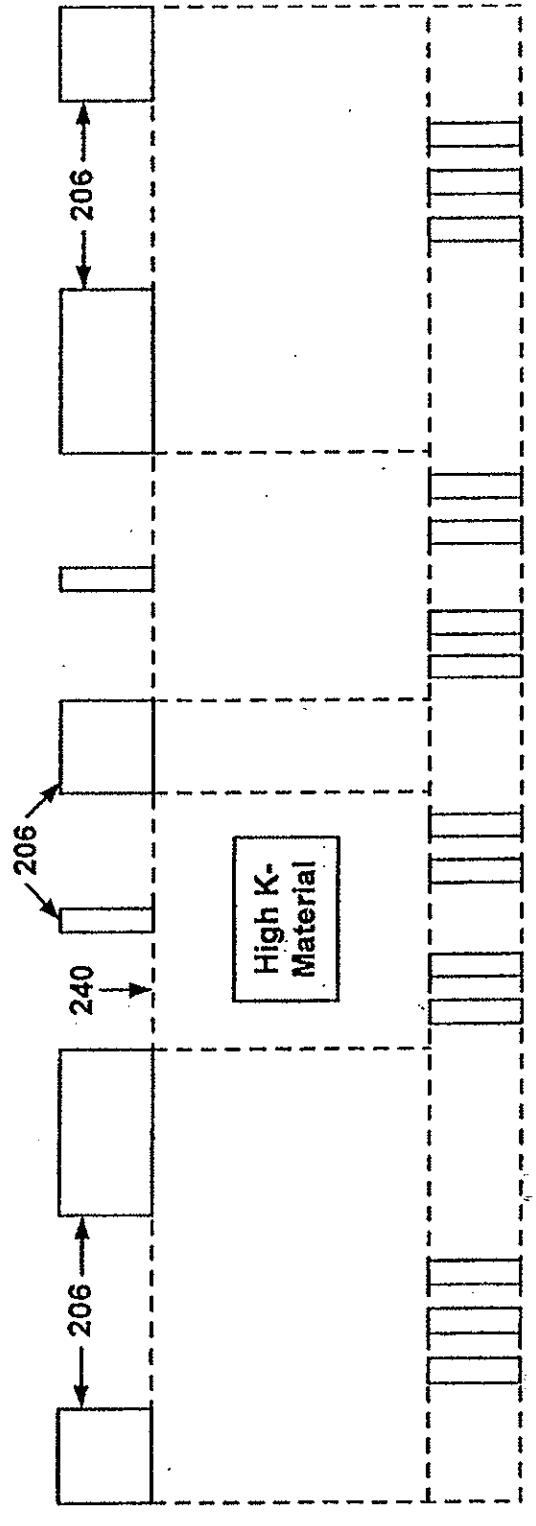


FIG. 2C

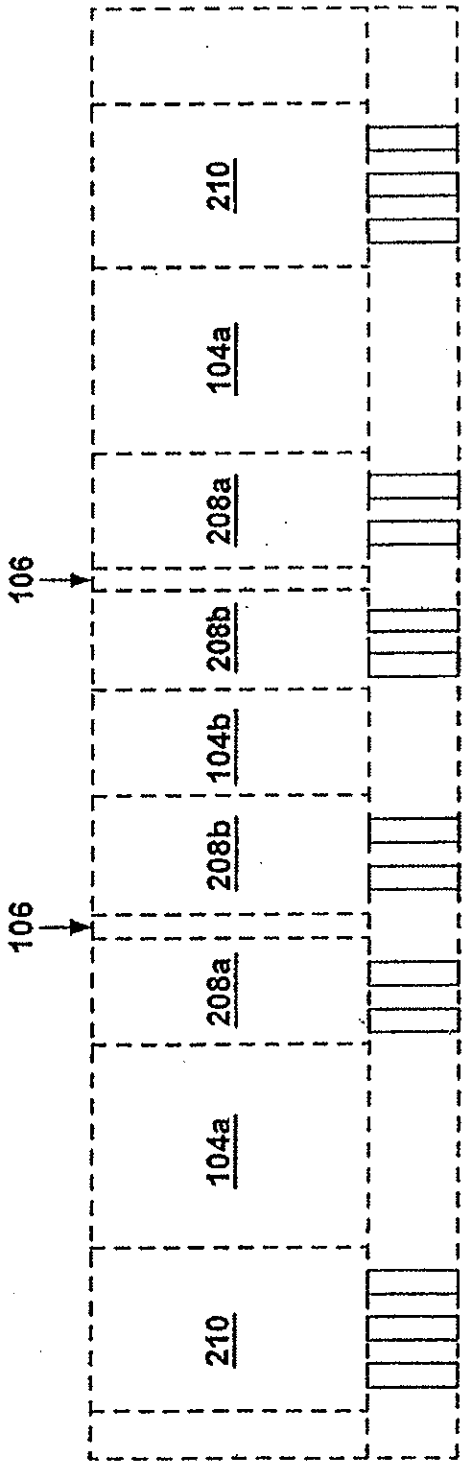


FIG. 2D

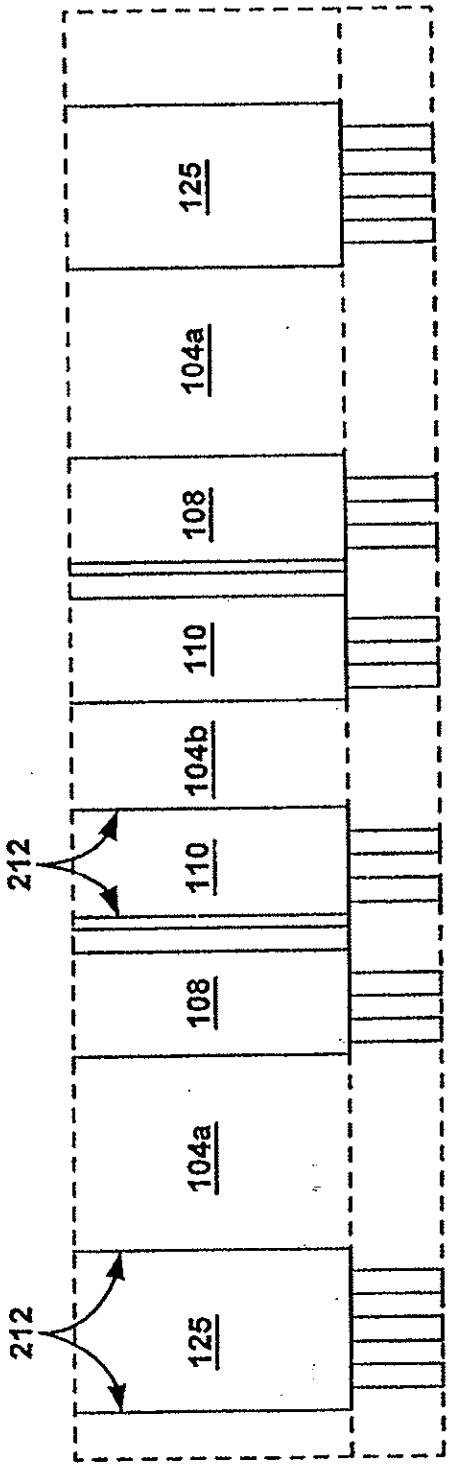


FIG. 2E

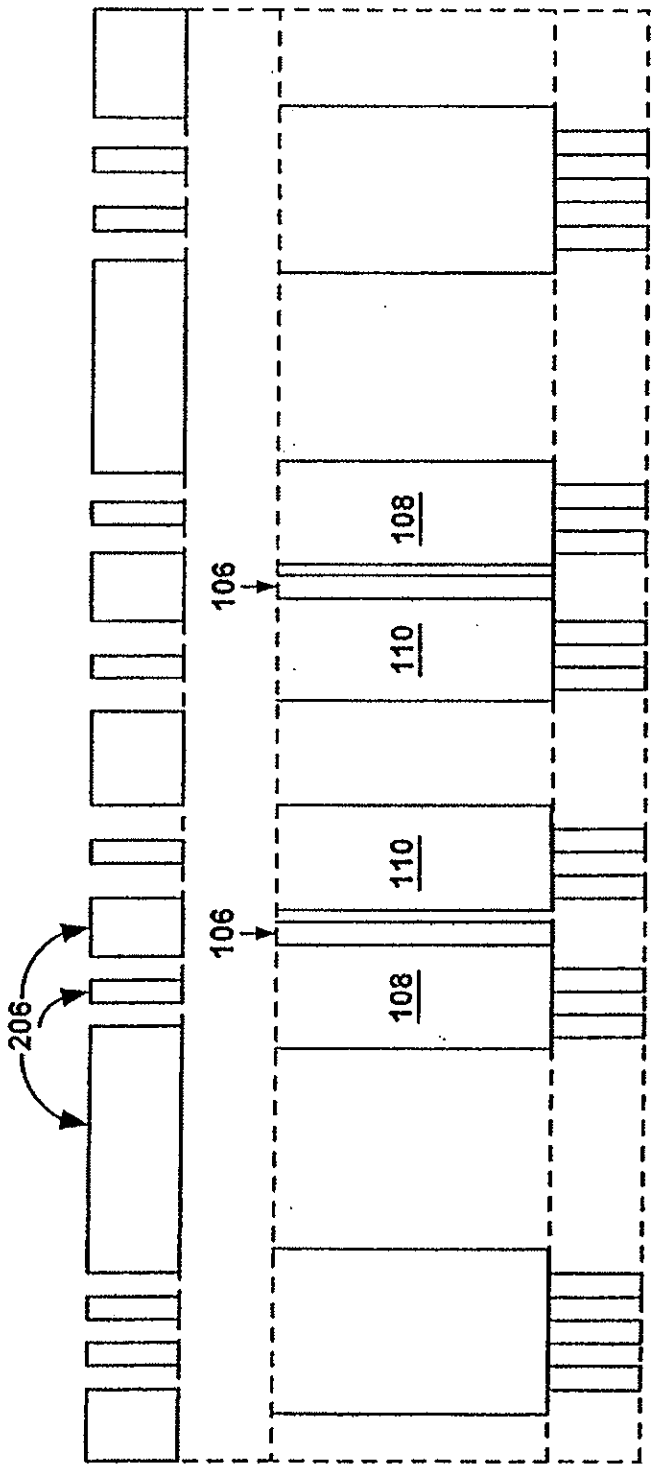


FIG. 2F

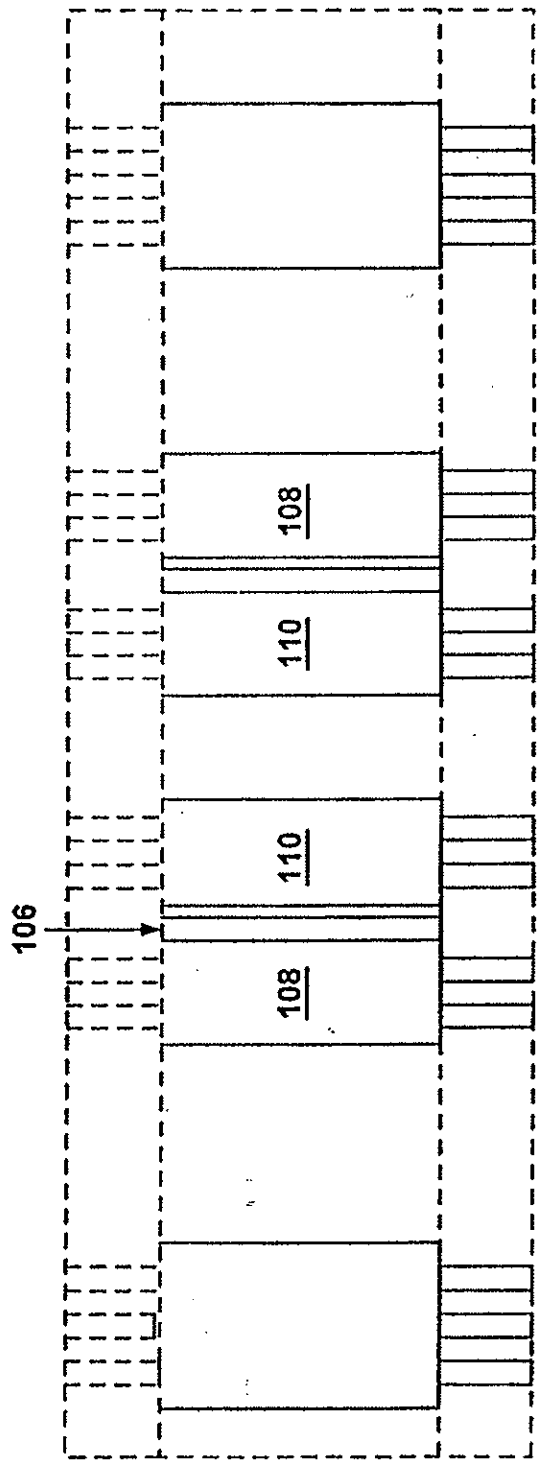


FIG. 2G

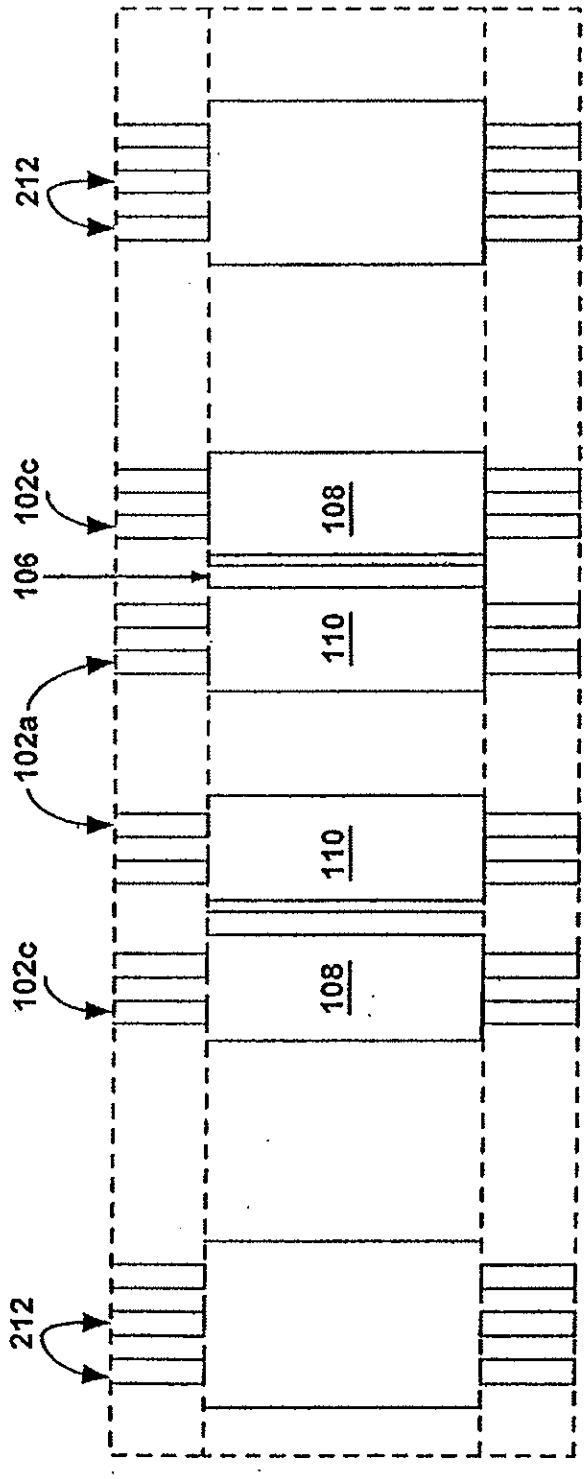


FIG. 2H

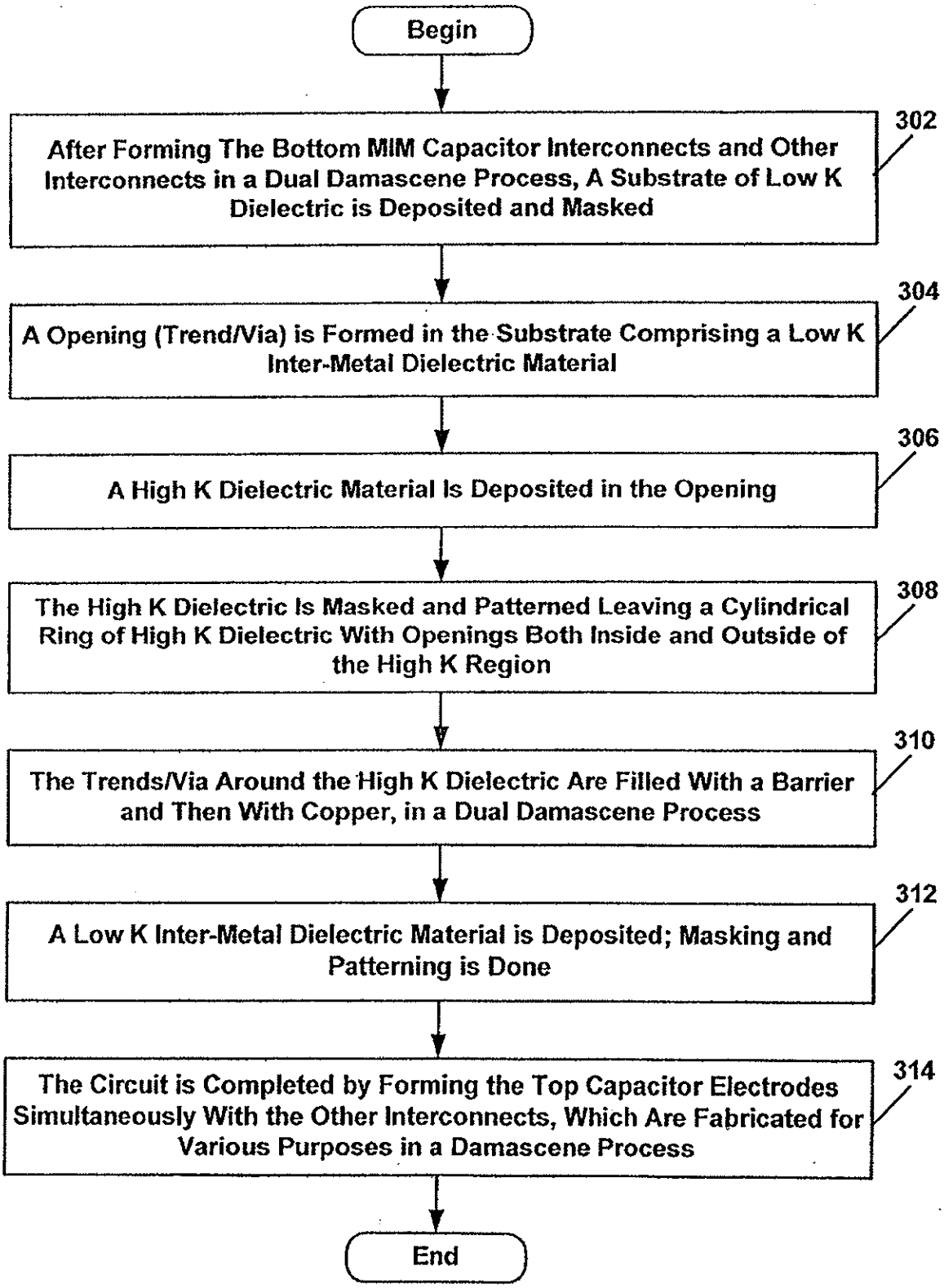

Begin
After Forming The Bottom MIM Capacitor Interconnects and Other Interconnects in a Dual Damascene Process, A Substrate of Low K Dielectric is Deposited and Masked
302
A Opening (Trend/Via) is Formed in the Substrate Comprising a Low K Inter-Metal Dielectric Material
304
A High K Dielectric Material Is Deposited in the Opening
306
The High K Dielectric Is Masked and Patterned Leaving a Cylindrical Ring of High K Dielectric With Openings Both Inside and Outside of the High K Region
308
The Trends/Via Around the High K Dielectric Are Filled With a Barrier and Then With Copper, in a Dual Damascene Process
310
A Low K Inter-Metal Dielectric Material is Deposited; Masking and Patterning is Done
312
The Circuit is Completed by Forming the Top Capacitor Electrodes Simultaneously With the Other Interconnects, Which Are Fabricated for Various Purposes in a Damascene Process
314
End

FIG. 3

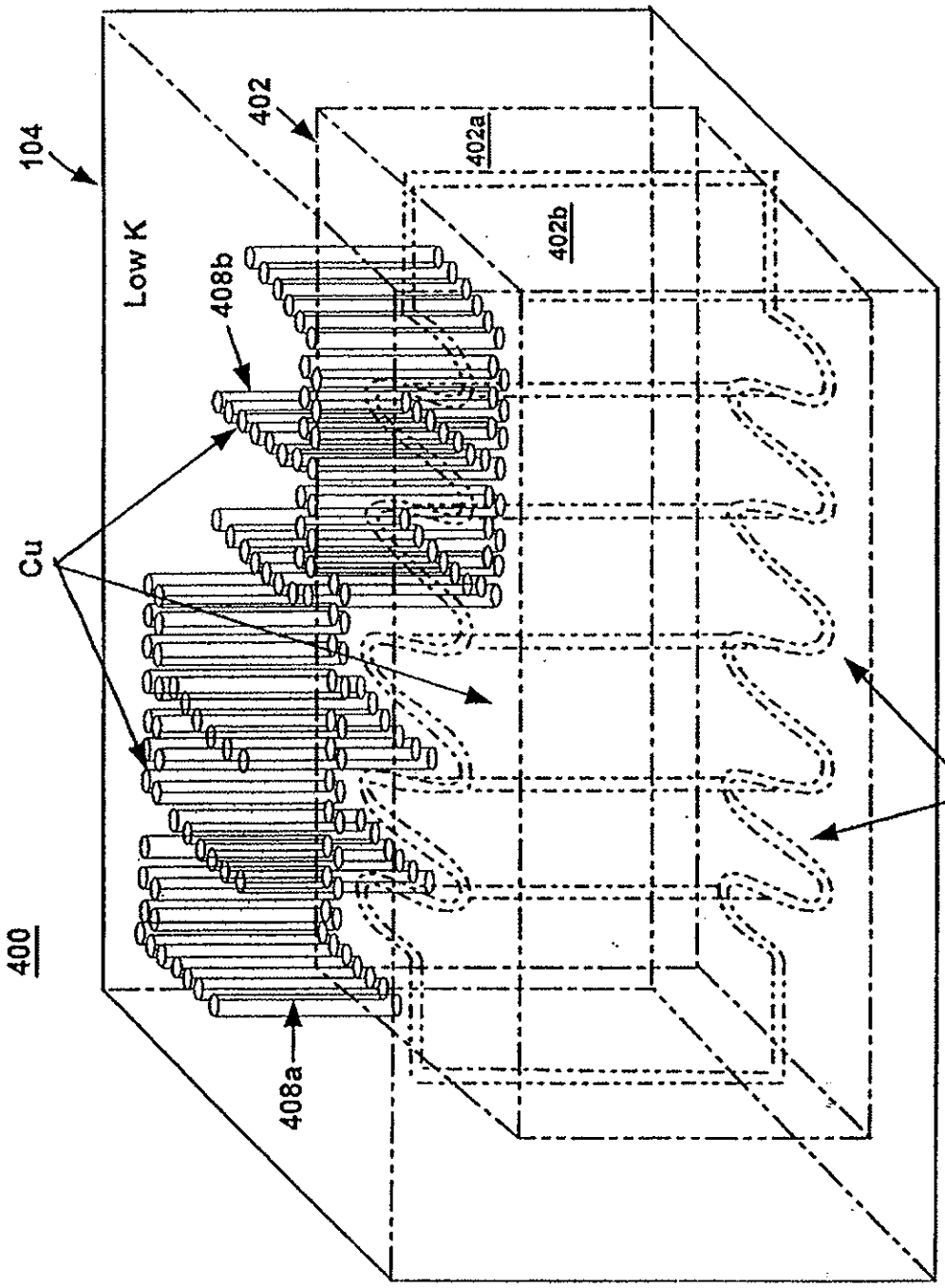


FIG. 4A

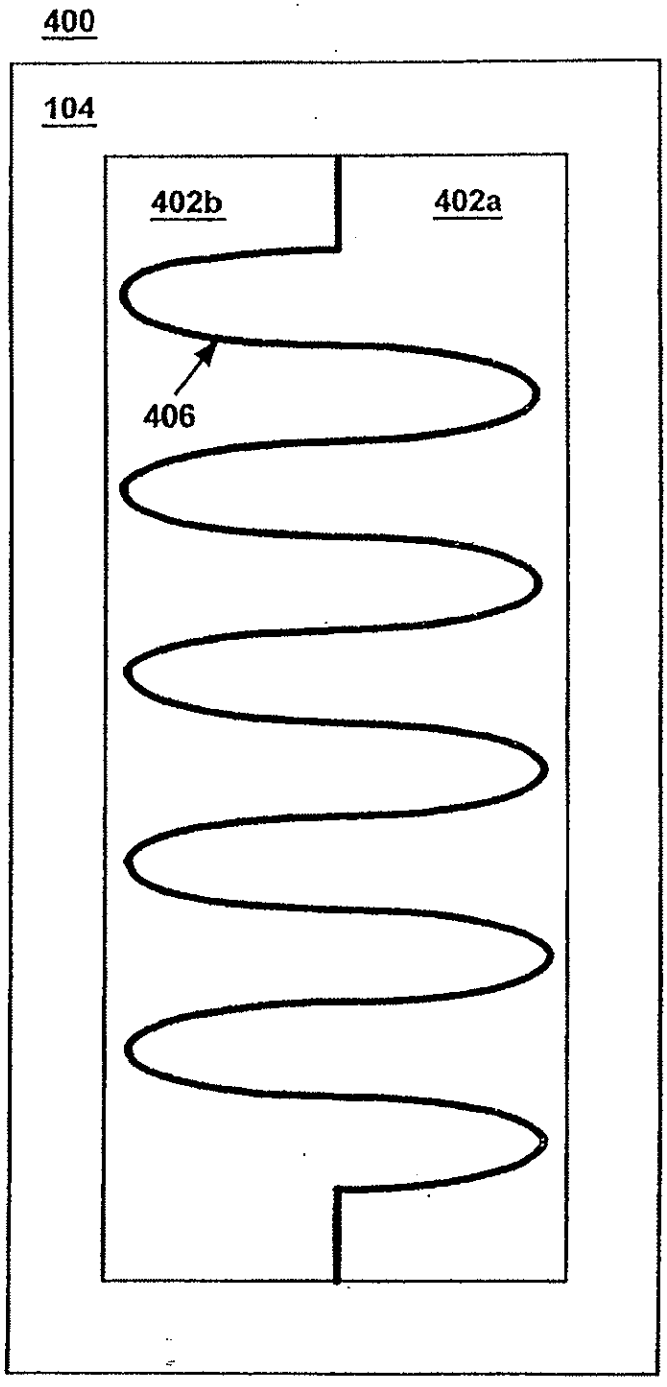


FIG. 4B

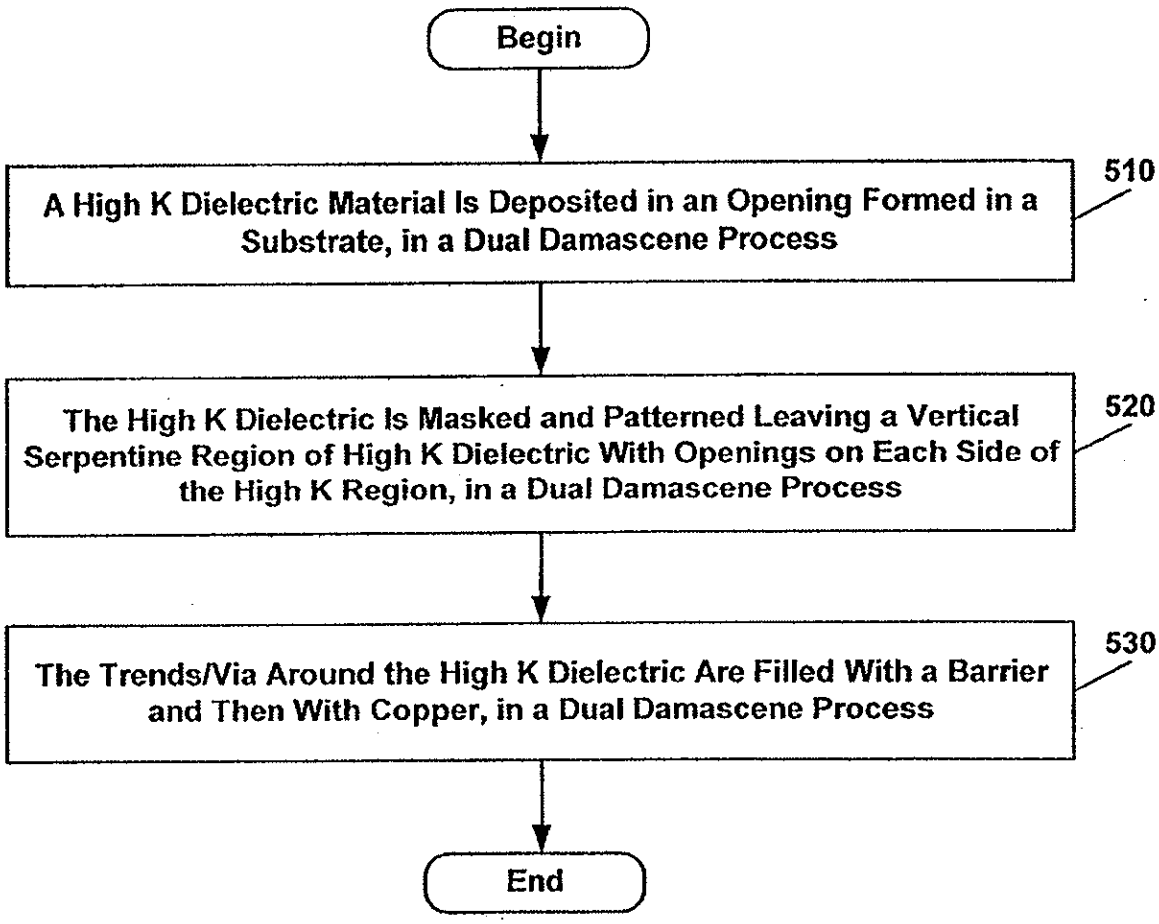

Begin
A High K Dielectric Material Is Deposited in an Opening Formed in a Substrate, in a Dual Damascene Process
510
The High K Dielectric Is Masked and Patterned Leaving a Vertical Serpentine Region of High K Dielectric With Openings on Each Side of the High K Region, in a Dual Damascene Process
520
The Trends/Via Around the High K Dielectric Are Filled With a Barrier and Then With Copper, in a Dual Damascene Process
530
End

FIG. 5

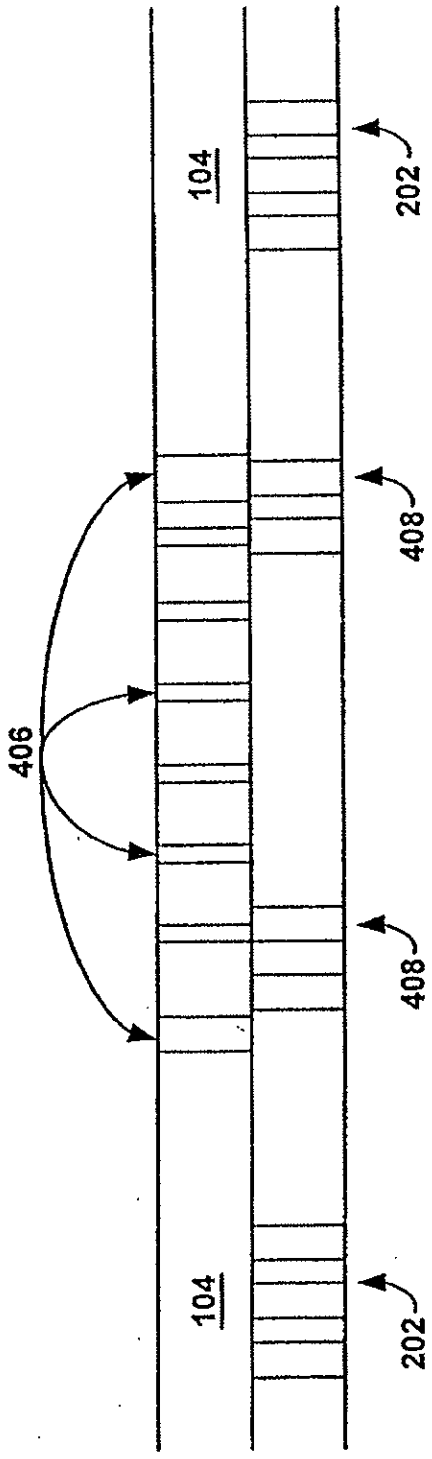


FIG. 6A

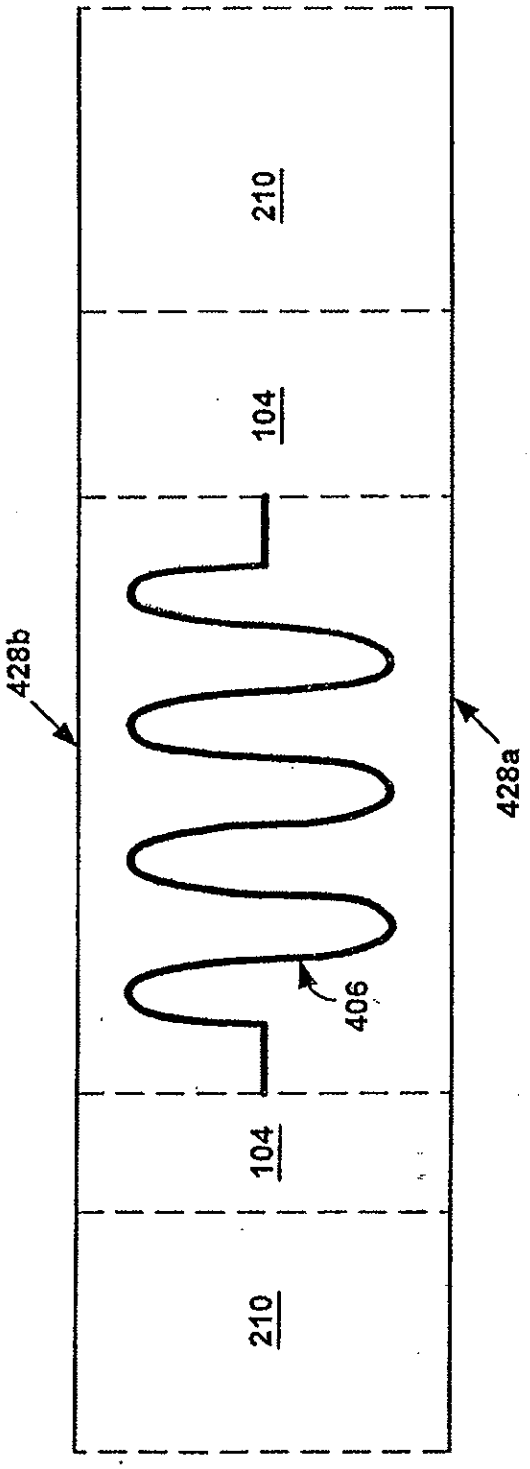


FIG. 6B

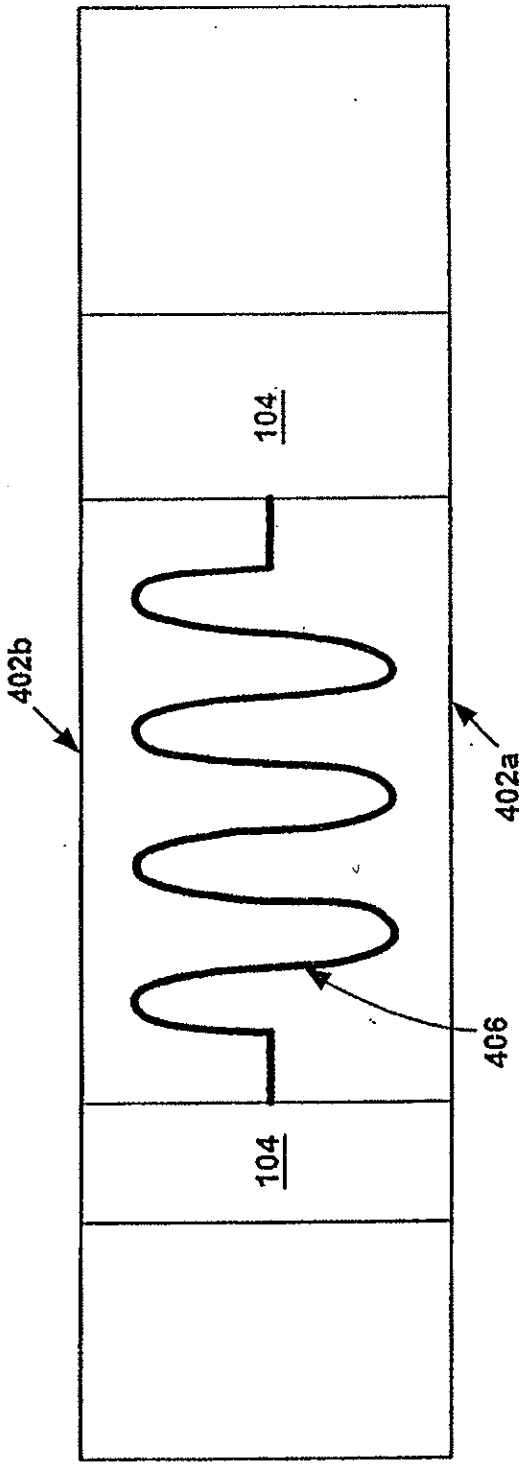


FIG. 6C