INTEGRATED CIRCUIT SYSTEM WITH DOUBLE DOPED DRAIN TRANSISTOR

TECHNICAL FIELD

[0001] The present invention relates to the field of semiconductor manufacturing, and more specifically to metal oxide semiconductor (MOS) transistor structures.

BACKGROUND ART

[0002] Integrated circuits are often manufactured in and on silicon and other semiconductor wafers. Such integrated circuits include literally millions of metal oxide semiconductor (MOS) field effect transistors, having gate lengths on the order of 0.05 microns. Such MOS transistors may include p-channel MOS (PMOS) transistors, and n-channel MOS (NMOS) transistors, depending on their dopant conductivity types.

[0003] Wafers are obtained by drawing an ingot of silicon out of a liquid silicon bath. The ingot is made of mono-crystalline (single-crystal) silicon, and is subsequently sawed into individual wafers. A layer of silicon is then deposited over each wafer. Because the wafer is made of mono-crystalline silicon, the deposition conditions can be controlled so that the layer of silicon deposits "epitaxially" over the wafer. "Epitaxy" refers to the manner in which the silicon layer deposits on the wafer. The layer of silicon has a lattice structure, which further follows the structure of the lattice of the mono-crystalline silicon of the wafer. The layer of silicon is also substantially the same material as the mono-crystalline silicon of the wafer, so that the lattice of the silicon layer also has substantially the same spacing as the spacing of the lattice of the mono-crystalline silicon of the wafer.

[0004] A gate dielectric layer, a gate electrode, and spacers are subsequently formed on the layer of silicon. Ions are also implanted into the layer of silicon, which form source and drain regions on opposing sides of the gate electrode. A voltage can be applied over the source and drain regions. Current flows from the source region to the drain region through a channel below the gate dielectric layer when a voltage is applied to the gate electrode.

[0005] Recent application of high voltage technologies for LCD (Liquid Crystal Display) driver market demands high voltage (6 - 40V range) transistors with minimum transistor pitch. Reduction of pitch poses serious concerns on transistor's HCI (hot-carrier injection) lifetime. HCI is a phenomenon by which the kinetic energy of the carriers (holes or

electrons) is increased as they are accelerated through large potential gradients and subsequently become trapped within the gate oxide. The greatest potential gradient, or maximum electric field, occurs near the drain during saturated operation. More specifically, the electric field is predominant at the lateral junction of the drain adjacent the channel.

[0006] For example in n-channel devices, the electric field at the drain causes channel electrons to gain kinetic energy. Electron-electron scattering randomizes the kinetic energy and the electrons become "hot". Some of these hot electrons have enough energy to create electron-hole pairs through impact ionization of the silicon atoms. Electrons generated by impact ionization join the flow of channel electrons, while the holes flow into the bulk to produce a substrate current in the device. The substrate current is the first indication of the creation of hot carriers in a device. For p-channel devices, the fundamentals of the process are essentially the same except that the role of holes and electrons are reversed.

[0007] HCI occurs when some of the hot carriers are injected into the gate oxide near the drain junction, where they induce damage and become trapped. Traps within the gate oxide generally become electron traps, even if they are initially filled with holes. As a result, there is a negative charge density in the gate oxide. The trapped charge accumulates with time, resulting in positive threshold shifts in both n-channel and p-channel devices. It is known that since hot electrons are more mobile than hot holes, HCI causes a greater threshold skew in n-channel devices than p-channel devices.

[0008] Unless modifications are made to the transistor structure, problems of sub-threshold current and threshold shift resulting from SCE (short-channel effects) and HCI will remain. To overcome these problems, alternative drain structures such as double-diffused drains (DDDs) and lightly doped drains (LDDs) must be used. The purpose of both types of structures is the same: to absorb some of the potential into the drain and thus reduce the maximum electric field. The popularity of DDD structures has given way to LDD structures since DDD causes unacceptably deep junctions and deleterious junction capacitance.

[0009] There appears to be no way to reduce the size of high voltage semiconductor devices, such as DDD MOS transistors or to reduce substrate current and increase lifetime of the transistors.

[0010] Thus, a need still remains for an integrated circuit system to lower costs with lower substrate currents, improved lifetime, reduced thermal cycles, and greater packaging densities, to provide and support systems that are capable of achieving optimal thin, high-density footprint semiconductor systems. In view of the ever-increasing commercial

competitive pressures, along with growing consumer expectations and the diminishing opportunities for meaningful product differentiation in the marketplace, it is critical that answers be found for these problems. Additionally, the need to save costs, improve efficiencies and performance, and meet competitive pressures, adds an even greater urgency to the critical necessity for finding answers to these problems.

[0011] Solutions to these problems have been long sought but prior developments have not taught or suggested any solutions and, thus, solutions to these problems have long eluded those skilled in the art.

DISCLOSURE OF THE INVENTION

[0012] The present invention provides a substrate, forming a gate over the substrate, forming a first drift region having a first counter diffused region and a source diffused region, the first drift region in the substrate adjacent a first side of the gate, and forming a second drift region having a second counter diffused region and a drain diffused region, the second drift region in the substrate adjacent a second side of the gate opposite the first side of the gate.

[0013] Certain embodiments of the invention have other advantages in addition to or in place of those mentioned above. The advantages will become apparent to those skilled in the art from a reading of the following detailed description when taken with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 is a cross-sectional view of an integrated circuit system;

[0015] FIG. 2 is a cross-sectional view of an integrated circuit system in a gate forming phase in an alternative embodiment of the present invention;

[0016] FIG. 3 is the structure of FIG. 2 in a double diffusion forming phase;

[0017] FIG. 4 is the structure of FIG. 3 in a spacer forming phase;

[0018] FIG. 5 is the structure of FIG. 4 in a source and drain forming phase n;

[0019] FIG. 6 is a cross-sectional view of the integrated circuit system;

[0020] FIG. 7 is a cross-sectional view of an integrated circuit system in a double diffusion forming phase in another alternative embodiment of the present invention;

[0021] FIG. 8 is the structure of FIG. 7 in a gate forming phase;

[0022] FIG. 9 is the structure of FIG. 8 in a spacer forming phase;

[0023] FIG. 10 is the structure of FIG. 9 in a source and drain forming phase;

[0024] FIG. 11 is a cross-sectional view of the integrated circuit system;

[0025] FIG. 12 is a substrate current graph; and

[0026] FIG. 13 is a flow chart of an integrated circuit system for manufacturing the integrated circuit system in an embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0027] The following embodiments are described in sufficient detail to enable those skilled in the art to make and use the invention. It is to be understood that other embodiments would be evident based on the present disclosure, and that system, process, or mechanical changes may be made without departing from the scope of the present invention.

[0028] In the following description, numerous specific details are given to provide a thorough understanding of the invention. However, it will be apparent that the invention may be practiced without these specific details. In order to avoid obscuring the present invention, some well-known circuits, system configurations, and process steps are not disclosed in detail. Likewise, the drawings showing embodiments of the system are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and are shown greatly exaggerated in the drawing FIGs. Where multiple embodiments are disclosed and described, having some features in common, for clarity and ease of illustration, description, and comprehension thereof, similar and like features one to another will ordinarily be described with like reference numerals.

[0029] For expository purposes, the term "horizontal" as used herein is defined as a plane parallel to the plane or surface of the invention, regardless of its orientation. The term "vertical" refers to a direction perpendicular to the horizontal as just defined. Terms, such as "on", "above", "below", "bottom", "top", "side" (as in "sidewall"), "higher", "lower", "upper", "over", and "under", are defined with respect to the horizontal plane.

[0030] The term "on" as used herein means and refers to direct contact among elements. The term "processing" as used herein includes deposition of material, patterning, exposure, development, etching, cleaning, and/or removal of the material or trimming as required in forming a described structure. The term "system" as used herein means and refers to the method and to the apparatus of the present invention in accordance with the context in which the term is used.

[0031] Referring now to FIG. 1, therein is a cross-sectional view of an integrated circuit system 100. The integrated circuit system 100 can include a substrate 102, such as a P-type body, with drift regions 104, such as N-type regions. The integrated circuit system 100 can include a gate 106 over a gate insulator 108 preferably formed over a region between the drift regions 104. The gate insulator 108 or the gate 106 can overlap the drift regions 104. The integrated circuit system 100 can also include counter diffused regions 110, such as a P+ counter doped regions, to form bipolar-like junction structures.

[0032] The counter diffused regions 110 can be formed in the drift regions 104 adjacent or near the gate insulator 108 and the gate 106. An edge of the counter diffused regions 110 near the gate insulator 108 can preferably provide spacing to an edge of the drift regions 104 also near the gate insulator 108. The counter diffused regions 110 can be formed to a depth less than a depth of the drift regions 104 such that current flows through the drift regions 104 and a bulk region 114 of the substrate 102.

[0033] The counter diffused regions 110 can preferably be formed to a depth of between approximately one-tenth of a micron (0.1um) to approximately three-tenths of a micron (0.3um) for the integrated circuit system 100 optionally formed as an N-type device, such as an N-type double-diffused drain (NDDD) transistor. The depth of the counter diffused regions 110 can be too shallow resulting in substantially no improvement in lifetime of the integrated circuit system 100 or substantially no improvement in device pitch. The counter diffused regions 110 can preferably have a dopant concentration approximately an order of magnitude less than a dopant concentration of the drift regions 104. The dopant concentration of the counter diffused regions 110 can be too high resulting in a decrease in drive current due in part to recombination effects.

[0034] For an N-type device, the counter diffused regions 110 can be formed with a dopant, such as Boron BF2 Indium. The dopant, such as Boron or compound thereof, can form the counter diffused regions 110 with implant energy between approximately ten thousand electronvolts (10keV) and approximately fifty thousand electronvolts (50keV), preferably thirty thousand electronvolts (30keV). A dose of the dopant, such as Boron or compound thereof, between approximately five hundred billion ions per square centimeter (5E11) to approximately three trillion ions per square centimeter (3E12), preferably one trillion ions per square centimeter (1E12), can form the counter diffused regions 110. For a P-type device, such as a P-type double-diffused drain (PDDD) transistor, the counter diffused regions 110 can be formed with a dopant, such as Phosphorus, Arsenic, or Antimony.

[0035] The integrated circuit system 100 can further include a source diffused region 116, such as an N-type doped region, and a drain diffused region 118, such as an N-type doped region. The source diffused region 116 and the drain diffused region 118 can preferably be formed having a higher dopant concentration than the drift regions 104 to provide an electrical contact area. For illustrative purposes, the integrated circuit system 100 is shown as an N-type field-effect transistor (NMOS FET) although it is understood that other configurations, such as a P-type field-effect transistor (PMOS FET) may also be used.

[0036] It has been discovered that the integrated circuit system 100 increases a path for carrier injection between the source diffused region 116 and the drain diffused region 118 thereby providing lower substrate current, improved lifetime, such as hot carrier injection (HCI) lifetime, reduced thermal cycles including impact on adjacent lower voltage transistors, and higher packing density, such as reducing device size or pitch.

[0037] Referring now to FIG. 2, therein is shown a cross-sectional view of an integrated circuit system 200 in a gate forming phase in an alternative embodiment of the present invention. Similar to the integrated circuit system 100, the integrated circuit system 200 can include can include a substrate 202, such as a P-type body, with drift regions 204, such as N-type regions. The integrated circuit system 200 can also include a gate 206 over a gate insulator 208 preferably formed over a region between the drift regions 204. The gate insulator 208 or the gate 206 can overlap the drift regions 204.

[0038] Referring now to FIG. 3, therein is shown the structure of FIG. 2 in a double diffusion forming phase. The integrated circuit system 200 can also include counter diffused regions 302, such as a P+ counter doped regions, to form bipolar-like junction structures. The counter diffused regions 302 can preferably be formed, such as self-aligned, over the gate 206 providing alignment to outer vertical edges of the gate 206. The counter diffused regions 302 can be formed to a depth less than a depth of the drift regions 204 such that current flows through the drift regions 204 and a bulk region 304 of the substrate 202.

[0039] Referring now to FIG. 4, therein is shown the structure of FIG. 3 in a spacer forming phase. The integrated circuit system 200 can include spacers 402, such as an oxide or other insulator. The spacers 402 can be formed adjacent outer vertical edges of the gate 206 and outer vertical edges of the gate insulator 208. A junction region of each of the counter diffused regions 302 can preferably be covered by the spacers 402. The spacers 402 can provide isolation of the junction region 4xx of each of the counter diffused regions 302 for further processing.

[0040] Referring now to FIG. 5, therein is shown the structure of FIG. 4 in a source and drain forming phase. The integrated circuit system 200 can include a source diffused region 502, such as an N-type doped region, and a drain diffused region 504, such as an N-type doped region. The source diffused region 502 and the drain diffused region 504 can optionally be formed adjacent a resist layer (not shown) such as a photoresist. The resist layer can provide additional area beyond the spacers 402 for the counter diffused regions 302. The source diffused region 502 and the drain diffused region 504 can preferably be formed having a higher dopant concentration than the drift regions 204 to provide an electrical contact area.

[0041] Referring now to FIG. 6, therein is shown a cross-sectional view of the integrated circuit system 200. The integrated circuit system 200 can includes connectors 602, such as metal contacts. The connectors 602 can provide electrical contact to the source diffused region 502 or the drain diffused region 504 and thereby the source terminal or drain terminal of the device, such as a metal-oxide-semiconductor field-effect transistor (MOSFET).

[0042] For illustrative purposes, the integrated circuit system 200 is shown as an N-type double-diffused drain transistor (NDDD) although it is understood that other configurations, such as a P-type double-diffused drain transistor (PDDD) may be used.

[0043] Referring now to FIG. 7, therein is shown a cross-sectional view of an integrated circuit system 700 in a double diffusion forming phase in another alternative embodiment of the present invention. Similar to the integrated circuit system 100, the integrated circuit system 700 can include can include a substrate 702, such as a P-type body, with drift regions 704, such as N-type regions. The integrated circuit system 700 can also include counter diffused regions 706, such as a P+ counter doped regions, to form bipolar-like junction structures. The counter diffused regions 706 can preferably be formed to a depth less than a depth of the drift regions 704 such that current flows through the drift regions 704 and a bulk region 708 of the substrate 702.

[0044] Referring now to FIG. 8, therein is shown the structure of FIG. 7 in a gate forming phase. The integrated circuit system 700 can include a gate 802 over a gate insulator 804 preferably formed, such as non-self-aligned, over a region between the drift regions 704 and the counter diffused regions 706. The gate insulator 804 or the gate 802 can overlap the drift regions 704 and provide outer vertical edges of the gate 802 or outer vertical edges of the gate insulator 804 substantially aligned to inner extents of the counter diffused regions 706.

[0045] Referring now to FIG. 9, therein is shown the structure of FIG. 8 in a spacer forming phase. The integrated circuit system 200 can include spacers 902, such as an oxide or other

insulator. The spacers 902 can be formed adjacent outer vertical edges of the gate 802 and outer vertical edges of the gate insulator 804. A junction region of each of the counter diffused regions 706 can preferably be covered by the spacers 902. The spacers 902 can provide isolation of the junction region 9xx of each of the counter diffused regions 706 for further processing.

[0046] Referring now to FIG. 10, therein is shown the structure of FIG. 9 in a source and drain forming phase. The integrated circuit system 700 can include a source diffused region 1002, such as an N-type doped region, and a drain diffused region 1004, such as an N-type doped region. The source diffused region 1002 and the drain diffused region 1004 can optionally be formed adjacent a resist layer (not shown) such as a photoresist. The resist layer can provide additional area beyond the spacers 902 for the counter diffused regions 706. The source diffused region 1002 and the drain diffused region 1004 can preferably be formed having a higher dopant concentration than the drift regions 704 to provide an electrical contact area.

[0047] Referring now to FIG. 11, therein is shown a cross-sectional view of the integrated circuit system 700. The integrated circuit system 700 can includes connectors 1102, such as metal contacts. The connectors 1102 can provide electrical contact to the source diffused region 1002 or the drain diffused region 1004 and thereby the source terminal or drain terminal of the device, such as a metal-oxide-semiconductor field-effect transistor (MOSFET).

[0048] For illustrative purposes, the integrated circuit system 700 is shown as an N-type double-diffused drain transistor (NDDD) although it is understood that other configurations, such as a P-type double-diffused drain transistor (PDDD) may be used.

[0049] Referring now to FIG. 12, therein is shown a substrate current graph 1200. The substrate current graph 1200 includes gate voltages 1202 and substrate currents 1204. A first plot 1206 of the substrate currents 1204 shown based on the gate voltages 1202 of the integrated circuit system 100 are significantly lower than a second plot 1208 of the substrate currents 1204 based on the gate voltages 1202 of an other structure (not shown), such as a conventional MOSFET. Hot carrier injection (HCI) lifetime based on the substrate current graph can be approximately two and two hundred fifty-two thousandths (2.252) years for the integrated circuit system 100 resulting in approximately one thousand times improvement over the other structure.

[0050] Referring now to FIG. 13, therein is shown a flow chart of an integrated circuit system 1300 for manufacturing the integrated circuit system 100 in an embodiment of the present invention. The system 1300 includes providing a substrate in a block 1302; forming a gate over the substrate in a block 1304; forming a first drift region having a first counter diffused region and a source diffused region, the first drift region in the substrate adjacent a first side of the gate in a block 1306; and forming a second drift region having a second counter diffused region and a drain diffused region, the second drift region in the substrate adjacent a second side of the gate opposite the first side of the gate in a block 1308.

[0051] In greater detail, a system to provide the method and apparatus of the integrated circuit system 100, in an embodiment of the present invention, is performed as follows:

1. Providing a substrate having a bulk region.
2. Forming a gate with a gate insulator over the substrate.
3. Forming a first drift region in the substrate adjacent a first side of the gate.
4. Forming a second drift region in the substrate adjacent a second side of the gate opposite the first side of the gate.
5. Forming a first counter diffused region in the first drift region adjacent the first side of the gate.
6. Forming a second counter diffused region in the second drift region adjacent the second side of the gate.
7. Forming a source diffused region in the first drift region adjacent a side of the first counter diffused region opposite the gate.
8. Forming a drain diffused region in the second drift regions adjacent a side of the second counter diffused region opposite the gate.

[0052] Thus, it has been discovered that the integrated circuit system method and apparatus of the present invention furnish important and heretofore unknown and unavailable solutions, capabilities, and functional aspects. The resulting processes and configurations are straightforward, cost-effective, uncomplicated, highly versatile, accurate, sensitive, and effective, and can be implemented by adapting known components for ready, efficient, and economical manufacturing, application, and utilization.

[0053] While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations, which fall within the scope of the

included claims. All matters hithertofore set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

What is claimed is:

1. An integrated circuit system comprising:

providing a substrate;

forming a gate over the substrate;

forming a first drift region having a first counter diffused region and a source diffused region, the first drift region in the substrate adjacent a first side of the gate; and

forming a second drift region having a second counter diffused region and a drain diffused region, the second drift region in the substrate adjacent a second side of the gate opposite the first side of the gate.

2. The system as claimed in claim 1 further comprising flowing current through the first drift region and a bulk region of the substrate providing the integrated circuit system with approximately one thousand times a lifetime of a conventional device.

3. The system as claimed in claim 1 wherein forming the first counter diffused region includes applying a dopant over the first drift region and the gate.

4. The system as claimed in claim 1 wherein forming the first counter diffused region includes applying a dopant over the first drift region without the gate.

5. The system as claimed in claim 1 wherein forming the first counter diffused region includes forming the first counter diffused region at a depth approximately half a depth of the first drift region.

6. An integrated circuit system comprising:

providing a substrate having a bulk region;

forming a gate with a gate insulator over the substrate;

forming a first drift region in the substrate adjacent a first side of the gate;

forming a second drift region in the substrate adjacent a second side of the gate opposite the first side of the gate;

forming a first counter diffused region in the first drift region adjacent the first side of the gate;

forming a second counter diffused region in the second drift region adjacent the second side of the gate;

forming a source diffused region in the first drift region adjacent a side of the first counter diffused region opposite the gate; and

forming a drain diffused region in the second drift region adjacent a side of the second counter diffused region opposite the gate.

7. The system as claimed in claim 6 wherein forming the first counter diffused region includes forming the first counter diffused region to a depth of approximately one-tenth of a micron to three-tenths of a micron.

8. The system as claimed in claim 6 wherein forming the first counter diffused region includes boron or a compound thereof.

9. The system as claimed in claim 6 wherein forming the first counter diffused region includes phosphorus, arsenic, antimony, or a compound thereof.

10. The system as claimed in claim 6 wherein forming the first counter diffused region includes forming the first counter diffused region with a dopant concentration approximately an order of magnitude less that a dopant concentration of the first drift region.

11. An integrated circuit system comprising:

a substrate;

a gate over the substrate;

a first drift region having a first counter diffused region and a source diffused region, the first drift region in the substrate adjacent a first side of the gate; and

a second drift region having a second counter diffused region and a drain diffused region, the second drift region in the substrate adjacent a second side of the gate opposite the first side of the gate.

12. The system as claimed in claim 11 wherein the first counter diffused region includes the first counter diffused region at a depth approximately half a depth of the first drift region.

13. The system as claimed in claim 11 further comprising the first drift region and a bulk region of the substrate for current flow providing the integrated circuit system with approximately one thousand times a lifetime of a conventional device.

14. The system as claimed in claim 11 wherein the first counter diffused region includes a dopant over the first drift region and the gate.

15. The system as claimed in claim 11 wherein the first counter diffused region includes a dopant over the first drift region without the gate.

16. The system as claimed in claim 11 wherein:

the substrate is the substrate with a bulk region;

the gate is the gate with a gate insulator over the substrate;

the first drift region is:

the first drift region in the substrate adjacent a first side of the gate;

the first counter diffused region in the first drift region adjacent the first side of the gate;

the source diffused region in the first drift region adjacent a side of the first counter diffused region opposite the gate; and

the second drift region is:

the second drift region in the substrate adjacent a second side of the gate opposite the first side of the gate;

the second counter diffused region in the second drift region adjacent the second side of the gate;

the drain diffused region in the second drift region adjacent a side of the second counter diffused region opposite the gate.

17. The system as claimed in claim 16 wherein the first counter diffused region includes the first counter diffused region to a depth of approximately one-tenth of a micron to three-tenths of a micron.

18. The system as claimed in claim 16 wherein the first counter diffused region includes boron or a compound thereof.

19. The system as claimed in claim 16 wherein the first counter diffused region includes phosphorus, arsenic, antimony, or a compound thereof.

20. The system as claimed in claim 16 wherein the first counter diffused region includes the first counter diffused region with a dopant concentration approximately an order of magnitude less that a dopant concentration of the first drift region.