

CORRECTED VERSION

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
16 September 2004 (16.09.2004)

PCT

(10) International Publication Number
WO 2004/079801 A1

(51) International Patent Classification⁷: **H01L 21/20**,
21/324, 21/762

(21) International Application Number:
PCT/IB2004/000940

(22) International Filing Date: 1 March 2004 (01.03.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0302623 4 March 2003 (04.03.2003) FR

(71) Applicant (for all designated States except US):
**S.O.I.TEC SILICON ON INSULATOR TECH-
NOLOGIES** [FR/FR]; Parc Technologique des Fontaines,
Chemin des Franques, F-38190 Bernin (FR).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **NEYRET, Eric**
[FR/FR]; 2, rue Lesguidières, F-38360 Sassenage (FR).
MALLEVILLE, Christophe [FR/FR]; 90, rue du
Château, F-38660 La Terrasse (FR).

(74) Agents: **MARTIN, Jean-Jacques** et al.; Cabinet Regim-
beau, 20, rue de Chazelles, F-75847 Paris Cedex 17 (FR).

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,

CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,
GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE,
KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD,
MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG,
PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM,
TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM,
ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), Euro-
pean (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR,
GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— of inventorship (Rule 4.17(iv)) for US only

Published:

— with international search report

(48) Date of publication of this corrected version:

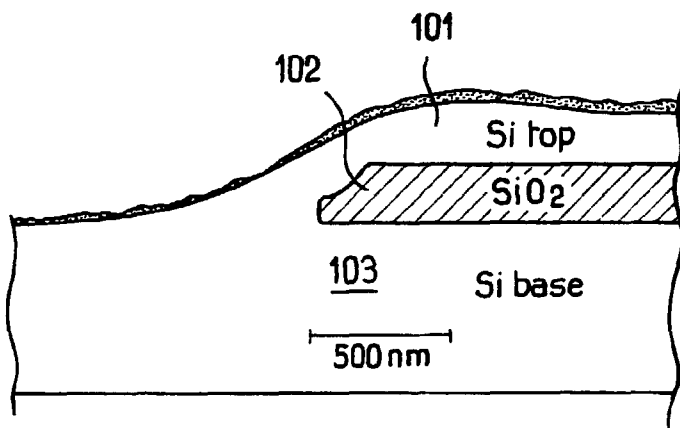
7 April 2005

(15) Information about Correction:

see PCT Gazette No. 14/2005 of 7 April 2005, Section II

For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: PREVENTIVE TREATMENT PROCESS FOR THE RING OF A MULTILAYER WAFER



(57) Abstract: The invention concerns a process for treatment of the ring of a multilayer wafer made by layer transfer and composed of materials chosen from among semiconducting materials, said wafer comprising at least an intermediate layer between a superficial region and a base layer, characterised in that the process includes rapid thermal annealing of the wafer to cause overlapping and encapsulation of the peripheral edge of said intermediate layer, by a layer of said superficial region of the surface of the wafer in order to prevent the attack on the peripheral part of said intermediate layer of the wafer during a subsequent treatment step of the wafer. The invention also concerns an associated multilayer wafer.

WO 2004/079801 A1