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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for all designations*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

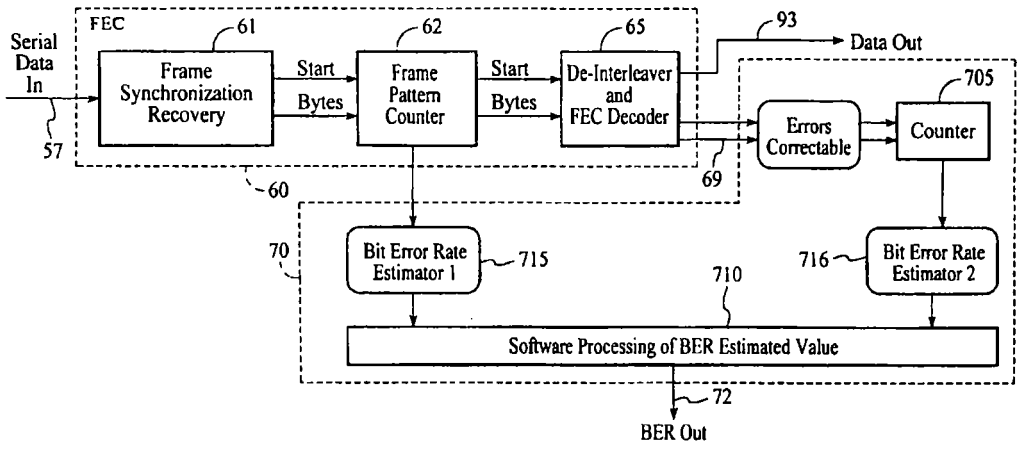
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(54) Title: DUAL BIT ERROR RATE ESTIMATION IN A QAM DEMODULATOR



(57) Abstract: A quadrature amplitude modulation type demodulator having a dual bit error rate estimator unit (70) that allows for high bit error rate measurements. The dual bit error rate estimator circuit (70) uses information pertaining to the number of corrected bytes from a forward error correction decoder (60) and the count of recognizable patterns of the frame over a sufficiently large number of frames. The two pieces of information can be compared at the bit error rate levels, where both the pattern recognition counter (62) and the FEC decoder (60) are able to output valid data. A comparison (710) between the two pieces of information provides a way to detect the type of noise which occurs on the network and makes it easier to correct problems in signal transmission.

WO 02/01788 A3

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